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High Frequency Noise Characterization and Modelling of Graphene Field Effect Transistors

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Abstract— This paper presents the small-signal and noise characterisation of different technologies based on CVD and SiC graphene field effect transistors. The noise model, built on noise figure measurements under 50Ω using the F_{50} method, was verified by additional source-pull measurements, with a special care to the GFET stability. The four noise parameters were then extracted using the validated F_{50} model up to 18 GHz and correlations between noise and small-signal parameters were shown for two different configurations: top-gated and back-gated GFETs.

Index Terms— FET, graphene, high frequency noise, source-pull, small signal model

I. INTRODUCTION

GRAPHENE research activities for circuit design have recently started and analogue and RF circuits have already been demonstrated up to microwave frequency range, despite the low maturity of the graphene material. Benefiting from the high carrier mobility and the ambipolar nature of the electronic transport in the graphene field effect transistor (GFET), interesting performances for key RF circuits for signal transmission and reception continue to be reported: [1]-[7]. Most recent results report an 88-100 GHz mixer exhibiting a 18-19 dB conversion loss [1] and an amplifier with 3.4 dB gain and 6.2 dB noise figure at 14.3 GHz, with a matching network only based on microstrip lines [4].

A good modelling of the graphene transistor, based on DC and RF device characterization, is essential for circuits design. So far, only few works related to GFET high frequency (HF) noise characterization and modelling have been reported [8]-[13]. Tanzid et al. reported in [9] the four noise parameters extraction using source-pull measurements of a GFET transistor, biased at the highest possible g_m . In regards to the tremendous literature of the graphene FET and f_T/f_{max} measurements, the poor literature on HF noise characterization topic is directly correlated to the complexity of this characterization type. In fact, the HF noise measurements are

highly complex and require access to rare characterization facilities containing a source-pull tuner together with a HF noise measurement bench.

Actually, source-pull noise measurements require complicated calibration, since the source-pull tuner and the noise receiver need to be calibrated before measuring the device under test. Then, DC and S-parameters of the device under test have to be recorded before the noise figure measurements. This long characterization process may degrade the noise measurement accuracy, due to eventual stochastic errors accumulation and degradation of the device under test. These measurements require automatic source-pull measurements that can set the device under an unstable operation by presenting a source coefficient reflection out of its stability region in the Smith chart, leading to oscillations and a potential damage of the transistor. Hence, considering the low maturity of the devices and the difficulty to fabricate them, a special care must be taken for their measurements in order to avoid the transistor's breaking/breakdown.

In this paper, we propose and validate a safe and time-efficient noise characterization and modelling procedure based on the measurement of noise figures under 50Ω (F_{50}) on GFET devices, as initiated in our previous work up to 6 GHz using only F_{50} measurements [8]. Although the F_{50} method proved its efficiency on HEMT [15] and MOSFET [16] devices, it has not been validated so far on emerging transistor technologies such as GFET. In order to validate this technique, the noise model elaborated using F_{50} method was verified for various source impedances thanks to selective source-pull measurements on GFET devices out of their unstable region at 15 GHz. This safe methodology was applied to two different GFET technologies (see Fig. 1): 1) two back-gated graphene transistors with a channel made by graphene grown by chemical vapor deposition (CVD) on copper, 2) three top-gated graphene transistors based on CVD graphene grown on

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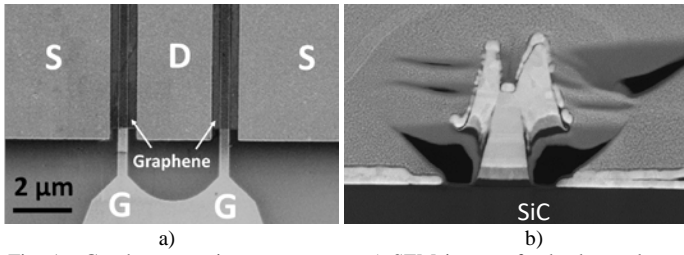


Fig. 1. Graphene transistors structures: a) SEM image of a back-gated CVD GFET; b) Cross section of a top-gated GFET on SiC substrate

Silicon-Carbide (SiC) substrate. The fabrication process is based on our previous work: [11] for CVD on SiO₂ transistors and [13] for CVD on SiC.

First, section II explains the small-signal and noise model parameter extraction procedure. Then, section III details the noise model validation strategy, which leads to the noise parameters extraction results up to 18 GHz. This noise characterization procedure was applied to obtain the results presented in [14].

II. GRAPHENE FET HIGH FREQUENCY MODELLING

A. Measurement setup

The 0.8-18 GHz high frequency noise and source-pull measurement bench is depicted in Fig. 2. The noise receiver is composed of Rohde & Schwarz® FSUP signal source analyzer and a BZ® 0.8-18 GHz wideband amplifier. Using switches at port 1 and port 2, S-parameter measurements up to 26.5 GHz can also be performed with a Keysight® PNA-X. Then, using the same bench, DC, S-parameter measurements and noise measurements up to 18 GHz were carried out under multiple bias points.

B. Small-signal GFET modelling

1) Extrinsic model parameters' extraction

Based on the field-effect transistor noise model described in [17], the small-signal equivalent circuit that we used is illustrated in Fig. 3. The extrinsic part represents the parasitic contribution originated from the accesses of the transistor. They can be modelled by capacitances (C_{pad1} , C_{pad12} and C_{pad2}) and inductances (L_{gx} , L_{dx} and L_{sx}). The capacitances are modelled by a π -network of three capacitances and extracted from a measurement of an open structure fabricated on the same substrate as GFET (see Fig. 4-a-b). The pad inductances are assessed thanks to an ADS-momentum electromagnetic simulation and adjusted on the measured S-parameters of the GFET, because no short test structures were available for the transistors under test on the measured samples. The parasitic contribution of these extrinsic parameter are subtracted out of each transistor S-parameters' measurement using a de-embedding correction.

2) Intrinsic model parameters' extraction

For a given bias point, the intrinsic model parameters are extracted from the de-embedded S-parameters of the GFET using a simple matrix calculation. It is worth to notice that for the intrinsic circuit considered here, the contact resistances are not extracted.

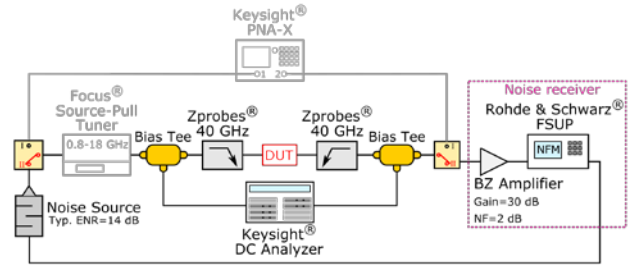


Fig. 2. Block diagram of the on-wafer F50 noise measurement setup up to 18 GHz.

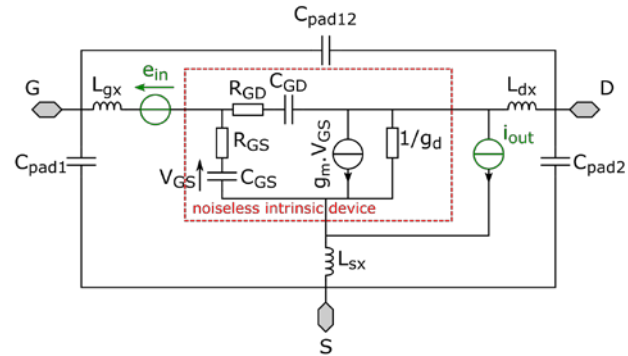


Fig. 3. GFET small-signal and noise equivalent circuit.

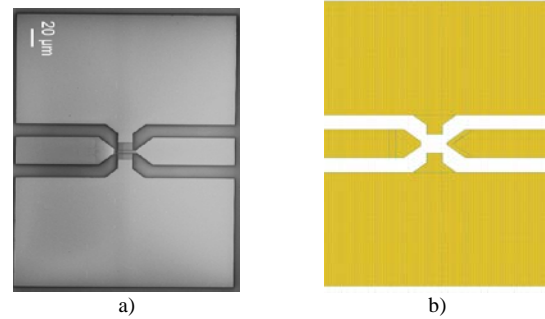


Fig. 4. Picture of test structures: a) transistor, b) Open-Pad dedicated to transistor S-parameters measurement correction (de-embedding).

The same small-signal and noise characterization, modelling procedure was applied to 9 transistors totally. The devices belong to five wafers:

- CVD1: back-gated transistors on silicon substrate with Hall mobility of 2800 cm²/V.s and contact resistance (R_c) of 2 k Ω . μ m
- CVD2: back-gated transistors on silicon substrate with Hall mobility of 2100 cm²/V.s and contact resistance of 125 Ω . μ m
- SiC_A: bilayer graphene growth by CVD on SiC substrate with mobility of 850 cm²/V.s, R_c =650 Ω . μ m
- SiC_B: monolayer graphene growth by CVD on SiC substrate with mobility of 3200 cm²/V.s
- SiC_C: graphene growth by graphitization of SiC substrate with mobility of 600 cm²/V.s, R_c =990 Ω . μ m

For transistors on silicon substrate, the mobilities were measured from Van der Pauw structures using Hall effect measurement. For transistors on SiC substrate, the mobilities were extracted from non-contact Terahertz spectroscopic measurement technique [18]. The transmission line measurement (TLM) approach is used to extract contact

resistance as illustrated in [19]. The TLM structures were fabricated on the same together chip with graphene transistors.

Table I summarizes the best f_T and f_{max} couples for each type of transistors.

As an example, the small-signal characterization and modelling procedure of the SiC_A GFET will be detailed in the paper. This transistor under test was biased at a fixed value of 1.5 V drain-to-source voltage (close to maximum g_m for this transistor) and the gate-to-source voltage was swept from 0 to 1.2 V with a 0.1 V-step.

In the small-signal equivalent circuit parameters extraction procedure, the intrinsic capacitances' mean values are averaged over the whole measurement frequency range, the intrinsic resistances' mean are obtained at high frequency (since they are masked by the capacitances at lower frequencies), between 14 and 16 GHz, and the conductance at 5 GHz (see Fig. 5). The small-signal extrinsic and intrinsic parameters extraction results are respectively given in Table II and Table III.

TABLE I
BEST EXTRINSIC (AS-MEASURED) RF PERFORMANCES OF THE 5 CVD AND SiC GFET TECHNOLOGIES

	CVD1	CVD2	SiC_A	SiC_B	SiC_C
W_g	2×12 μm	2×12 μm	2×15 μm	2×15 μm	12 μm
l_g	200 nm	300 nm	80 nm	80 nm	140 nm
f_T	5 GHz	19 GHz	28 GHz	19 GHz	25 GHz
f_{max}	3 GHz	12 GHz	17 GHz	17 GHz	19 GHz

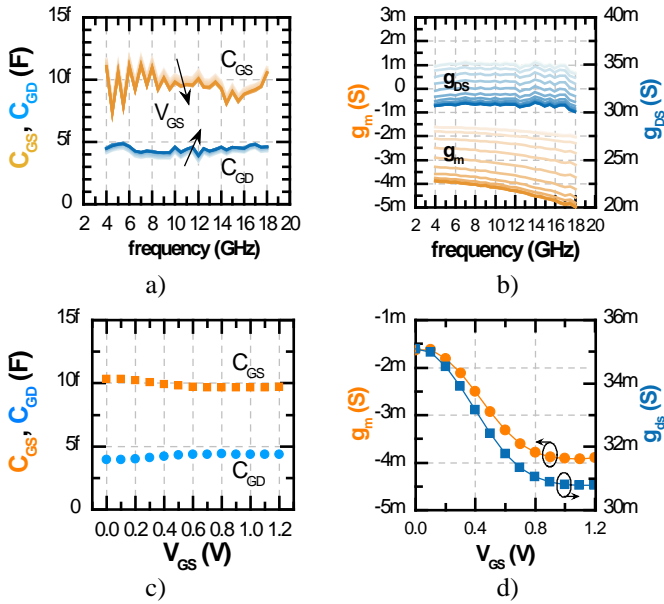


Fig. 5. Intrinsic capacitances and conductances extraction versus frequency and gate voltage: $V_{DS}=1.5V$, $V_{GS}=0-1.2V$ with 0.1V-step. Transistor under test: SiC_A GFET, $W=2 \times 12 \mu m$, $L=150 nm$

TABLE II
EXTRINSIC PARAMETERS FOR CVD2 AND SiC_A GFETS

	C_{pad1}	C_{pad12}	C_{pad2}	L_{gx}	L_{dx}	L_{sx}
CVD2	8.1 fF	1 fF	8.2 fF	58 pH	38 pH	1pH
SiC_A	8.2 fF	0.7 fF	7.8 fF	60 pH	40 pH	0 pH

TABLE III

INTRINSIC PARAMETERS FOR CVD2 SiC_A GFET AT $V_G=0.7$ AND 1V				
	R_{GS}/R_{GD}	C_{GS}/C_{GD}	g_m	g_{ds}
CVD2	63 / 98 Ω	38 / 45 fF	-10.3 mS	26 mS
SiC_A	100/100 Ω	9.7 / 4.4 fF	-3.8 mS	31 mS

C. High frequency noise modelling

The noise equivalent circuit is depicted in Fig. 3 and is based on [17]. The intrinsic part of the device is considered as noiseless. The noise model relies on two extrinsic uncorrelated noise sources, respectively an input voltage noise source e_{in} and an output current noise source i_{out} . These two noise sources are related to the electrical equivalent circuit as given in equations 1 and 2:

$$\overline{e_{in}^2} = 4kT_{in}Re(H_{11})\Delta f \quad (1)$$

$$\overline{i_{out}^2} = 4kT_{out}Re(H_{22})\Delta f \quad (2)$$

Following the noise modelling procedure described in [17], T_{in} is approximated by the ambient temperature and T_{out} is adjusted to fit the measured noise figure up to 18 GHz curve for each V_{GS} value (see Fig. 6). With measured noise figures standing between 20 and 30 dB for SiC GFET (see Fig. 7-a) and between 10 and 16 dB for CVD GFET (See Fig. 7-b), the T_{out} values range between 400 and 1300 K. These high values of noise figures or noise temperatures can be explained by the dependence of T_{out} on the drain current density J_{DS} , which is specific to field effect transistors [20][21]. As shown in Fig. 6, T_{out} shows a linear dependence on J_{DS} for most of the measured CVD and SiC GFETs, which were biased close to maximum g_m . In fact, SiC GFETs feature higher current densities due to a high residual carrier density in the graphene sheet compared to CVD GFETs which reduces the access resistance. Furthermore, the NF_{50} measurement accuracy (see Fig. 7) is affected by the impedance mismatch at the input of the transistor. Indeed, under 50 Ω input impedance, the graphene transistors show a small gain ($|S_{21}| < -15$ dB) and a high level of noise, which results in a ± 1 dB NF_{50} measurement accuracy.

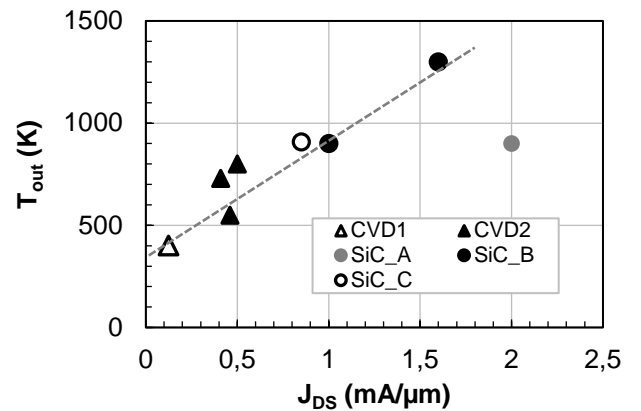


Fig. 6. Output equivalent temperature versus drain-to-source current density for different technologies of CVD and SiC GFETs. The dashed line only provides a visual guide (not a fit to the experimental data).

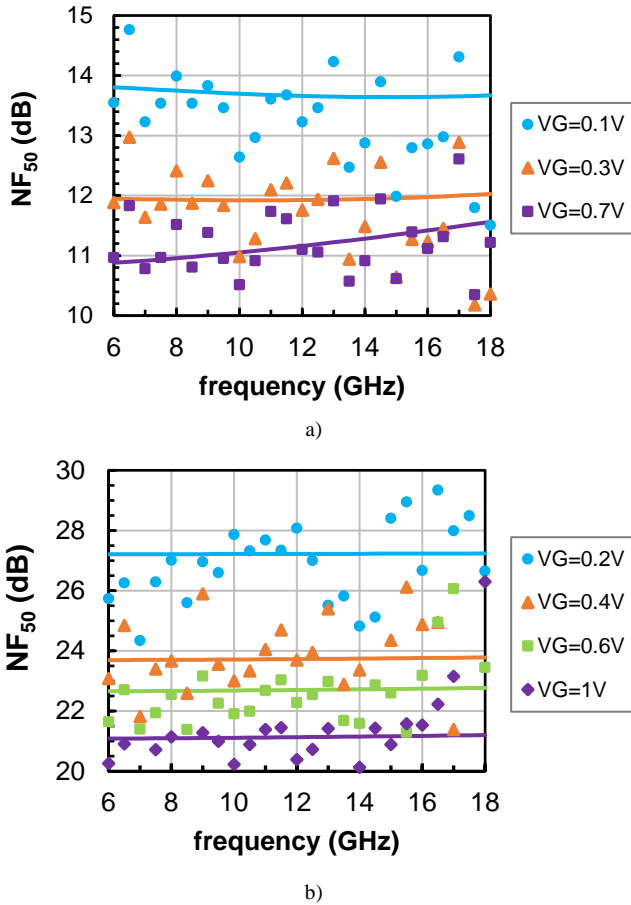


Fig. 7. Measured and simulated noise figure under $50\ \Omega$ versus frequency up to 18 GHz for: a) CVD2 GFET; b) SiC_A GFET.

III. NOISE PARAMETER EXTRACTION

A. Small-signal model validation up to 18 GHz

An accurate modelling of the transistor's S-parameters is crucial to accurately estimate the transistor's gain and precisely assess the optimum noise reflection coefficient Γ_{opt} .

Following the small-signal equivalent circuit procedure described in Section II, a satisfying agreement was obtained from 4 to 18 GHz between the simulated and the measured S-parameters for SiC_A GFET as shown in Fig. 8. This guarantees the accuracy of the simulated gain through the final small-signal and noise model.

B. Noise model validation by source-pull measurements at 15 GHz

The source-pull tuner was used to vary the source impedance, Γ_s , presented to the transistor at its gate input terminal. While monitoring the drain current to detect any instability that could damage the transistor, we chose to first increase the magnitude and then increase the phase by keeping the magnitude constant.

An example of the design of experiment (DOE) is given in Fig. 9. The quarter top right of the Smith Chart was selected in order to be close to the optimum noise area, which approximately corresponds to the conjugate of parameter S_{11} for FETs.

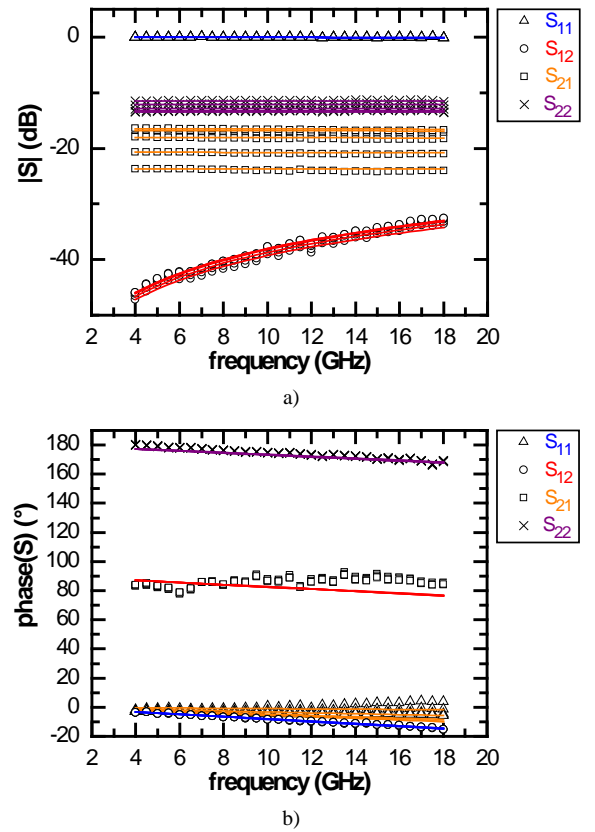


Fig. 8. Measured and simulated S-parameters versus frequency up to 18 GHz for SiC_A GFET: a) in magnitude; b) in phase. Bias conditions: $V_{DS}=1.5\text{V}$, $V_{GS}=0.2\text{-}1\text{V}$ (step=0.2V)

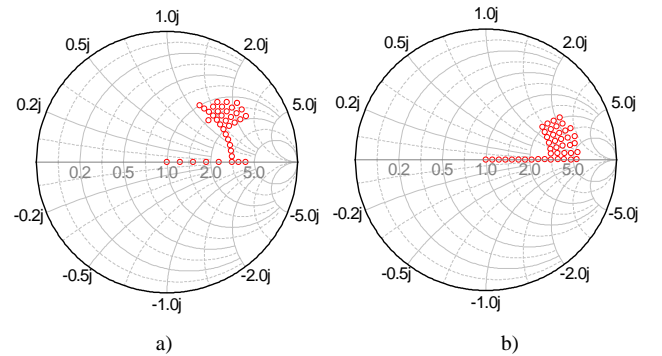


Fig. 9. Synthesized impedances for source-pull measurements at 15 GHz for a) CVD2 and b) SiC_A GFETs. Γ_s is increased from 0 to 0.7 and then for a fixed magnitude the phase is increased from 0° to 30° .

The measurement frequency was fixed to 15 GHz, reasonably far from the source-pull tuner calibration frequency limit at 18 GHz. Moreover, when increasing the magnitude of Γ_s , the upper limit was fixed to $|\Gamma_s|=0.7$. Indeed, above 0.7 and close to 18 GHz, the source-pull tuner shows more and more insertion loss, which strongly affects the sensitivity of the noise figure meter and consequently degrades the noise figure measurement accuracy.

In order to reproduce the source-pull setup measurements, the F_{50} noise model was simulated using the measured source impedances as Port-1 terminal impedance. The comparison between the simulated and measured noise figure and

associated gain, when sweeping Γ_S magnitude and phase, is respectively shown in Fig. 10 and 11. The agreement between noise measurement and simulation is satisfying, especially for this delicate type of measurement. On noise figures, we observed a 0.3 dB mean error (2%) with magnitude sweep and 1.4 dB mean error (9%) with phase sweep. The measurement and simulation of the associated gain are quasi-superimposed, proving the accurate modelling of the S-parameters. This agreement between the simulated F_{50} data and the source-pull noise measurements at 15 GHz indicates that the F_{50} method can be applied to extract the HF noise parameters of graphene transistors.

C. Noise parameters extraction up to 18 GHz

The two-port noise figure as function of the source impedance is expressed by equation (3):

$$F(\Gamma_S) = F_{min} + \frac{4R_n}{z_0} \times \frac{|\Gamma_{opt} - \Gamma_S|^2}{|1 + \Gamma_{opt}|^2 \times (1 - |\Gamma_S|^2)} \quad (3)$$

where F_{min} , R_n and Γ_{opt} represents the noise parameters as defined in [22].

The noise and small-signal modelling procedure was applied to the five transistors whose f_{tr}/f_{max} are presented in Table 1. The noise parameters of each transistor were simulated from the corresponding F_{50} noise model using Keysight® ADS RF simulator. The validity of the noise parameters extraction was verified by computing the Lange noise parameter, N [20]. Considering all the transistors, quantity $4NT_0/T_{min}$ stands between 1 and 2 for the entire frequency range from 2 to 18

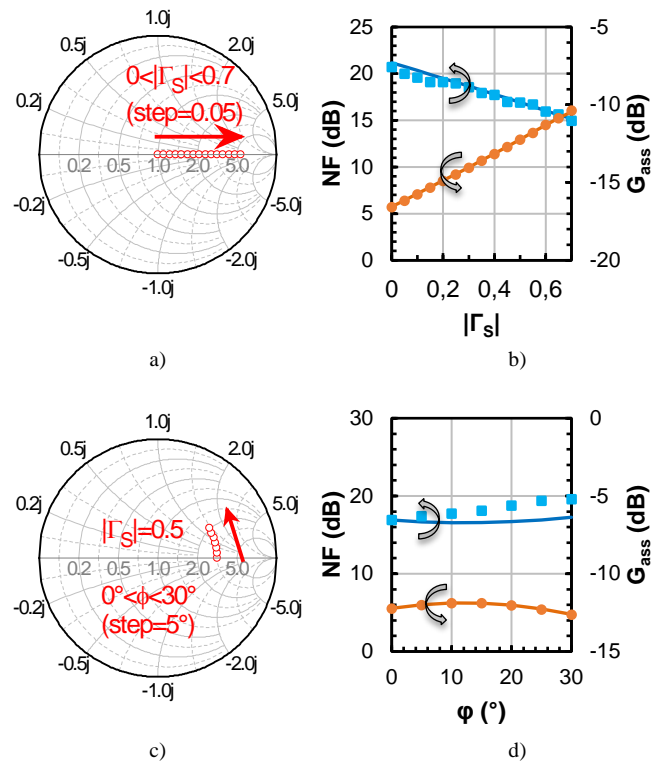


Fig. 11. Noise figures at 15 GHz versus $|\Gamma_S|$ for SiC_A GFET: a) DOE with Γ_S magnitude increase; b) measured and simulated noise figure and associated gain according to DOE-a; c) DOE with Γ_S phase increase at $|\Gamma_S|=0.5$; d) measured and simulated noise figure and associated gain according to DOE-c.

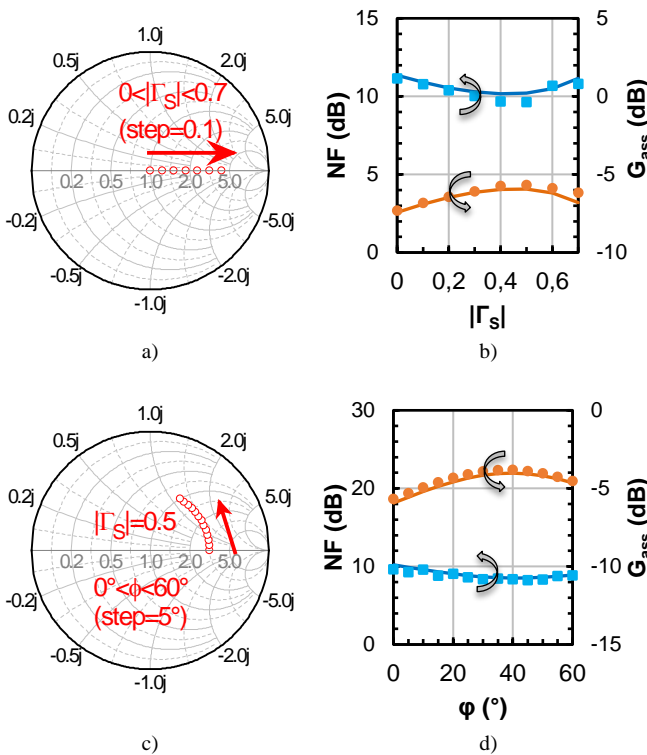


Fig. 10. Noise figures at 15 GHz versus $|\Gamma_S|$ for CVD2 GFET: a) DOE with Γ_S magnitude increase; b) measured and simulated noise figure and associated gain according to DOE-a; c) DOE with Γ_S phase increase at $|\Gamma_S|=0.5$; d) measured and simulated noise figure and associated gain according to DOE-c.

GHz. This validated the physical aspect of the extracted noise parameters. The minimum noise figures and associated gains for all characterized transistors are depicted in Fig. 12. The intersection point between NF_{min} and G_{ass} marks the upper frequency limitation for low noise amplifier design consideration using each device. Then, last generations of GFETs on SiC (SiC_A and SiC_B) show higher gain and lower noise than CVD GFETs and seem to be more suitable for RF design above 9 GHz. The main challenge lies in the matching solution, since the optimum source reflection coefficient is located at the border of the Smith Chart for these transistors.

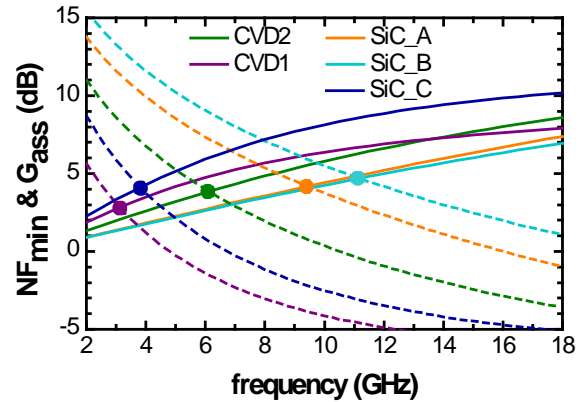


Fig. 12. Extraction of the GFETs minimum noise figure (straight line) and associated gain (dashed line) using the noise model from 2 to 18 GHz

D. Noise parameters correlation with model parameters

In order to quantify the impact of the small-signal model parameters on the noise performances, the correlation between the transconductance and the output conductance and the four noise parameters was studied. To equally compare the five types of GFETs, g_m and g_{ds} was normalized by the gate width, as shown in Fig. 13 and 14. NF_{min} and R_n are plotted at both 2 and 10 GHz to allow comparison with the state-of-the-art CVD GFET at 2 GHz [9] (ref_CVD) and SiC GFET at 10 GHz [12] (ref_SiC). As expected [20], NF_{min} shows a linear evolution with respect of g_m/W for most of transistors, especially CVD GFETs. However, increasing simultaneously g_m and g_{ds} for both types of GFETs allows a reduction of the transistor's noise but it has also a positive impact on R_n and $|F_{opt}|$. In fact, from transistor technology's point of view, decreasing R_n is of utmost importance to minimize the sensitivity to noise mismatch and reducing $|F_{opt}|$ offers realistic matching conditions, possibly using small passive devices.

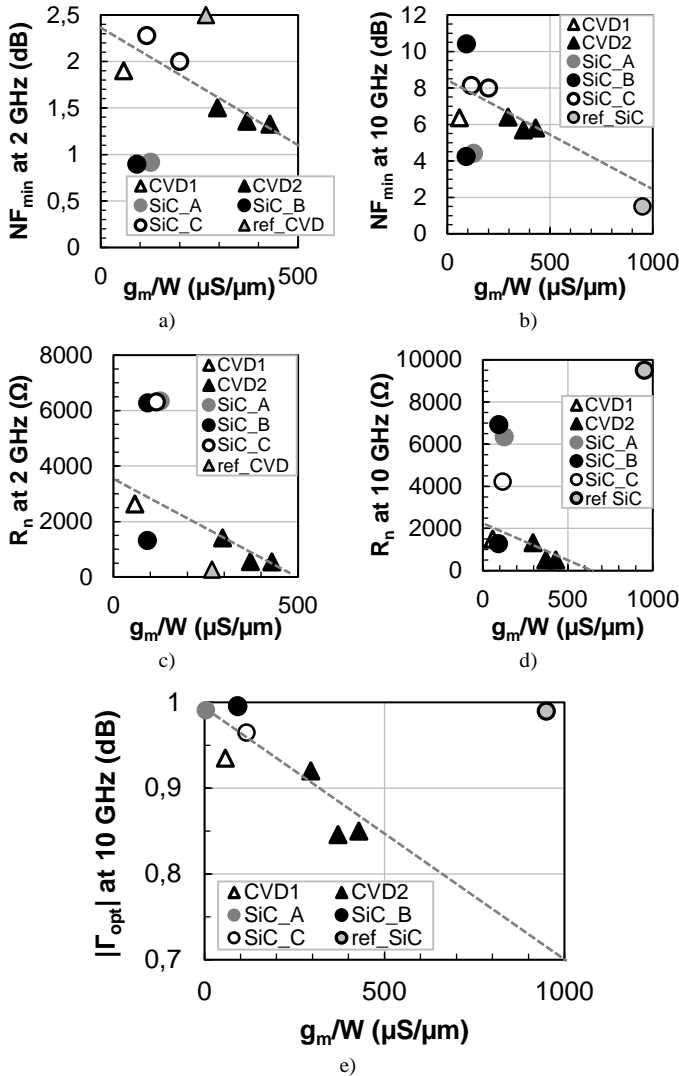


Fig. 13. Noise parameters versus transconductance normalized by gate width. The dashed lines only provide a visual guide (not a fit to the experimental data).

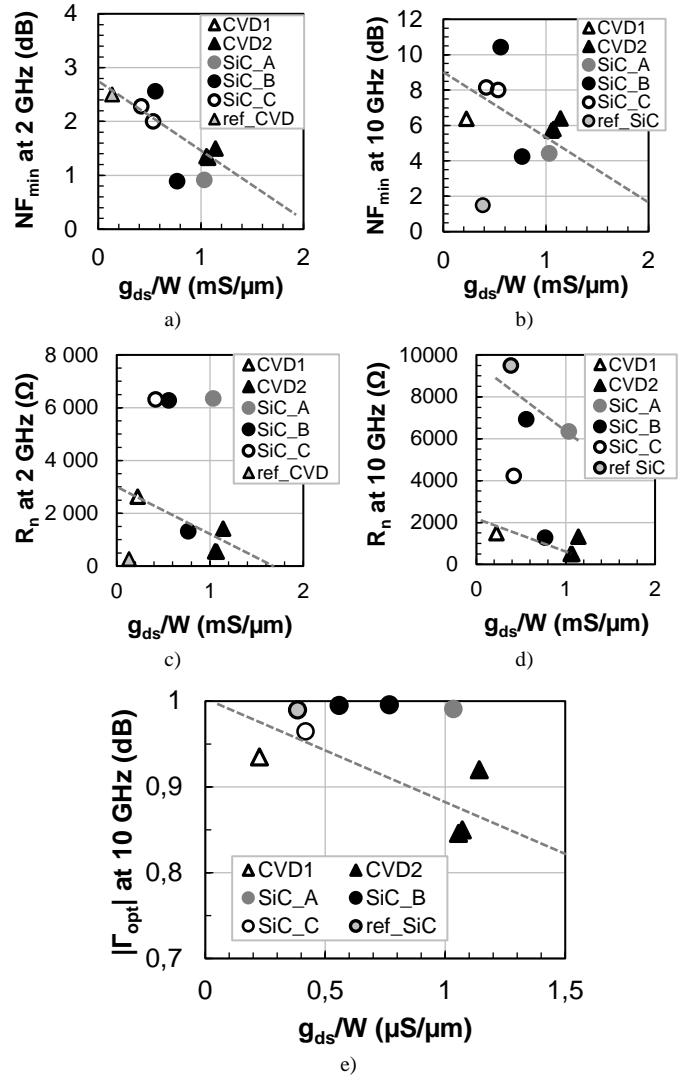


Fig. 14. Noise parameters versus output conductance normalized by gate width. The dashed lines are only a guide to the eye (not a fit to the experimental data).

IV. CONCLUSION

The high frequency noise and small-signal characterization and modelling of CVD graphene grown GFETs and SiC GFETs up to 18 GHz was presented. Based on the $F50$ method, the noise parameter extraction was completed using a noise model that was validated by additional and selective source-pull measurements. This work shows that, combined with S-parameter measurements, simple noise figure measurements under 50Ω are sufficient to build an accurate noise model in order to estimate the high frequency noise performance of a FET technology. For the first time, this safe, time-efficient and cost-effective methodology was validated by the characterization of GFETs fabricated using different process and graphene materials. This suggests its possible extension for high frequency noise characterization of other emerging transistors technology based on low dimensional materials. Furthermore, its application to several GFETs has clearly shown that g_m and g_{ds} are key parameters to improve f_T and f_{max} , but also the noise parameters such as NF_{min} , R_n or F_{opt} of the graphene transistors.

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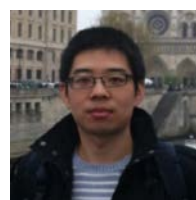
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