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To cite this version:
Marina Deng, Dalal Fadil, Wei Wei, Emiliano Pallecchi, Henri Happy, et al.. High-Frequency Noise Characterization and Modeling of Graphene Field-Effect Transistors. IEEE Transactions on Microwave Theory and Techniques, 2020, 68 (6), pp.2116-2123. 10.1109/TMTT.2020.2982396. hal-02540064

HAL Id: hal-02540064
https://hal.science/hal-02540064
Submitted on 5 Jul 2021

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High Frequency Noise Characterization and Modelling of Graphene Field Effect Transistors

M. Deng, Member, IEEE, D. Fadil, W. Wei, E. Pallecchi, H. Happy, G. Dambrine, Fellow IEEE, M. De Matos, T. Zimmer, Senior Member, IEEE, S. Fregonese

Abstract—This paper presents the small-signal and noise characterisation of different technologies based on CVD and SiC graphene field effect transistors. The noise model, built on noise figure measurements under 50Ω using the $F_{50}$ method, was verified by additional source-pull measurements, with a special care to the GFET stability. The four noise parameters were then extracted using the validated $F_{50}$ model up to 18 GHz and correlations between noise and small-signal parameters were shown for two different configurations: top-gated and back-gated GFETs.

Index Terms—FET, graphene, high frequency noise, source-pull, small signal model

I. INTRODUCTION

GRAPHENE research activities for circuit design have recently started and analogue and RF circuits have already been demonstrated up to microwave frequency range, despite the low maturity of the graphene material. Benefiting from the high carrier mobility and the ambipolar nature of the electronic transport in the graphene field effect transistor (GFET), interesting performances for key RF circuits for signal transmission and reception continue to be reported: [1]-[7]. Most recent results report an 88-100 GHz mixer exhibiting a 18-19 dB conversion loss [1] and an amplifier with 3.4 dB gain and 6.2 dB noise figure at 14.3 GHz, with a matching network only based on microstrip lines [4].

A good modelling of the graphene transistor, based on DC and RF device characterization, is essential for circuits design. So far, only few works related to GFET high frequency (HF) noise characterization and modelling have been reported [8]-[13]. Tanzid et al. reported in [9] the four noise parameters extraction using source-pull measurements of a GFET transistor, biased at the highest possible $g_m$. In regards to the tremendous literature of the graphene FET and $f_{r}/f_{max}$ measurements, the poor literature on HF noise characterization topic is directly correlated to the complexity of this characterization type. In fact, the HF noise measurements are highly complex and require access to rare characterization facilities containing a source-pull tuner together with a HF noise measurement bench.

Actually, source-pull noise measurements require complicated calibration, since the source-pull tuner and the noise receiver need to be calibrated before measuring the device under test. Then, DC and S-parameters of the device under test have to be recorded before the noise figure measurements. This long characterization process may degrade the noise measurement accuracy, due to eventual stochastic errors accumulation and degradation of the device under test. These measurements require automatic source-pull measurements that can set the device under an unstable operation by presenting a source coefficient reflection out of its stability region in the Smith chart, leading to oscillations and a potential damage of the transistor. Hence, considering the low maturity of the devices and the difficulty to fabricate them, a special care must be taken for their measurements in order to avoid the transistor’s breaking/breakdown.

In this paper, we propose and validate a safe and time-efficient noise characterization and modelling procedure based on the measurement of noise figures under 50 Ω ($F_{50}$) on GFET devices, as initiated in our previous work up to 6 GHz using only $F_{50}$ measurements [8]. Although the $F_{50}$ method proved its efficiency on HEMT [15] and MOSFET [16] devices, it has not been validated so far on emerging transistor technologies such as GFET. In order to validate this technique, the noise model elaborated using $F_{50}$ method was verified for various source impedances thanks to selective source-pull measurements on GFET devices out of their unstable region at 15 GHz. This safe methodology was applied to two different GFET technologies (see Fig. 1): 1) two back-gated graphene transistors with a channel made by graphene grown by chemical vapor deposition (CVD) on copper, 2) three top-gated graphene transistors based on CVD graphene grown on...
Silicon-Carbide (SiC) substrate. The fabrication process is based on our previous work: [11] for CVD on SiO2 transistors and [13] for CVD on SiC.

First, section II explains the small-signal and noise model parameter extraction procedure. Then, section III details the noise model validation strategy, which leads to the noise parameters extraction results up to 18 GHz. This noise characterization procedure was applied to obtain the results presented in [14].

II. GRAPHENE FET HIGH FREQUENCY MODELLING

A. Measurement setup

The 0.8-18 GHz high frequency noise and source-pull measurement bench is depicted in Fig. 2. The noise receiver is composed of Rohde & Schwarz® FSUP signal source analyzer and a BZ® 0.8-18 GHz wideband amplifier. Using switches at port 1 and port 2, S-parameter measurements up to 26.5 GHz can also be performed with a Keysight® PNA-X. Then, using the same bench, DC, S-parameter measurements and noise measurements up to 18 GHz were carried out under multiple bias points.

B. Small-signal GFET modelling

1) Extrinsic model parameters’ extraction

Based on the field-effect transistor noise model described in [17], the small-signal equivalent circuit that we used is illustrated in Fig. 3. The extrinsic part represents the parasitic contribution originated from the accesses of the transistor. They can be modelled by capacitances ($C_{pad1}$, $C_{pad12}$ and $C_{pad2}$) and inductances ($L_{gx}$, $L_{dx}$ and $L_{sx}$). The capacitances are modelled by a π-network of three capacitances and extracted from a measurement of an open structure fabricated on the same substrate as GFET (see Fig. 4-a-b). The pad inductances are assessed thanks to an ADS-momentum electromagnetic simulation and adjusted on the measured S-parameters of the GFET, because no short test structures were available for the transistors under test on the measured samples. The parasitic contribution of these extrinsic parameter are subtracted out of each transistor S-parameters’ measurement using a de-embedding correction.

2) Intrinsic model parameters’ extraction

For a given bias point, the intrinsic model parameters are extracted from the de-embedded S-parameters of the GFET using a simple matrix calculation. It is worth to notice that for the intrinsic circuit considered here, the contact resistances are not extracted.

For transistors on silicon substrate, the mobilities were measured from Van der Pauw structures using Hall effect measurement. For transistors on SiC substrate, the mobilities were extracted from non-contact Terahertz spectroscopic measurement technique [18]. The transmission line measurement (TLM) approach is used to extract contact
resistance as illustrated in [19]. The TLM structures were fabricated on the same together chip with graphene transistors.

Table I summarizes the best $f_T$ and $f_{max}$ couples for each type of transistors.

As an example, the small-signal characterization and modelling procedure of the SiC_A GFET will be detailed in the paper. This transistor under test was biased at a fixed value of 1.5 V drain-to-source voltage (close to maximum paper. This transistor under test was biased at a fixed value of 1.5 V drain-to-source voltage (close to maximum

In the small-signal equivalent circuit parameters extraction procedure, the intrinsic capacitances’ mean values are averaged over the whole measurement frequency range, the intrinsic resistances’ mean are obtained at high frequency (since they are masked by the capacitances at lower frequencies), between 14 and 16 GHz, and the conductance at 5 GHz (see Fig. 5). The small-signal extrinsic and intrinsic parameters extraction results are respectively given in Table II and Table III.

### Table I

<table>
<thead>
<tr>
<th></th>
<th><strong>CVD1</strong></th>
<th><strong>CVD2</strong></th>
<th><strong>SiC_A</strong></th>
<th><strong>SiC_B</strong></th>
<th><strong>SiC_C</strong></th>
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<td>$w_g$ (µm)</td>
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<td>2x12</td>
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<td>2x15</td>
<td>12</td>
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<tr>
<td>$L_D$ (nm)</td>
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<td>80</td>
<td>80</td>
<td>140</td>
</tr>
<tr>
<td>$f_T$ (GHz)</td>
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<td>19</td>
<td>28</td>
<td>19</td>
<td>25</td>
</tr>
<tr>
<td>$f_{max}$ (GHz)</td>
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<td>12</td>
<td>17</td>
<td>17</td>
<td>19</td>
</tr>
</tbody>
</table>

**Extrinsic parameters for CVD2 and SiC_A GFETs**

<table>
<thead>
<tr>
<th></th>
<th>$C_{pad}$</th>
<th>$C_{pad12}$</th>
<th>$C_{pad2}$</th>
<th>$L_g$</th>
<th>$L_d$</th>
<th>$L_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVD2</td>
<td>8.1 nF</td>
<td>1 nF</td>
<td>8.2 nF</td>
<td>58 pF</td>
<td>38 pF</td>
<td>1 pF</td>
</tr>
<tr>
<td>SiC_A</td>
<td>8.2 nF</td>
<td>0.7 nF</td>
<td>7.8 nF</td>
<td>60 pF</td>
<td>40 pF</td>
<td>0 pF</td>
</tr>
</tbody>
</table>

### C. High frequency noise modelling

The noise equivalent circuit is depicted in Fig. 3 and is based on [17]. The intrinsic part of the device is considered as noiseless. The noise model relies on two extrinsic uncorrelated noise sources, respectively an input voltage noise source $e_{in}$ and an output current noise source $i_{out}$. These two noise sources are related to the electrical equivalent circuit as given in equations 1 and 2:

$$\bar{e_{in}^2} = 4kTinRe(H_{11})\Delta f$$

$$\bar{i_{out}^2} = 4kTonRe(H_{22})\Delta f$$

Following the noise modelling procedure described in [17], $T_{in}$ is approximated by the ambient temperature and $T_{out}$ is adjusted to fit the measured noise figure up to 18 GHz curve for each $V_{GS}$ value (see Fig. 6). With measured noise figures standing between 20 and 30 dB for SiC GFET (see Fig. 7-a) and between 10 and 16 dB for CVD GFET (See Fig. 7-b), the $T_{out}$ values range between 400 and 1300 K. These high values of noise figures or noise temperatures can be explained by the dependence of $T_{out}$ on the drain current density $J_{DS}$, which is specific to field effect transistors [20][21]. As shown in Fig. 6, $T_{out}$ shows a linear dependence on $J_{DS}$ for most of the measured CVD and SiC GFETs, which were biased close to maximum $g_m$. In fact, SiC GFETs feature higher current densities due to a high residual carrier density in the graphene sheet compared to CVD GFETs which reduces the access resistance. Furthermore, the $NF_{50}$ measurement accuracy (see Fig. 7) is affected by the impedance mismatch at the input of the transistor. Indeed, under 50 Ω input impedance, the graphene transistors show a small gain ($|S_{21}|$<-15 dB) and a high level of noise, which results in a ±1 dB $NF_{50}$ measurement accuracy.
Fig. 7. Measured and simulated noise figure under 50 Ω versus frequency up to 18 GHz for: a) CVD2 GFET; b) SiC_A GFET.

III. NOISE PARAMETER EXTRACTION

A. Small-signal model validation up to 18 GHz

An accurate modelling of the transistor’s S-parameters is crucial to accurately estimate the transistor’s gain and precisely assess the optimum noise reflection coefficient $\Gamma_{\text{opt}}$.

Following the small-signal equivalent circuit procedure described in Section II, a satisfying agreement was obtained from 4 to 18 GHz between the simulated and the measured S-parameters for SiC_A GFET as shown in Fig. 8. This guarantees the accuracy of the simulated gain through the final small-signal and noise model.

B. Noise model validation by source-pull measurements at 15 GHz

The source-pull tuner was used to vary the source impedance, $\Gamma_S$, presented to the transistor at its gate input terminal. While monitoring the drain current to detect any instability that could damage the transistor, we chose to first increase the magnitude and then increase the phase by keeping the magnitude constant.

An example of the design of experiment (DOE) is given in Fig. 9. The quarter top right of the Smith Chart was selected in order to be close to the optimum noise area, which approximately corresponds to the conjugate of parameter $S_{11}$ for FETs.

The measurement frequency was fixed to 15 GHz, reasonably far from the source-pull tuner calibration frequency limit at 18 GHz. Moreover, when increasing the magnitude of $\Gamma_S$, the upper limit was fixed to $|\Gamma_S|=0.7$. Indeed, above 0.7 and close to 18 GHz, the source-pull tuner shows more and more insertion loss, which strongly affects the sensitivity of the noise figure meter and consequently degrades the noise figure measurement accuracy.

In order to reproduce the source-pull setup measurements, the $F_{50}$ noise model was simulated using the measured source impedances as Port-1 terminal impedance. The comparison between the simulated and measured noise figure and
associated gain, when sweeping $f_S$ magnitude and phase, is respectively shown in Fig. 10 and 11. The agreement between noise measurement and simulation is satisfying, especially for this delicate type of measurement. On noise figures, we observed a 0.3 dB mean error (2%) with magnitude sweep and 1.4 dB mean error (9%) with phase sweep. The measurement and simulation of the associated gain are quasi-superimposed, proving the accurate modelling of the S-parameters. This agreement between the simulated $F_{50}$ data and the source-pull noise measurements at 15 GHz indicates that the $F_{50}$ method can be applied to extract the HF noise parameters of graphene transistors.

C. Noise parameters extraction up to 18 GHz

The two-port noise figure as function of the source impedance is expressed by equation (3):

$$F(G_S) = F_{\text{min}} + \frac{4R_n}{Z_0} \left| \frac{\Gamma_{\text{opt}} - \Gamma_S}{1 + \Gamma_{\text{opt}} \Gamma_S (1 - |\Gamma_S|^2)} \right|^2 \quad (3)$$

where $F_{\text{min}}$, $R_n$ and $\Gamma_{\text{opt}}$ represents the noise parameters as defined in [22].

The noise and small-signal modelling procedure was applied to the five transistors whose $f_t/f_{\text{max}}$ are presented in Table 1. The noise parameters of each transistor were simulated from the corresponding $F_{50}$ noise model using Keysight® ADS RF simulator. The validity of the noise parameters extraction was verified by computing the Lange noise parameter, $N$ [20]. Considering all the transistors, quantity $4NT_0/T_{\text{min}}$ stands between 1 and 2 for the entire frequency range from 2 to 18 GHz. This validated the physical aspect of the extracted noise parameters. The minimum noise figures and associated gains for all characterized transistors are depicted in Fig. 12. The intersection point between $NF_{\text{min}}$ and $G_{\text{ass}}$ marks the upper frequency limitation for low noise amplifier design consideration using each device. Then, last generations of GFETs on SiC (SiC_A and SiC_B) show higher gain and lower noise than CVD GFETs and seem to be more suitable for RF design above 9 GHz. The main challenge lies in the matching solution, since the optimum source reflection coefficient is located at the border of the Smith Chart for these transistors.
D. Noise parameters correlation with model parameters

In order to quantify the impact of the small-signal model parameters on the noise performances, the correlation between the transconductance and the output conductance and the four noise parameters was studied. To equally compare the five types of GFETs, $g_m$ and $g_d$ was normalized by the gate width, as shown in Fig. 13 and 14. $NF_{min}$ and $R_n$ are plotted at both 2 and 10 GHz to allow comparison with the state-of-the-art CVD GFET at 2 GHz [9] (ref_CVD) and SiC GFET at 10 GHz [12] (ref_SiC). As expected [20], $NF_{min}$ shows a linear evolution with respect of $g_m/W$ for most of transistors, especially CVD GFETs. However, increasing simultaneously $g_m$ and $g_d$ for both types of GFETs allows a reduction of the transistor’s noise but it has also a positive impact on $R_n$ and $|\Gamma_{opt}|$. In fact, from transistor technology’s point of view, decreasing $|\Gamma_{opt}|$ offers realistic matching conditions, possibly using small passive devices.

Fig. 13. Noise parameters versus transconductance normalized by gate width. The dashed lines only provide a visual guide (not a fit to the experimental data).

Fig. 14. Noise parameters versus output conductance normalized by gate width. The dashed lines are only a guide to the eye (not a fit to the experimental data).

IV. CONCLUSION

The high frequency noise and small-signal characterization and modelling of CVD graphene grown GFETs and SiC GFETs up to 18 GHz was presented. Based on the $F50$ method, the noise parameter extraction was completed using a noise model that was validated by additional and selective source-pull measurements. This work shows that, combined with S-parameter measurements, simple noise figure measurements under 50 $\Omega$ are sufficient to build an accurate noise model in order to estimate the high frequency noise performance of a FET technology. For the first time, this safe, time-efficient and cost-effective methodology was validated by the characterization of GFETs fabricated using different process and graphene materials. This suggests its possible extension for high frequency noise characterization of other emerging transistors technology based on low dimensional materials. Furthermore, its application to several GFETs has clearly shown that $g_m$ and $g_d$ are key parameters to improve $f_T$ and $f_{max}$ but also the noise parameters such as $NF_{min}$, $R_n$ or $|\Gamma_{opt}|$ of the graphene transistors.
REFERENCES


Marina Deng received the Ph.D. degree in electronics from the University of Lille, Villeneuve-d’Ascq, France, in 2014. During her Ph.D. research with IEMN, she worked on SiGe HBT small-signal and high-frequency noise characterization and modeling in the sub-THz range. Since November 2015, she has been an Associate Professor with the University of Bordeaux, Talence, France, within the MODEL team. Her current research focuses on millimeter-wave and sub-millimeter-wave characterization of HF transistors, including on-wafer calibration and HF noise measurements.

Dalal Fadil received her PhD in Electronics, Microelectronics and Nanoelectronics Engineering in 2011 from University of Caen, France. She worked as postdoctoral research scientist with Carbon group in the IEMN laboratory in 2016 on fabrication and characterization of high frequency transistors based 2D materials, including graphene field effect transistors.

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Gilles Dambrine received the engineer diploma, the Ph.D. degree and the Habilitation à Diriger des Recherches (HDR) degree from the University of Lille, France in 1986, 1989 and 1996 respectively. He was permanent researcher at the CNRS between 1989 and 1999. He is full Professor of Electronic at the University of Lille since 1999. His main research interests are concerned with the characterization and modelling of ultimate low-noise devices for application in millimeter and sub-millimeter wave ranges. Over these few years, his research interests are oriented to the study of the microwave properties and applications of nanodevices. He is author and co-author of 140 papers and communications and 6 chapters of books, in the field of microwave devices. From 2010-2020, he was deputy director of the Institute of Electronics, Microelectronics and Nanotechnologies - IEMN gathering about 500 researchers and PhD students. from 2017 - 2020, he is scientific delegate in charge of industrial partnership and innovation at CNRS headquarter. He received the IEEE Fellow grade in 2016. Since 2018, he is member of EuMA BoD.

Magali De Matos received the M.S. degree in microelectronics from the University of Bordeaux, France in 1999. She then joined the Laboratory of Integration from Materials to Systems, IC Design Team, IMS, University of Bordeaux, as a Research Engineer. Since 2007, she has been in charge of the characterization platform NANOCOM at IMS, providing support to Ph.D. students working in the domains of IC design and compact modeling of devices. She is involved in sub-THz S-parameter characterization with the Nanoelectronics Group.

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Sébastien Fregonese was born in Bordeaux, France, in 1979. He received the M.Sc. and Ph.D. degrees in electronics from Université Bordeaux, Bordeaux, France, in 2002 and 2005, respectively. During his Ph.D. research, he investigated SiGe heterojunction bipolar transistor (HBTs), with emphasis on compact modeling. From 2005 to 2006, he was a Post-Doctoral Researcher with TU Delft, Delft. The Netherlands, where his research activities dealt with the Si strain FET emerging devices, focusing on process and device simulation. In 2007, he joined CNRS, IMS, Bordeaux, as a Researcher. From 2011 to 2012, he was a Visiting Researcher with the University of Lille, France, focusing on the graphene FET device modelling. He is involved in a couple of National and European research projects such as the European FP7 IP Dot5, Dot7, FET GRADE, and H2020 TARANTO. His current research interests include electrical compact modeling and characterization of HF devices such as SiGe HBTs and carbon-based transistors.