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28 Gbps silicon-germanium hetero-structure avalanche photodetectors

(Contributed paper)

Daniel Benedikovic^{a, *}, Léopold Viro^b, Guy Aubin^a, Jean-Michel Hartmann^b, Farah Amar^a, Bertrand Szelag^b, Xavier Le Roux^a, Carlos Alonso-Ramos^a, Paul Crozat^a, Eric Cassan^a, Delphine Marris-Morini^a, Charles Baudot^c, Frédéric Boeuf^c, Jean-Marc Fédéli^b, Christophe Kopp^b and Laurent Vivien^a

^aUniversité Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies, 91120, Palaiseau, France;

^bUniversity Grenoble Alpes and CEA, LETI, Minatec Campus, F-38054 Grenoble, France;

^cTechnology R&D, STMicroelectronics SAS, 850 Rue Jean Monnet, 38920 Crolles, France

ABSTRACT

Owing to its low-cost, high-yield, and dense integration ability, silicon nanophotonics is a good candidate to tackle the needs of exponentially growing communications in data centers, high-performance computers, and cloud services. Moreover, a number of nanophotonic functions are now available on a single chip, as they take advantages of silicon-fabrication process maturity and epitaxial germanium integration. Optical photodetectors are key building blocks in the library of group-IV components and their performances are quite successful nowadays. In particular, silicon-germanium waveguide-integrated photodetectors are fixing new standards for next generation of on-chip interconnects in terms of compactness, speed, power consumption and cost. Indeed, conventional pin photodetectors yield good responsivities (~ 1 A/W in a 1.5 μm wavelength range), high bandwidths (~ 50 GHz), and dark currents well below 1 μA . Despite recent advances, their optical power sensitivities remain rather modest and speeds are limited to 25 Gbps only, however. Compensating for the insufficient photodetector sensitivity requires higher transmitter output powers and therefore higher energy consumption. Additional energy savings can be obtained by eliminating receiver electronics. Alternatively, an appealing approach is to exploit device structures with an internal multiplication gain to lower even more the power budget and improve energy efficiency of chip-based optical links. In this work, we report on waveguide-integrated photodetectors with lateral silicon-germanium-silicon heterojunctions. Here, we present avalanche photodetectors fabricated on 200-mm silicon-on-insulator wafers using complementary metal-oxide-semiconductor-compatible processes. Devices operate in the low-gain-regime to facilitate high-speed link operations at 1.55 μm wavelengths. An error-free signal detection was achieved at 28 Gbps, with power sensitivity of -11 dBm for 10^{-9} bit-error-rate, which is a relevant link rate for emerging chip-scale optical interconnects.

Keywords: silicon photonics, complementary metal-oxide semiconductor technology, optical photodetectors, pin mode operation, avalanche mode operation, germanium, impact ionization, gain, gain-bandwidth product, high-speed links

*e-mail: daniel.benedikovic@c2n.upsaclay.fr

1. INTRODUCTION

Photonic integration technologies are essential for the realization of optical chips and provide an access to many emerging applications. Foreseen applications range from environmental sensing and health monitoring, through object recognition and civil engineering, to optical communications and interconnects, to list a few. The latter areas are key drivers in the field of photonics integration, as optical interconnects are rapidly replacing traditional copper-based electrical wirings in a variety of chip-scale communication links. Indeed, photonic technologies are particularly promising for long-haul optical fiber systems, short-reach data centers, and clouds, among others. Dense integration is a natural route to tackle challenges associated with cost, portability, speed and bandwidth as well as power consumption¹⁻⁴.

Small-sized and high-performance photonic devices were recently integrated in a single chip thanks to a monolithic integration approach^{4,5}. Such achievements were obtained with the help of two group-IV materials: silicon (Si) and germanium (Ge). Si is definitely an indirect bandgap semiconductor, while Ge is almost direct, with a lower bandgap

(0.67 eV \leftrightarrow 1.14 eV at room temperature). Ge thus provides singular advantages and complementarities over pure Si platforms. Group-IV nanophotonics therefore enable complex on-chip functionalities⁶⁻¹⁰, from light generation and modulation to waveguiding and light detection¹¹⁻¹⁴.

Optical photodetectors, devices that convert light into an electrical signal, are crucial components in integrated optical circuits. They were extensively investigated since the late 1990s^{1,14,15-37}. Group-IV optical photodetectors integrated in mature silicon-on-insulator (SOI) waveguide platforms provide many advantages. Their fabrication makes full use of mainstream Si complementary metal-oxide-semiconductor (CMOS) processes, with therefore reproducible yields. They can otherwise be miniaturized and have potential for large-volume integration and therefore lower costs of ownership. III-V photodetectors on SOI substrates may be used as well, through hybrid or heterogeneous integration with bonding or direct hetero-epitaxy^{38,39}. This, however, typically comes hand-in-hand with increased production costs, fabrication complexity and potentially CMOS line contamination. Therefore, the use of group-IV materials seems optimal for the future needs of monolithic chip integration.

Various types of waveguide-integrated optical photodetectors with a p-i-n structure have been studied the last 10 to 15 years. Since the first fabrication of waveguide-integrated diodes by Ahn, *et al.*¹⁹, a large number of homo-junction (full Ge structures)¹⁵⁻²⁸ and hetero-junction (combined Si-Ge structures)²⁹⁻³⁷ devices have been proposed, fabricated and experimentally evaluated. Both types of devices make use of p-i-n junctions, with light absorption in the intrinsic zones. The overall performance of homo-junction photodetectors is limited by process issues (ion implantation for *p*- and *n*-doped regions and metal vias are performed in/on top of Ge) and optical considerations (ultra-weak optical confinement within the intrinsic zone). Such devices are typically less performant compared to their hetero-junction Si-Ge-Si p-i-n counterparts. Full-Ge p-i-n photodetectors have slower responses, decreased responsivity (quantum efficiency) and higher dark current levels¹⁵⁻²⁸. In stark contrast, hetero-structured Si-Ge photodetectors take advantages of advanced fabrication processes. Hetero-junction devices are fabricated with full Si metal via-contacts and doping (by ion implantation)¹⁰. Such an approach avoids Ge process issues and simplifies the process flow. It otherwise yields, because of optical index confinement differences between Ge and Si, a much better light confinement in the intrinsic device zone, significantly improving photodetector performances. Hetero-structured Si-Ge photodetectors have already been demonstrated with significantly better performance metrics across the near-infrared (near-IR) fiber-optic communication wavelengths³¹⁻³⁷.

Although promising, conventional p-i-n diodes typically provide only restricted levels of responsivity due to external quantum efficiency limits. From a system point of view, the device sensitivity for high-speed signals is quite modest in p-i-n photodetectors. Furthermore, simple p-i-n diodes also yield low electrical output levels. Because of that, extra electronic stages with trans-impedance amplifiers (TIA) or limiting amplifiers (LA) are typically attached to the devices. Improved performance photo-detectors can be obtained by switching over to devices that exploit an internal multiplication gain^{1,14,40-48}, i.e. on-chip avalanche photodetectors (APDs). In the course of years, APDs have been fabricated with the following structures: metal-semiconductor-metal (MSM) or separate absorption charge multiplication (SACM). MSM devices are operated at low bias, with fabrication, which is compatible with CMOS tools. They however suffer from high dark currents and degraded sensitivity⁴⁰. In contrast, SACM photodetectors benefit from a low multiplication noise thanks to the use of Si within the region of avalanche multiplication. However, devices with top-illuminated^{41,42} or waveguide-coupled⁴³ architectures call upon high voltages, typically beyond 20 V, and still operate with a bit rate of 10 Gbps only. State-of-the-art Si-Ge APDs can nowadays be operated with voltages lower than 10 V. The working speeds are still limited to 10 Gbps^{44,45} or 25 Gbps⁴⁶⁻⁴⁸, however.

In this work, we present recent results on compact photodetectors with lateral Si-Ge-Si p-i-n hetero-junctions. Photodetectors were fabricated on 200-mm SOI substrates using Si CMOS foundry processes. First, we comprehensively study the opto-electrical properties of waveguide-integrated photodetectors with different waveguide geometries. Photodetectors were operated under low-voltage supplies. At a 1 V reserve bias, devices exhibited dark currents between 5 nA and 150 nA, dark current densities between 0.404 A/cm² and 0.808 A/cm², responsivities (quantum efficiencies) spanning the 0.17 A/W - 1.16 A/W range (14% to 93% range), and -3dB bandwidths in the 7 GHz to 35 GHz range. Next, devices that operate in an avalanche regime were demonstrated, yielding improved signal quality for high-speed signal detections at 1.55 μ m wavelength. An error-free signal detection was achieved at a link rate of 28 Gbps, with a power sensitivity of -11 dBm for a 10⁻⁹ bit-error-rate.

The manuscript is organized as follows. After the introductory *Section 1*, data on device dimensions, fabrication, and characterization are provided in *Section 2*. *Section 3* reports on a low-bias operation of waveguide-integrated Si-Ge-Si p-

i-n photodetectors, while *Section 4* presents recent results for avalanche-mode-operated Si-Ge-Si p-i-n photodetectors. Finally, conclusions are drawn in *Section 5*.

2. DESIGN, FABRICATION AND TESTING

Optical photodetectors with lateral Si-Ge-Si hetero-junctions are shown schematically in Fig. 1. Fig. 1(a) is a cross-sectional schematics of such a photodetector, while Fig. 1(b) is a top view of foundry mask layout. Optical microscopy images of some fabricated photodetectors can be found in Fig. 1(c)

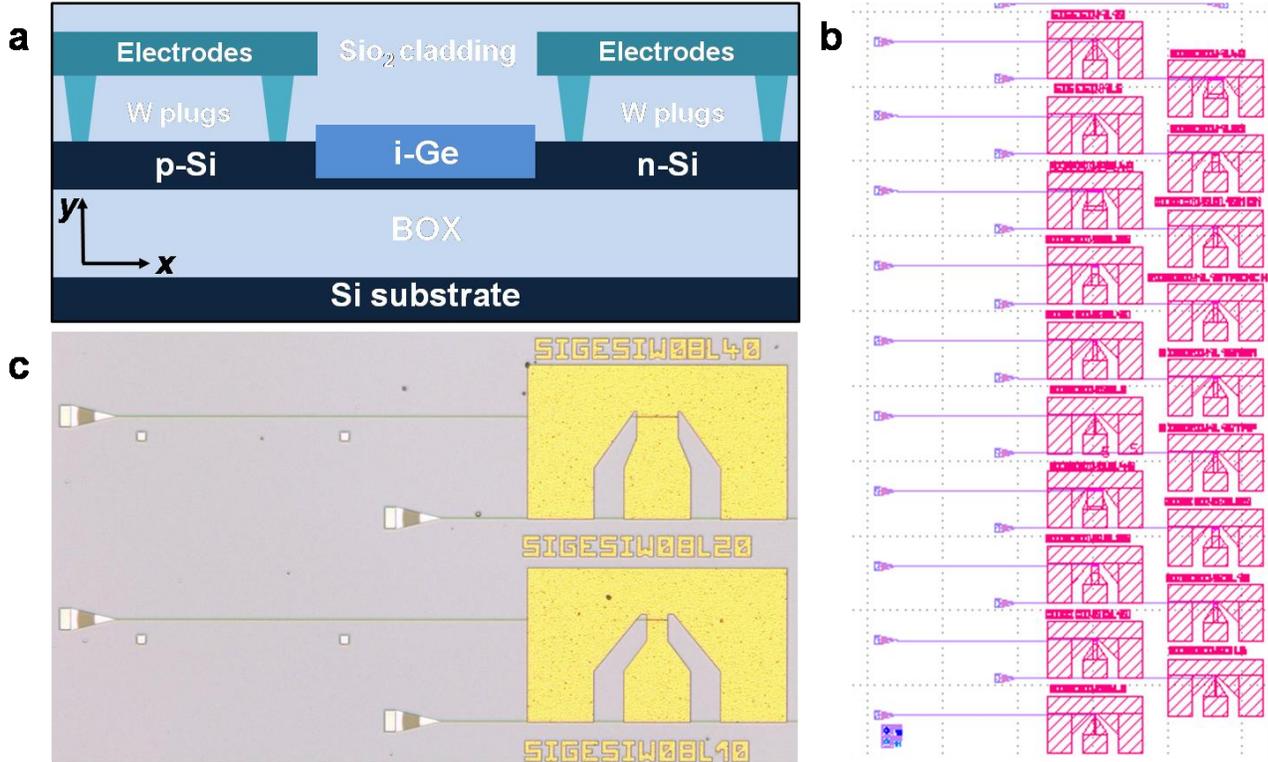


Figure 1. (a) Cross-sectional schematics of a waveguide-integrated photodetector with a lateral silicon-germanium-silicon hetero-junction. (b) Top view of a mask layout with different photodetector geometries. (c) Optical micrograph image of a few fabricated photodetectors.

In this work, optical photodetectors are integrated at the end of SOI waveguides. A butt-waveguide-coupling is used together with lateral p-i-n junctions. The 220 nm thick Si guiding layer is on top of 2- μ m-thick buried oxide (BOX). The integration strategy facilitates the fabrication of small-footprint photodetectors at the end of good optical quality waveguides³⁵. The Ge layer (i.e. the intrinsic photodetector region) is ~260 nm thick. This light-absorbing layer is selectively grown in narrow Si trenches. the remaining Si thickness at the bottom of those trenches is about 60 nm. The active layer is embedded between p-type and n-type Si-doped regions with metal contacts formed on top. Variations in widths (w_i) and lengths (l_i) of the intrinsic device region are included on the mask. Surface grating couplers are used to inject light from an optical fiber into the Si chip. Surface grating couplers and Si interconnecting waveguides are designed to support transverse electric (TE) polarization at 1.55 μ m. The injection Si waveguides are mono-mode, with a cross-section of 220 nm by 500 nm (thickness by width)^{35,36}.

Optical photodetectors were fabricated using CMOS-compatible tools in *CEA LETI's* cleanroom facilities on 200 mm SOI substrates. The fabricated devices were fully characterized in laboratories of *Centre de Nanosciences et de Nanotechnologies* through static current-voltage measurements, small-signal radio-frequency testing, and large-signal data link measurements for eye diagram acquisitions and bit-error-rate assessments, respectively. A detailed description of the manufacturing flow and the comprehensive opto-electrical characterization techniques used on devices can be found elsewhere³⁵⁻³⁷.

3. LOW-BIAS P-I-N MODE OPERATION

Dark- and photo-currents have been evaluated using current-voltage tests without and with light injected into the photodetectors, both as a function of the reverse voltage. Photodetectors of different widths and different lengths have been characterized, in this section, for a low-bias operation, ranging from 0 V to 3 V. Dark-current characteristics of different device geometries are shown in Fig. 2(a). Dark-currents under 1 V reverse bias remain consistently low ($< 1 \mu\text{A}$), typically of the order of a few tens of nA. The largest dark-current levels of around 150 nA are found for the largest devices ($1 \mu\text{m}$ wide and $40 \mu\text{m}$ long). The dark-currents measured in Si-Ge-Si photodetectors are comparable to others hetero-junction devices^{29,30} and considerably lower than in devices with pure Ge junctions^{17,19,20,22,24,26,28}. The dark-current increases with the reverse bias (for a fixed device geometry) and becomes higher when the intrinsic region is less wide (for a fixed bias)³⁷. Small-footprint diodes are desired and preferred, as they facilitate low noise operation, i.e. they yield high signal-to-noise ratios (SNRs). Typically, p-i-n devices driven with low voltages are attached to additional electronics such as TIA and/or LA^{24,28}. In such cases, the overall noise is then dominated by the noise of TIA or LA, which is larger than the dark current.

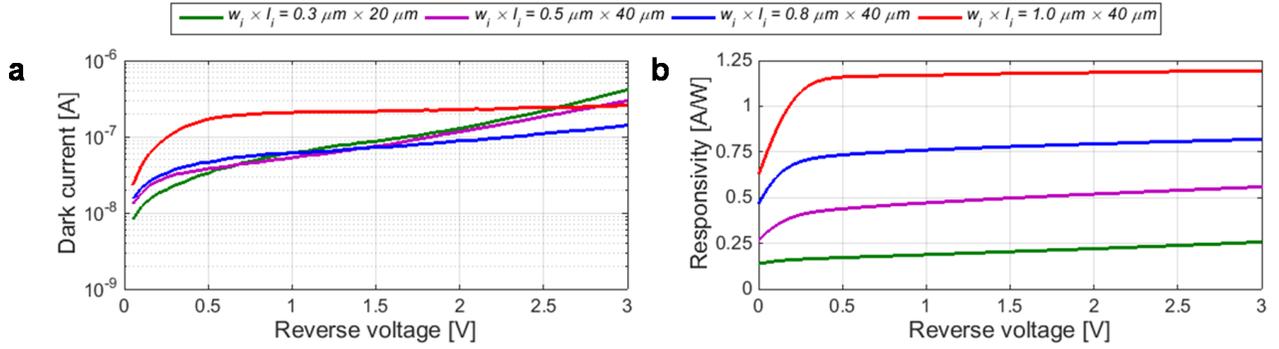


Figure 2. (a) Dark-current and (b) photo-responsivity functions of an applied reverse voltage for different geometries of hetero-structured Si-Ge-Si p-i-n photodetectors. w_i and l_i stand for the width and length of the intrinsic Ge zone.

Figure 2(b) shows the device responsivity as a function as an applied reverse bias at a nominal wavelength of $1.55 \mu\text{m}$. Photo-responsivity is determined from the current-voltage measurements under light illumination as a ratio between the generated photo-current (without a dark-current) and the optical power injected into the device. As shown in Fig. 2(b), wider and longer devices yield higher levels of photo-responsivity. Under 0 V voltage, the responsivity of hetero-structured Si-Ge-Si photodetectors is always low due to the weak built-in electric field. The smallest devices ($0.3 \mu\text{m}$ wide and $20 \mu\text{m}$ long) have only a 0.14 A/W responsivity, while the largest photodetectors ($1 \mu\text{m}$ wide and $40 \mu\text{m}$ long) have a 0.63 A/W responsivity. Furthermore, the responsivity increases with the reverse bias, as a consequence of a higher electric field within the intrinsic Ge zone. The device responsivity consistently reaches plateau at 0.5 V bias, with a very low³⁶ or a moderate voltage dependency for higher bias³⁷. For Fig. 2(b) device geometries, the measured responsivities at 0.5 V reverse bias are equal to 0.17 A/W , 0.44 A/W , 0.73 A/W and 1.16 A/W , respectively. Consequently, waveguide-coupled p-i-n diodes also yield high levels of quantum efficiency near the theoretical limit of 100%. Corresponding quantum efficiencies, at 0.5 V bias and an illumination wavelength of $1.55 \mu\text{m}$, are estimated to be 13.8%, 35.1%, 58.7% and 92.8% for Fig. 2(b) devices.

The bandwidth properties of hetero-structured photodetectors have been studied via small-signal radio-frequency (RF) measurements. Normalized S_{21} traces for different p-i-n photodetectors and different bias (0 V and 1 V) are shown in Figs. 3(a) and 3(b), respectively. The RF tests have been performed at a wavelength of $1.55 \mu\text{m}$, with a power coupled into the device of about -11.4 dBm . Zero-bias operation, shown in Fig. 3(a), yields low cut-off frequencies of 4.8 GHz , 3.8 GHz , 1.3 GHz , and 1.1 GHz for given device geometries. Small cut-off frequencies are attributed to the long transit carrier time and the weak built-in electric field. This agrees with a low responsivity observed under such conditions. In contrast, devices biased at 1 V provide significantly larger -3dB bandwidths of 35 GHz , 24.2 GHz , 15.7 GHz , and 6.7 GHz (see Fig. 3(b)). Under non-zero bias, the improved device bandwidth is also consistent with the enhancement in device responsivity. A summary of -3dB bandwidth versus reverse bias for all tested devices is provided in Fig. 3(c). Narrower photodetectors provide faster response, well beyond 50 GHz for a 2 V biasing. It is otherwise obvious that the -3dB bandwidth increases as the width of the intrinsic Ge region decreases. Moreover, we also observed that for a fixed

width of the intrinsic photodetector region, the extracted cut-off frequencies do not really depend on the length of the intrinsic Ge region^{36,37}. This suggests that the frequency response of the hetero-structured Si-Ge-Si p-i-n photodetectors is not primarily limited by the resistance-capacitance (RC) delay. The main limitation for the device speed is setup by the transit time.

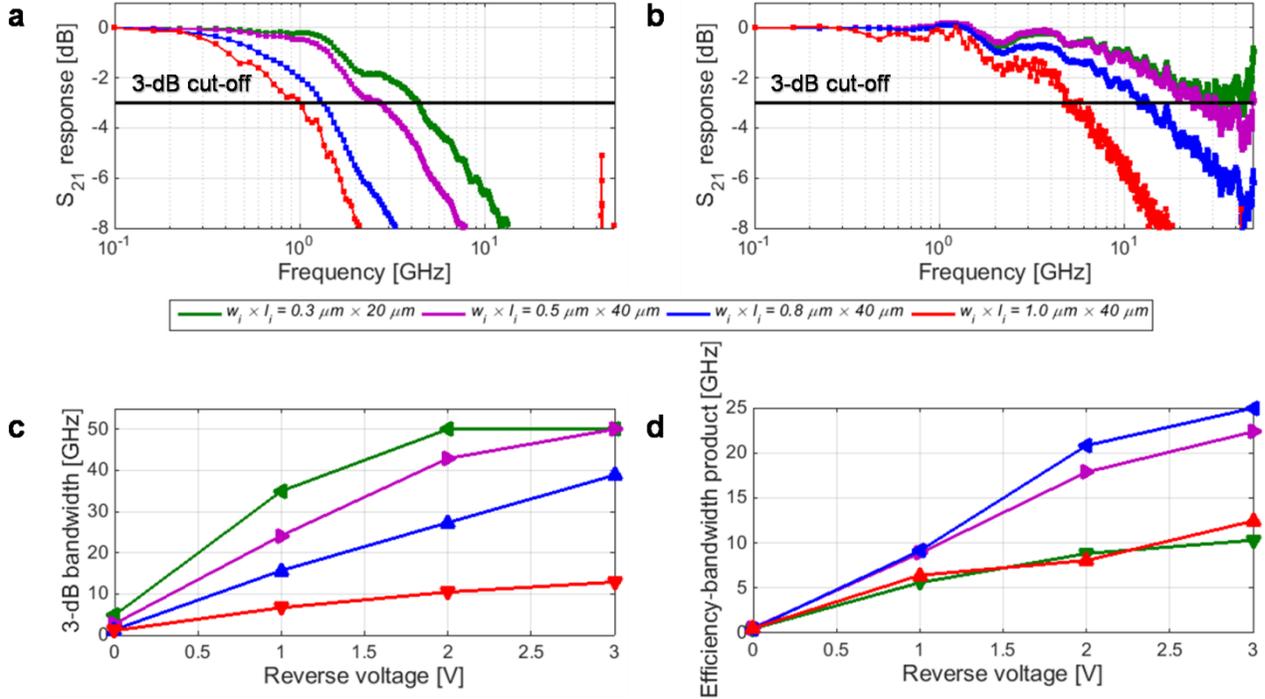


Figure 3. Normalized S_{21} parameters as a function of the radio-frequency for different Si-Ge-Si photodetector geometries and different reverse bias conditions: (a) 0 V and (b) 1 V. (c) Opto-electrical bandwidth characteristics and (d) an efficiency-bandwidth product as a function of an applied reverse bias voltage for different geometries of waveguide-coupled p-i-n photodetectors with a lateral Si-Ge-Si hetero-junction.

Figure 3(d) shows the product of quantum efficiency by the -3dB bandwidth as a function of a reverse bias for different photodetector geometries. It becomes clear that $0.3 \mu\text{m} \times 20 \mu\text{m}$ and with $1.0 \mu\text{m} \times 40 \mu\text{m}$ Si-Ge-Si photodetector geometries yield only a moderate opto-electrical performances. In the first case, the photodetector can support fast operation. However, the photo-responsivity is not high enough to be of use. In the latter case, the device may provide an outstanding responsivity, however, but the response is largely limited by the long transit time. In opposite, $0.5 \mu\text{m} \times 40 \mu\text{m}$ and $0.8 \mu\text{m} \times 40 \mu\text{m}$ devices yield the best opto-electrical performances for high bit rate applications. Both devices yield good levels of responsivities (0.44 A/W and 0.73 A/W) and fast responses with cut-off frequencies of 24 GHz and 16 GHz, respectively.

These observations and trends are further investigated through large-signal data link measurements using detailed eye diagram inspections. This study was performed on a single device featuring a $0.8 \mu\text{m}$ wide and $40 \mu\text{m}$ long intrinsic Ge region. Figure 4 shows an evolution of eye diagram apertures for various transmission bit rates ranging from 10 Gbps to 40 Gbps. The Si-Ge-Si p-i-n photodetector was biased at 1 V. The eye apertures remain clearly open for data rates up to 32 Gbps (see Figs. 4(a) to 4(e)). These results agrees well with small-signal RF measurements. At a transmission bit rate of 40 Gbps, shown in Fig. 4(f), the Si-Ge-Si p-i-n photodiode operates in a voltage-limited regime and diagram apertures starts to have a distinct eye closure. For higher voltages, for instance a 2 V bias, the cut-off frequency increases to 27 GHz. This level is high enough to yield a clear eye opening for 40 Gbps optical signal detection. These achievements are promising for an on-chip detection of high-speed signals using Si-Ge-Si photodetectors operated at low-voltages.

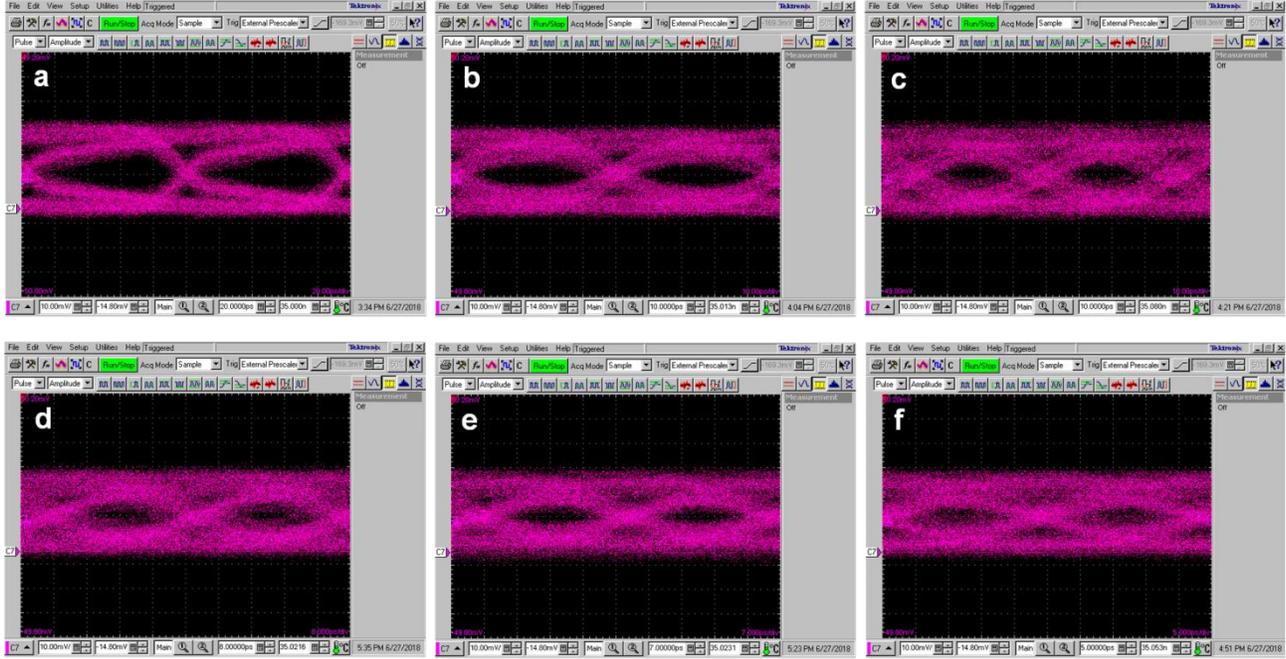


Figure 4. Evolution of eye diagram apertures of a 0.8 μm wide and 40 μm long waveguide-integrated Si-Ge-Si p-i-n photodetector. The device is biased at 1 V. Eye diagrams are inspected for different transmission bit rates: (a) 10 Gbps, (b) 20 Gbps, (c) 25 Gbps, (d) 28 Gbps, (e) 32 Gbps, and (f) 40 Gbps.

4. HIGH-BIAS AVALANCHE MODE OPERATION

Promising way of improving performances of optical photodetectors is to operate them in the avalanche regime. building on the results reported in the previous section, we used a 0.8 μm wide and 40 μm long photodetector to explore the avalanche characteristics of hetero-structured Si-Ge-Si devices.

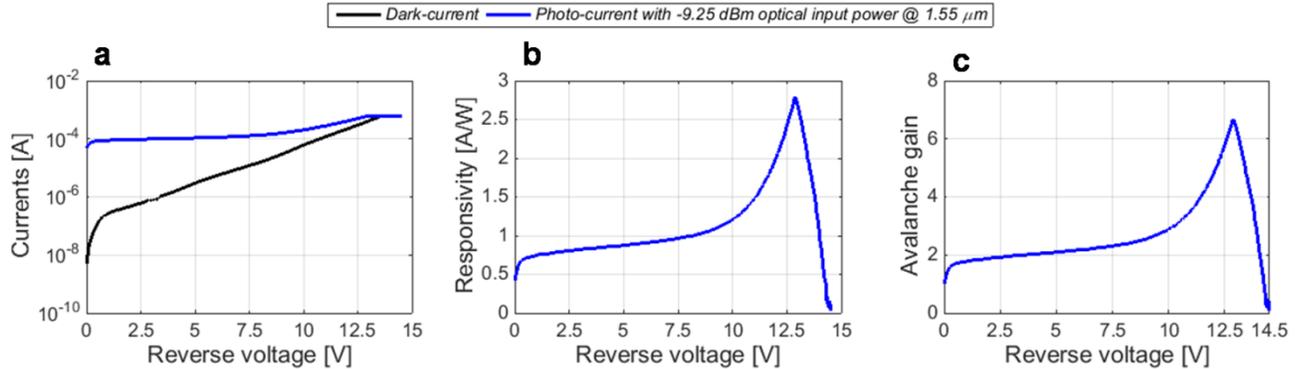


Figure 5. (a) Current-voltage, (b) responsivity-voltage, and (c) gain-voltage characteristics of a 0.8 μm wide and 40 μm long Si-Ge-Si p-i-n photodetector operated in an avalanche regime. The illumination wavelength is 1.55 μm and the optical power coupled into the device is -9.25 dBm.

Figure 5 shows current-voltage, responsivity-voltage and gain-voltage characteristics of this Si-Ge-Si p-i-n photodetector operated under avalanche regime. In particular, Fig. 5(a) shows dark- and photo-currents versus reverse bias. The dark current increase with the applied bias is typical of avalanche operation. The dark-current remains low, below 1 μA , for low-voltage operation rises up. The avalanche collapse is reached at a voltage of about 13.5 V, with a dark-current level of 600 μA . The photo-current was generated from a laser at a wavelength of 1.55 μm , with an optical input power coupled into the photodetector of -9.25 dBm. Responsivity versus reverse bias is shown in Fig. 5(b). Under low-bias regime, in particular at 0 V and 1 V, the responsivity is equal to 0.42 A/W and 0.74 A/W, respectively. This agrees well with our previous demonstrations³⁷. Then, the responsivity progressively increases, reaching a maximum of 2.79 A/W

near the avalanche breakdown point. Corresponding avalanche multiplication gain versus reverse bias is shown in Fig. 5(c). The avalanche gain is calculated as the ratio of the net-light photo-current and a net-light current at 0 V (unity gain point). The maximum multiplication gain of 6.78 is extracted from current-voltage measurements. After reaching a peak, the gain drops down sharply.

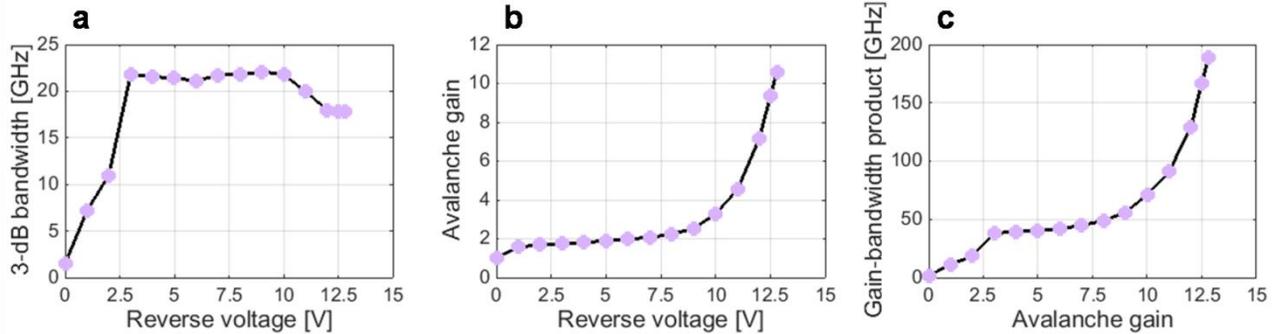


Figure 6. Opto-electrical bandwidth assessments for a Si-Ge-Si p-i-n photodetector operated under avalanche regime. (a) -3 dB bandwidth and corresponding (b) multiplication gain as a function of reverse voltage. (c) Gain-bandwidth product as a function of the avalanche multiplication gain. The tested device featured 0.8 μm wide and 40 μm long intrinsic Ge region. Testing was performed at a nominal wavelength of 1.55 μm . The optical input power was -17.5 dBm.

Figure 6 shows the opto-electrical bandwidth properties of a 0.8 μm wide and 40 μm long hetero-structured Si-Ge-Si photodetector under an avalanche operation. They were determined thanks to small-signal RF measurements at a nominal wavelength of 1.55 μm . The optical input power coupled into the p-i-n photodetector was -17.5 dBm. Figure 6(a) shows the extracted -3dB device bandwidth as a function of applied bias. The evolution of the avalanche gain is shown in Fig. 6(b). The -3dB bandwidth increases from 1.5 up to 21.8 GHz, when the bias increases from 0 V up to 3 V. Then, the -3dB bandwidth remain almost constant from 3 V up to 10 V. The generated carriers have reached their saturation velocity. In this region, the gain goes up slowly, from 1.76 up to 3.26. Beyond a 10 V bias, the -3dB bandwidth drops down, as a result of an avalanche built-up. Accordingly, the avalanche multiplication gain rises up exponentially, reaching a maximum of 10.6. A peak gain-bandwidth product of about 189 GHz is extracted.

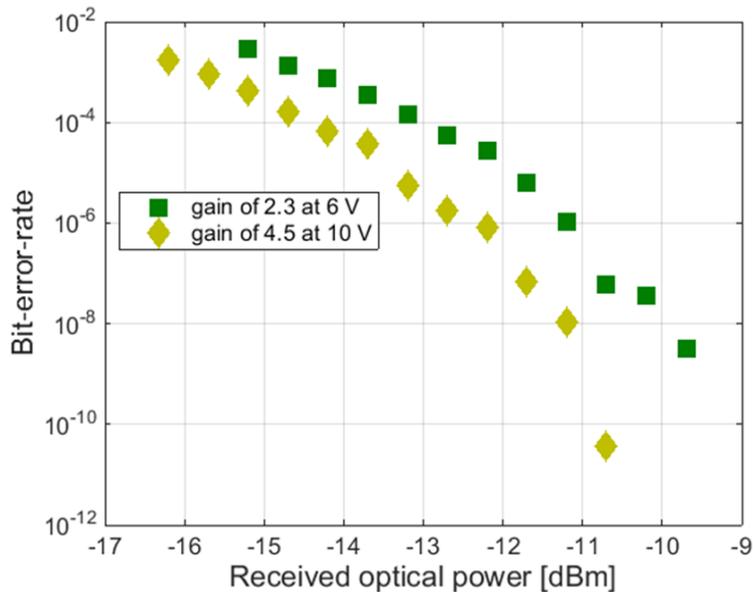


Figure 7. Bit-error-rate testing of the Si-Ge-Si p-i-n photodetector as a function of the received optical power for a transmission bit rate of 28 Gbps and different avalanche operating conditions.

The Si-Ge-Si p-i-n photodetector was also tested via large-signal data link measurements using bit-error-rate assessments. Figure 7 shows bit-error-rate (BER) as a function of the received optical power. BER acquisitions were

carried out for a transmission bit rate of 28 Gbps and different avalanche operating conditions, with reverse voltages of 6 V and 10 V, respectively. The corresponding avalanche gains are equal to 2.3 and 4.5, respectively. As a result, measured optical power sensitivities, at a BER of 10^{-9} , are equal to -9.7 dBm and -11 dBm for those bias states.

5. CONCLUSIONS

In this work, we demonstrated our recent achievements on compact optical photodetectors based on lateral Si-Ge-Si p-i-n hetero-junctions. Devices benefit from the combination of butt-waveguide coupling and lateral hetero-structured junctions, resulting in reduced fabrication complexity and improved opto-electronic performances. More specifically, we firstly report on a comprehensive study of different dimensions p-i-n photodetectors operating under low-voltages. At a 1 V reserve bias, devices exhibit dark currents of at most 150 nA and dark current densities of 0.808 A/cm^2 , responsivity (quantum efficiency) of 1.16 A/W (93%), and 3dB bandwidths beyond 50 GHz, respectively. Moreover, devices were also operated in the avalanche regime to favor enhanced signal quality for high-speed detection at the C-band wavelength of $1.55 \mu\text{m}$. For this, an error-free signal detection was achieved at a transmission bit rate of 28 Gbps, with a power sensitivity of -11 dBm for a 10^{-9} bit-error-rate. These demonstrations are promising for the potential deployment of high-speed, power-efficient, and cost-effective photodetectors in a myriad of emerging nanophotonic applications.

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