



## **Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation**

Hélène Hourdequin, Lionel Laudebat, Marie-Laure Locatelli, Pierre Bidan

### **► To cite this version:**

Hélène Hourdequin, Lionel Laudebat, Marie-Laure Locatelli, Pierre Bidan. Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation. 2016 IEEE International Conference on Dielectrics (ICD), Jul 2016, Montpellier, France. pp.999-1002, <10.1109/ICD.2016.7547786>. <hal-02537414>

**HAL Id: hal-02537414**

**<https://hal.science/hal-02537414v1>**

Submitted on 8 Apr 2020

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

# Design of Packaging Structures for High Voltage Power Electronics Devices: Electric Field Stress on Insulation

Hélène HOURDEQUIN<sup>1,2</sup>, Lionel LAUDEBAT<sup>1,2,3</sup>, Marie-Laure LOCATELLI<sup>1,2</sup>, Pierre BIDAN<sup>1,2</sup>

<sup>1</sup>Université de Toulouse ; UPS, INP ; LAPLACE (Laboratoire Plasma et Conversion d'Énergie); 118 route de Narbonne, F-31062 Toulouse cedex 9, France.

<sup>2</sup>CNRS ; LAPLACE ; F-31062 Toulouse, France.

<sup>3</sup>Institut National Universitaire Champollion; Place de Verdun 81012 Albi Cedex, France.

**Abstract**—The use of very high voltage power modules (> 10 kV) requires the implementation of appropriate structures for the device packaging. Particularly the triple point between the insulating substrate, the metallization and the encapsulation is subjected to strong electric field stress. A novel architecture is proposed for the metallized ceramic substrate. Its interest is validated by using finite element method simulations to analyze the electric field distribution inside the module. It is shown that creating a gap between the top electrodes thus forming mesa structures, enables a significant spreading of the equipotential lines. The resulting maximum electric field decreases exponentially versus the height of the mesa structure, with better results than when simply increasing the thickness of the ceramic in a conventional module structure.

**Keywords**—power module; metallized ceramic substrate; triple point; finite element method

## I. INTRODUCTION

The advent of wide bandgap semiconductor materials, such as silicon carbide (SiC), enables the development of smaller chips able to withstand much higher voltage (up to a few tens of kV) compared to the silicon chips currently available. Current very high voltage SiC demonstrators, (as bipolar diodes [1], and transistors [2],[3],[4]), enable a major evolution in the power domain and show the need to adapt the characteristics of the power modules packaging. The environment of these new components should be completely adjusted to meet the new requirements, such as high current density caused by the reduced size of the components and, consequently, the high thermal dissipation per unit area. Moreover, because of the very high switching frequency of these components, care should be taken to minimize the parasitic inductances. Finally, such high expected rating voltages requires high breakdown voltage insulating materials.

The typical structure of a 6.5 kV power module using silicon Insulated Gate Bipolar Transistors (IGBT) is shown in Fig. 1. The three main roles of the module package are to protect and insulate the semiconductor dies from their environment, allow good heat dissipation from the dies and finally, provide an electrical connection between the chips and

with external connections. Inside the module, the dies are soldered to a double side metallized ceramic substrate, which has to provide both excellent thermal conductivity and electrical insulation. The most commonly used ceramic materials are alumina ( $\text{Al}_2\text{O}_3$ ) and aluminum nitride (AlN). The metallization is typically realized by a thick copper layer, either connected to the oxide by a eutectic bonding process (Direct Bonded Copper, DBC) or by an active metal brazing process (AMB). The ceramic substrate is soldered to a base plate (ex. AlSiC), which ensures the mechanical maintaining of the assembly and the thermal transfer towards the cold source. The whole module is commonly immersed in a soft encapsulant, typically silicone gel, in order to ensure the dielectric strength along the surfaces of the substrate and between any other parts of the module subjected to high electric fields. The use of an epoxy resin can be considered in order to suppress the deformation of the power chips and of the substrate caused by the expansion and the constriction repeated during a thermal cycling [5]. Front connections are made with wire bonds or ribbons [6] to electrically connect the different chips and pads.

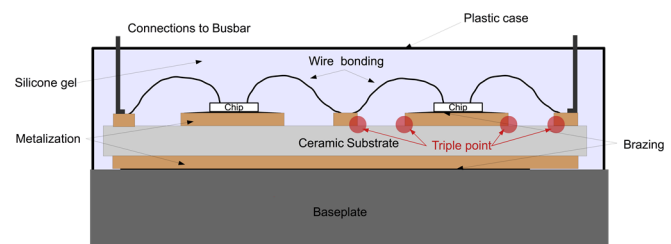


Fig. 1. Cross-section view of a power module.

This paper is focused on the ceramic substrate used in isolated power modules. The ceramics are the only electrical insulators having good enough thermal properties. The minimum thickness of this substrate is imposed by the aimed insulation voltage and depends on the dielectric strength of the material. For the high voltage power modules, AlN offers the best compromise between the thermal and electrical properties. In practice, the thickness of the AlN substrate used in the isolated modules is equal to 0.320 mm for rating voltage lower than 1.2 kV, 0.635 mm for voltages from 1.7 kV to 3.3 kV and

1 mm for 6.5 kV modules. Today the maximum thickness commercially available AlN substrate is 1 mm.

The triple point created between the metallization/substrate/encapsulation materials is one of the weakest points in a power module. This region, at the edge of the substrate metallization, is a concentration area of high electric field, as shown in red point Fig. 1, and can lead to partial discharges or even breakdown of the insulation. Several research works have been conducted on the encapsulating material in order to improve the distribution of the electric field at the triple point by the use of field-graded materials, such as resistive layer on the top of the substrate or high permittivity composites. Resistive materials in the form of silicon-based coating [7] of the substrate contribute to the spreading of the equipotential surfaces in this area and reduce the electric stress but lead also to power losses. Non-linear resistive materials including a polymer matrix filled with SiC or zinc oxide particle, allowing a high conductivity only under high electric field, is an improvement solution [8] [9]. Another path is to adjust the permittivity of the coating. The materials, made of a polymer filled with high permittivity particles, such as lead zirconate titanate (PZT) or barium titanate (BaTiO<sub>3</sub>), can also help to spread the equipotential lines, and so to increase the partial discharge inception voltage (PDIV) and breakdown voltages [10]. The results of the latter approach are significant: thanks to the use of a silicone gel filled with 15 vol.% of BaTiO<sub>3</sub> an improvement of 60% in the PDIV of encapsulated IGBT power module has been obtained compared to the unfilled one. Other technologies are investigated such as epoxy/alumina composite [11], for which the addition of nano-fillers allows to increase the dielectric breakdown strength and the partial discharge resistance of micro-filled epoxy composites.

However, change only the encapsulation material properties might not be enough for very high voltage applications. Studies of geometrical modifications of the substrate are rare and mainly focused towards the improvement of the thermal mechanical performance of the power module or the lowering of parasitic inductances. However, once a geometrical modification including a "pocket" under the ceramic substrate was proposed to address the triple point problem [12]. The simulation showed an improvement in the electrical insulation system, by reducing the intensity of the electric field at the triple point. Another proposal is to embed the metallization in the substrate [13], in order to localize the maximum field inside the substrate which electrical characteristics are much better than the dielectric silicone gel ones.

In this work, we propose an action on the substrate geometry by creating mesa structures. The goal is to evaluate and optimize the package geometry, using numerical simulation, in order to minimize the electric field stress at the triple point.

## II. PRESENTATION OF THE METHOD

The finite element method (FEM) enables to simulate the electric field distribution inside the power module in order to evaluate the effect of the material properties and of the structure's architecture. The simulations provide quantitative

results on the electric field, which enable to study different configurations of the metallized substrates that can be compared. The equations associated with the electrostatic analysis in COMSOL Multiphysics are:

$$\begin{aligned} \text{Poisson Equation} \quad \Delta V &= -\rho/\epsilon_0 \\ \vec{E} &= -\vec{\nabla}V \end{aligned}$$

In order to study the electrical insulation, the modeled structure is typically represented by the metallized substrate, the silicone gel encapsulating the entire module and copper electrodes. The structure was meshed using quadrilateral form as shown in Fig. 2, which are well adapted to the shape of the simulated structure. The meshing is thus perfectly controlled and the simulation results can be compared with each other.

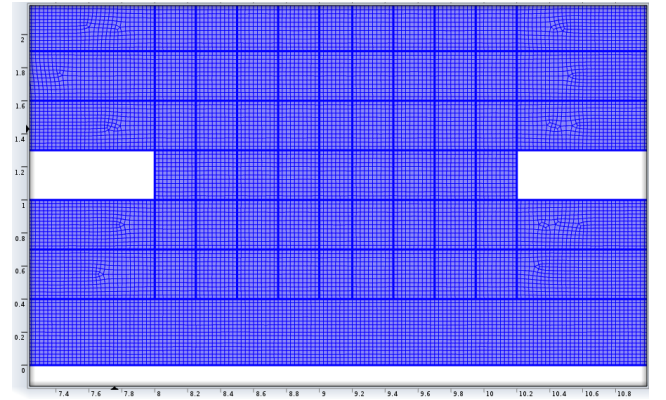


Fig. 2. Geometry and mesh used for the finite element simulations in COMSOL Multiphysics. The minimum mesh size is 0.025x0.025 mm<sup>2</sup>.

### A. Conventional structure

The proposed structure of the simulation is a typical geometry of DBC substrate, with a thickness of the ceramic layer of 1 mm. We have chosen not to represent the real profile of the etching but an academic etching profile in order to be able to generate a controlled mesh. Two electrodes are placed above the substrate, separated by a 2 mm distance, and considered as perfect conductors. Another electrode is placed below the substrate. Encapsulation is conventionally made of silicone gel. On the left electrode, an electrical potential of 15 kV is supplied (terminal) and the other electrodes are connected to the ground (Fig. 3).

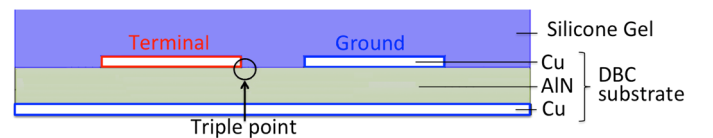


Fig. 3. Geometry for "Conventional structure" simulation.

Thereafter this structure is considered as a "reference", the simulation results after the structure modifications are compared with it.

### B. Mesa structure

The aim is to create a structure, which can improve the distribution of the electric field at the triple point. In Fig. 4 a modification in the structure, by creating a gap between the two electrodes, thus forming two mesa structures, is proposed.

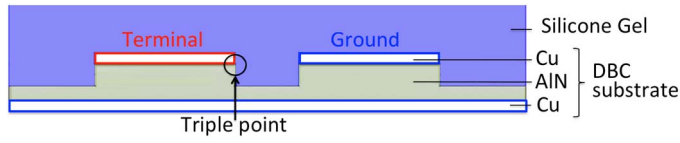


Fig. 4. Geometry for "Mesa structure" simulation.

Simulations of the electric fields and potentials are performed for this mesa structure with the same 15 kV voltage as for the conventional structure. The height of the mesa is varied, first keeping the thickness of the ceramic substrate under the top electrodes equal to 1 mm for comparison with the reference structure in Fig. 3. Then, cases with thicker ceramic substrates are considered.

### III. STUDY OF THE ELECTRIC FIELD DISTRIBUTION BY SIMULATION

Figure 5 presents the FEM simulation of the reference structure (Fig. 3) with equipotential lines and electric field intensity (the color scales are defined in the figure). The material parameters are only the absolute or relative permittivity of the ceramic and of the silicone gel, respectively equal to 9 and 2.7. The magnitude field distribution is shown (Fig. 5) exhibiting a maximum value of 154 kV/mm at the triple point in this reference case.

Considering 0.6 mm thick mesa structure (Fig.6), enables to decrease the maximum electric field down to 65 kV/mm, which means that the stress at the triple point is considerably lowered (decrease of 57% in comparison with the conventional structure in the Figure 5).

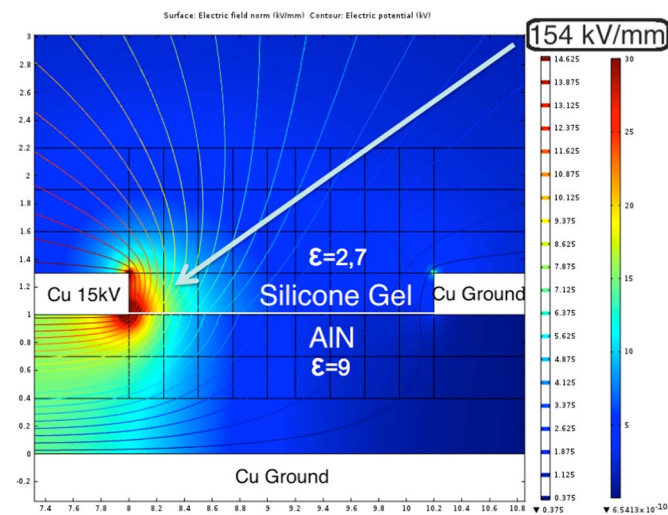


Fig. 5. Electric field distribution at the triple point in "Conventional structure".

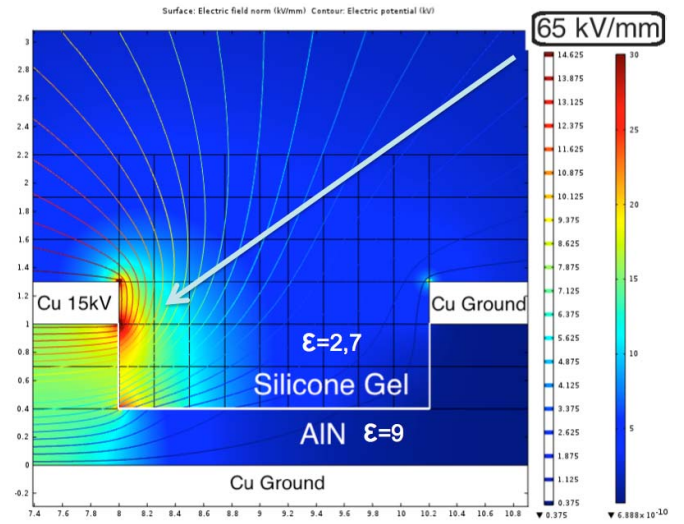


Fig. 6. Electric field distribution in a 0.6 height "Mesa structure".

Other heights of the mesas, ranging from 0 to 0.6 mm, were tested in order to evaluate the effect on the triple point for a 1 mm thick substrate. Fig. 7 (black line) shows that the relationship between the electric field at the triple point and the height of the mesas is inversely exponential. It is shown, that a significant diminution of the electric field at the triple point, by the creation of the mesa in 1 mm thick substrate, can be obtained. While almost no deterioration of the thermal resistance is induced, in comparison with the reference structure.

Nevertheless, as the electric field values for 1 mm substrate remain still high compared to current materials' dielectric strengths. The case consisting in doubling the thickness of the AlN substrate has been simulated as well (Fig. 7, red line). The same significant effect of the mesa shaping is observed. In this latter case, a further reduction of the field stress is obtained, compared to the reference structure.

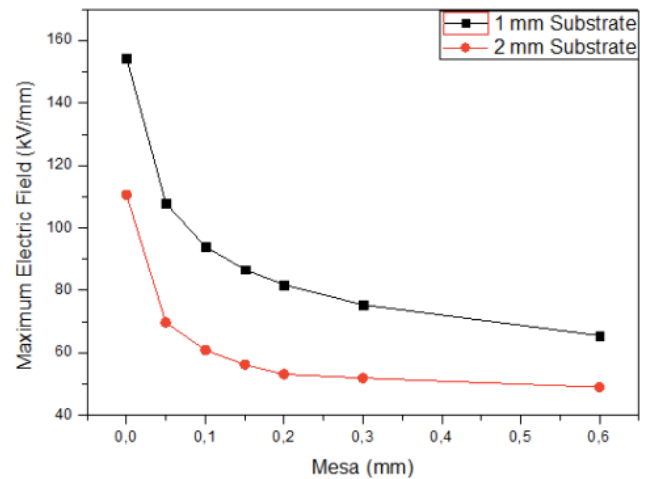


Fig. 7. Maximum electric field at the triple point as a function of the mesa structure (0, 0.1, 0.15, 0.2, 0.3, 0.6 mm).



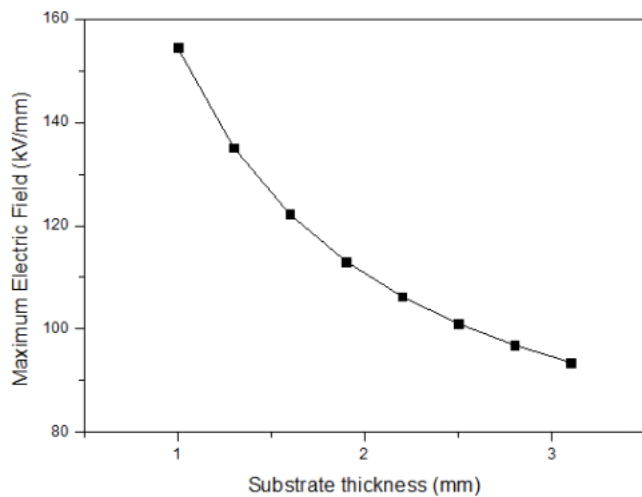


Fig. 8. Maximum electric field at the triple point as a function of substrate thickness for the conventional structure.

To prove the asset of the mesa structure, a comparison with the conventional one was made. The simulations indicate that, even by increasing the AlN substrate thickness up to 3 mm, the resulting reduction in the electric field at the triple point (presented on Fig. 8) can never be as significant as it can be for a thinner substrate (Fig. 7) with a relatively small height (0.2 or 0.3 mm) of the mesa structure.

#### IV. CONCLUSION

In this work we have investigated a new geometric structure to reduce the electric field intensity at a singular point, the triple point in the power module. By the means of the FEM analysis, we have compared conventional and mesa structures and we have obtained a significant improvement.

The electric field intensity in the conventional structure could be reasonably reduced with a thickness of ceramic being at least tripled. The mesa structure is expected to allow a better trade-off between electrical and thermal performance. Such a mesa structure could be implemented either by CO<sub>2</sub> laser etching or by machinability. Thus, experimental tests will be carried out to validate the mesa structure. Moreover, the substrate structure proposed here offers perspectives to be combined with other technologies, such as employing innovative encapsulating materials, in order to cumulate their beneficial effects on the triple point stress.

#### REFERENCES

- [1] T. Kimoto, K. Kawahara, H. Niwa, N. Kaji, J. Suda, « Ion Implantation Technology in SiC for Power Device Applications », Junction Technology (IWJT), International Workshop on, 2014
- [2] Ryu, S. B., Capell, C., Jonas, C., Lemma, Y., O'Loughlin, M., Clayton, J., et al. (2013). « Ultra high voltage IGBTs in 4H-SiC » (pp. 36–39). Presented at the Wide Bandgap Power Devices and Applications (WiPDA), 2013 IEEE Workshop on IS - SN - VO - VL -, IEEE. <http://doi.org/10.1109/WiPDA.2013.6695557>
- [3] Madhusoodhanan, S., Hatua, K., Bhattacharya, S., Leslie, S., Ryu, S.-H., Das, M., et al. (n.d.). « Comparison study of 12kV n-type SiC IGBT with 10kV SiC MOSFET and 6.5kV Si IGBT based on 3L-NPC VSC applications » (pp. 310–317). Presented at the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), IEEE. <http://doi.org/10.1109/ECCE.2012.6342807>
- [4] Miyake, H., Okuda, T., Niwa, H., Kimoto, T., & Suda, J. (2012). « 21-kV SiC BJTs With Space-Modulated Junction Termination Extension ». *IEEE Electron Device Letters*, 33(11), 1598–1600. <http://doi.org/10.1109/LED.2012.2215004>
- [5] Masafumi Horio, Yuji Iizuka, Yoshinari Ikeda, « Packaging Technologies for SiC Power Modules », FUJI ELECTRIC REVIEW, vol.58, no.2, pp.75,78, May 2012
- [6] L. Ménager, B. Allard, V. Bley, « Conditionnement des modules de puissance », article Techniques de l'Ingénieur, 2010
- [7] G. Mitic, T. Licht, G. Lefranc, « IGBT Module Technology with High Partial Discharge Resistance », Industry Applications Conference, Thirty-sixth IAS Annual Meeting, vol.3, pp.1899,1904, 2001
- [8] C. Duchesne, Contribution à l'étude de la gradation de potentiel dans les modules de puissance haute tension, PhD Thesis, Université Paul Sabatier, Toulouse, 2009
- [9] L. Donzel, J. Schuderer, « Nonlinear resistive electric field control for power electronic modules », Dielectrics and Electrical Insulation, IEEE Transactions on, vol.19, no.3, pp.955,959, June 2012
- [10] Ningyan Wang, I. Cotton, J. Robertson, S. Follmann, K. Evans, D. Newcombe, « Partial discharge control in a power electronic module using high permittivity non-linear dielectrics », Dielectrics and Electrical Insulation, IEEE Transactions on, vol.17, no.4, pp.1319,1326, August. 2010
- [11] Z. Li, K. Okamoto, Y. Ohki, T. Tanaka, « The Role of Nano and Micro Particles on Partial Discharge and Breakdown Strength in Epoxy Composites », Dielectrics and Electrical Insulation, IEEE Transactions on, vol.18, no.3, pp.675,681, 2011
- [12] C. Wesley Tipton, D. Ibitayo, D. Urciuoli, G. K. Ovrebø, « Development of a 15kV Bridge Rectifier Module Using 4H-SiC Junction-barrier Schottky Diodes », Dielectrics and Electrical Insulation, IEEE Transactions on, vol.18, no.4, pp.1137,1142, August 2011
- [13] D.Frey, J. L. Schanen, J. L. Auge, O. Lesaint, « Electric field investigation in high voltage power modules using finite element simulations and partial discharge measurements », Industry Applications Conference, Thirty-eighth IAS Annual Meeting, vol.2, pp.1000,1005, 2003