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# Shunt Regulator for the Serial Powering of the ATLAS CMOS Pixel Detector Modules

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**Abstract**— A shunt regulator was designed to meet the specifications for the serial powering of the CMOS pixel detector modules in compatibility with the next upgrade of the ATLAS detector. Serial powering greatly increases the system's power efficiency when compared to a parallel powering scheme and allows for significant material budget savings in the power cabling. In such a scheme, each pixel detector chip is powered by a shunt regulator that takes in a constant current and produces a regulated output voltage relative to the module's potential ground. The proposed regulator has a modular structure. Each regulator module consists of a shunt regulation submodule followed by a low drop-out voltage regulation submodule, and is designed to deliver a nominal output current of 10 mA. The regulator module's schematic is presented along with a theoretical study and stability analysis. A test chip was designed in CMOS 0.18  $\mu\text{m}$  technology containing one main shunt regulator composed of 126 modules, as well as two separate regulators each composed of one single module. The characterization measurements show a correct DC startup for various load conditions, as expected by simulations. The output voltage of a single module is regulated with a precision  $< 1\%$ . Moreover, the regulator module works with a low voltage drop-out of 200 mV for a large range of input current from 3 mA to 18 mA. The equivalent series resistance of a 40-module regulator is measured to be 15 m $\Omega$ , including the wire bonding and test bench parasitics. The test chip is successfully tested in serial mode and in parallel mode. In the latter mode, the current mismatch between parallel chips is measured to be less than 3.4% for an input current of 1 A. Moreover, transient measurements performed with an active load show a proper functioning with no undershoots or overshoots. Finally, the test chip was irradiated with an X-ray source up to 125 Mrad. Measurements show a stable response of the regulator with an intrinsic output voltage variation less than 1%.

**Index Terms**—ATLAS, CMOS pixel module, serial powering, shunt regulator

## I. INTRODUCTION

ATLAS Inner Tracker (ITk) is scheduled for upgrade to cope with the High Luminosity Large Hadron Collider (HL-LHC) operating in 2026 [1]. One motivation is to increase power efficiency and decrease material budget in pixel detector modules, which adopt a parallel powering scheme today as described in Fig. 1(a). In such a scheme, high current densities circulate in long cables up to 100 m with a limited cross section leading to significant power losses. In the present pixel detector, the power efficiency is around 20% [2].

To resolve this problem, serial powering has been proposed as shown in Fig. 1(b). In a serial powering scheme, a relatively small current flows through the cables, and through the modules

connected in series. This current corresponds to one module consumption plus some headroom for proper operation. If the total current is reduced by a factor  $N$ , the power losses due to cable resistance will decrease by  $N^2$ . Such increase in efficiency allows the reduction of cables volume, reducing thus the material budget.

In order to benefit from serial powering, the module electronics need to be adapted accordingly, as they are designed to work under a constant voltage and not under a constant current. The proposed solution consists in adding shunt regulators in each pixel detector chip, which takes in a constant current, and produces a regulated output voltage with respect to the module's ground.

The serial powering solution has been investigated in previous front end chips FE-I3 [3] and FE-I4 [4] designed for ATLAS. Nevertheless, it has been decided to adopt a classical parallel powering approach for the first IBL upgrade [5]. Today, the serial powering scheme is chosen as the baseline for the next ITk upgrade. Consequently, the shunt regulator concept previously developed [6] is adapted to match the specifications for the hybrid pixel modules designed by the RD53 collaboration [7].

Alternatively, monolithic CMOS pixel modules [8] [9] constitute a high potential technology for future applications. In a monolithic module, the sensor is implemented in the same substrate as the readout electronics, reducing thus the time and cost of modules production when compared to hybrid modules. This solution still needs to be fully compatible with the serial powering system.

In this paper, a novel shunt regulator circuit is proposed to be integrated in the CMOS pixel modules. In the next section, shunt regulator architecture will be described followed by a stability analysis. In section III, the test chip architecture will be illustrated with emphasis on power management. Finally, characterization measurements will be presented along with irradiation test results.

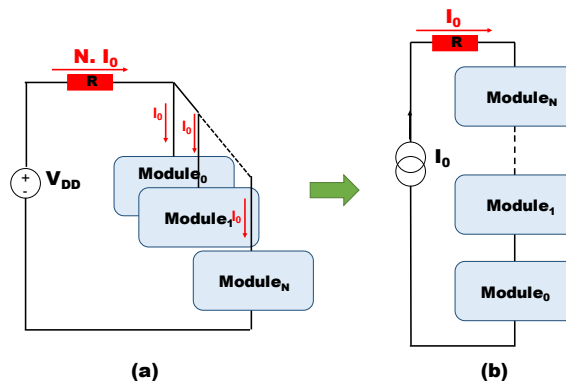


Fig. 1. Parallel powering scheme (a) versus serial powering scheme (b)

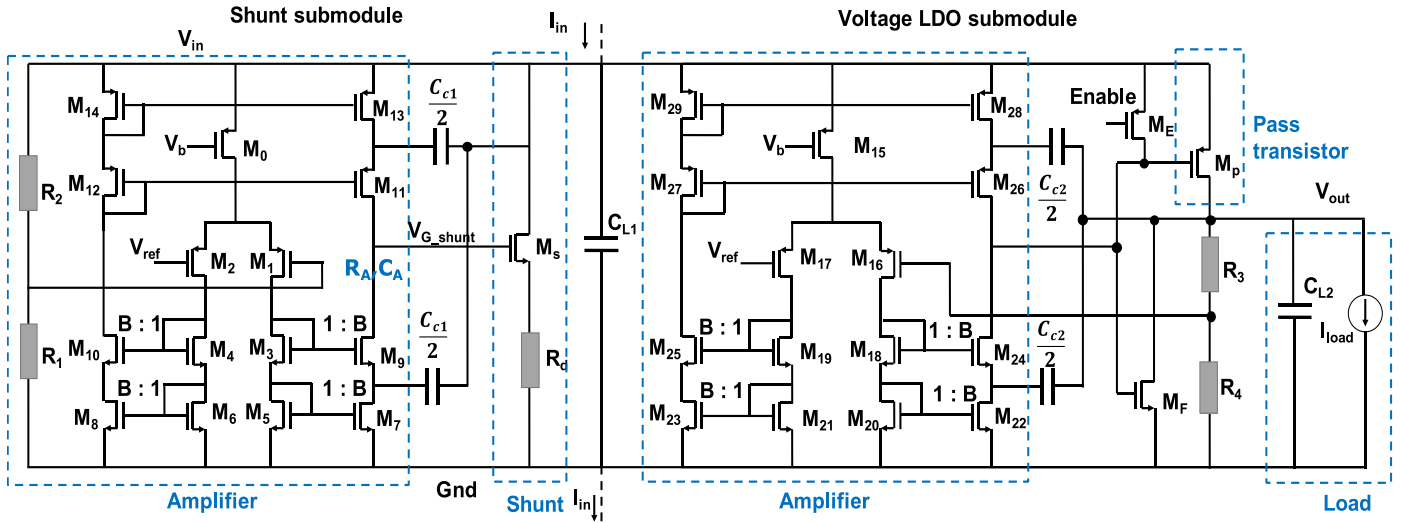


Fig. 2. Shunt regulator module architecture

## II. SHUNT REGULATOR ARCHITECTURE

The shunt regulator has a modular structure. Each module consists of two submodules: a shunt submodule and a voltage low-dropout (VLDO) submodule as shown in Fig. 2. The shunt submodule is composed of an amplifier controlling the gate voltage of a shunt transistor  $M_S$ . The amplifier compares a fraction of the input voltage  $V_{in}$  to a reference voltage  $V_{ref}$  generated by a bandgap circuit and controls the shunt transistor  $M_S$  in order to stabilize the input voltage at a value  $V_{in} = V_{ref}/\alpha_1$ , where  $\alpha_1$  is the resistive ratio  $R_1/(R_1+R_2)$ . Accordingly,  $M_S$  is controlled to shunt the fraction of input current that is not consumed by the load.

The voltage LDO submodule performs a second round of regulation, where its amplifier senses the input voltage  $V_{in}$ , and controls a pass transistor  $M_P$  in order to keep the output voltage regulated at  $V_{out} = V_{ref}/\alpha_2$ , where  $\alpha_2$  is the resistive ratio  $R_4/(R_3+R_4)$ . This regulation requires a certain voltage drop across  $M_P$  that should be kept to a minimum value, around 200 mV.

Combining the shunt and VLDO submodules, the output voltage is regulated two times providing thus a good noise immunity. Circuit stability is, however, crucial for proper operation. The circuit in Fig. 2 can be studied as two independent feedback regulation loops, one constituted by the shunt submodule and the other constituted by the VLDO submodule. In fact, the two loops have the same transfer function; they are both composed of a differential amplifier controlling the gate of a transistor in common source configuration. That said, the position of the poles and zeroes are different in each loop. One particular problem is that the output impedance of the VLDO can become very high in some load conditions. This problem will be addressed further in the article. This section will focus on the transfer function of the shunt submodule.

The shunt regulation loop consists of two low frequency poles (or zeros depending on the studied transfer function), one at the amplifier output and the other at the regulator output. A compensation is thus needed to stabilize the circuit. Most regulators use an off-chip capacitor for stability and noise filtering [10]. Other work proposes a fully on-chip solution [11], however, there is an upper limit on the load capacitance beyond

which the system becomes unstable. In the present work, the compensation is mainly performed by two capacitors connected between  $V_{in}$  and the sources of cascode transistor  $M_9$  and  $M_{11}$  as it is classically done in operational amplifiers. This compensation technique guarantees a low impedance feedback path for the current at high frequencies. For symmetry, both capacitors have the same value  $C_{c1}/2$ . The closed loop behavior of the circuit can be modeled, with some approximation, as a second order system:

$$\frac{V_{out}}{I_{load}} = -R_0 \frac{\left[1 + \frac{s}{z_1}\right]}{1 + 2\zeta \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \quad (1)$$

Where  $R_0$  is the equivalent series resistance:

$$R_0 = \frac{1}{\alpha_1 g_{m_s} B g_{m_1} R_A} \quad (2)$$

And where  $g_{m_s}$  is the effective transconductance of  $M_S$  taking into account the degeneration by  $R_d$ ,  $B$  is the mirroring ratio between the first and second stage of the amplifier, and  $g_{m_1}$  denotes the transconductance of  $M_1$  which is equivalent to that of  $M_2$ , and  $R_A$  is the output resistance of the amplifier. The Zero ' $z_1$ ' is expressed as:

$$z_1 = \frac{1}{R_A C_A} \quad (3)$$

$C_A$  being the total capacitance at the output node of the amplifier. For a load capacitance  $C_L$ , the natural frequency  $\omega_0$  is written as:

$$\omega_0 = \sqrt{\frac{\alpha_1 g_{m_s} B g_{m_1}}{C_A(C_{L1} + C_{c1})}} \quad (4)$$

While the expression for the damping factor  $\zeta$  is:

$$\zeta = \frac{C_{c1} g_{m_s} R_A + C_{L1}}{2 R_A} \sqrt{\frac{1}{\alpha_1 g_{m_s} B g_{m_1} C_A(C_{L1} + C_{c1})}} \quad (5)$$

According to control theory, the damping factor must be greater than zero in all cases for the system to be stable. Therefore, the expression (5) must be strictly positive. In the absence of load capacitor, the damping factor has the following form:

$$\zeta \approx \frac{1}{2} \sqrt{\frac{C_{c1} g m_s}{\alpha_1 B g m_1 C_A}} \quad (6)$$

This expression can be designed to have a positive value by choosing an appropriate  $C_{c1}$ . If the load capacitor is sufficiently large, that is  $C_{L1} \gg C_{c1} g m_s R_A$ , then the damping factor takes the following form:

$$\zeta \approx \frac{1}{2 R_A} \sqrt{\frac{C_{L1}}{\alpha_1 g m_s B g m_1 C_A}} \quad (7)$$

In that case, the damping factor increases linearly with  $\sqrt{C_{L1}}$ . By studying the derivative of equation (5), it can be proved that the function has one global minimum at  $C_{L1} = C_{L,critical} = C_{c1} g m_s R_A$ , where the minimum damping factor is:

$$\zeta_{min} = \sqrt{\frac{C_{c1}}{\alpha_1 B g m_1 R_A C_A}} \quad (8)$$

By choosing  $C_{c1}$  as to set  $\zeta_{min} > 0$ , one can guarantee the stability for all values of  $C_L$ , as shown in in Fig. 3.

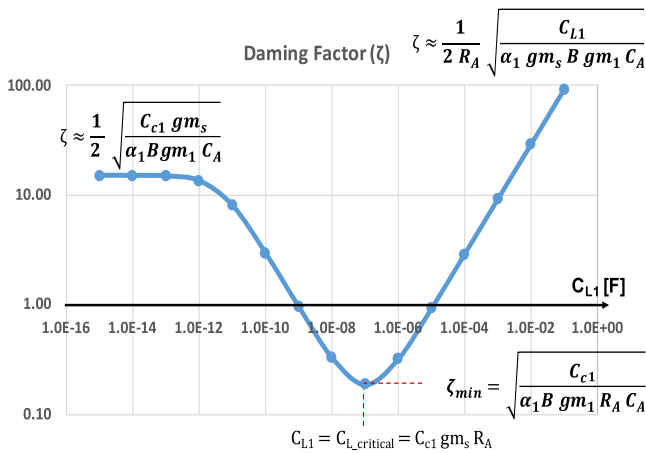


Fig. 3. Damping factor as a function of the load capacitor

Finally, the phase margin can be calculated directly from the damping factor [12]:

$$\phi_M = \tan^{-1} \frac{2}{\left[ \left( 4 + 1/\zeta^4 \right)^{1/2} - 2 \right]^{1/2}} \quad (9)$$

Fig. 4 shows a simulation where a current pulse of 1 mA is drawn as a load current, for three different values of  $C_{L1}$ . For  $C_{L1} = 0$ , the system is stable with a damping factor of 15, but the transient regulation is relatively poor. If  $C_{L1}$  is at its critical value  $C_{L,critical} = C_{C1}$  ( $= 100$  nF in that case) the system exhibits some damped oscillations with a damping factor of 0.2. If  $C_{L1}$  has a relatively large value of  $10$   $\mu$ F, the system is stable with a damping factor of 0.9. In that case, the system response approaches a first order system with good regulation and transient response. For that reason, it was chosen to operate the circuit in that last mode; with on-chip compensation capacitors and an off-chip load capacitor. It is worth noting that the circuit would probably be stable with such a large value of  $C_{L1}$  even without compensation. However, the present calculations did not take into consideration wire bonding parasitics which could affect the circuit stability by introducing a

high impedance in series with  $C_{L1}$ . Therefore, the used compensation guarantees stability, even in the absence of a load capacitor, which gives robustness to the design.

A single shunt module is designed to deliver an output current of 10 mA. To build a bigger regulator, as many modules as needed are connected in parallel to deliver the required output current. The concept works well in case all the modules are identical. However, mismatches are to be expected within the modules of the same chip, as well as between different chips. In that case, the current may not be evenly distributed between parallel regulators. To compensate for this problem, as many signals as possible are put in common between parallel modules; that is  $V_{in}$ ,  $V_{ref}$  and  $V_{G,shunt}$ . By connecting  $V_{ref}$  in common, any bandgap voltage offset is corrected and by connecting  $V_{G,shunt}$  in common, the amplifier offset is corrected. There will still be the shunt transistor offset. For that matter, the shunt transistor  $M_s$  is operated in strong inversion which decreases the transconductance of  $M_s$  when compared to the weak inversion mode. Current mismatch due to threshold voltage offset is thus reduced. Moreover, a degeneration resistance  $R_d$  is added to the source of  $M_s$  which acts negative local feedback. Any increase of current in one regulator will be counter-balanced by the increase of the source potential of  $M_s$  due to  $R_d$ . Furthermore,  $R_d$  is implemented as many resistances in parallel with a careful layout in order to minimize the mismatch. Another advantage of  $R_d$  is the reduction of the drain – source voltage of  $M_s$  to be compliant with technology's specifications.

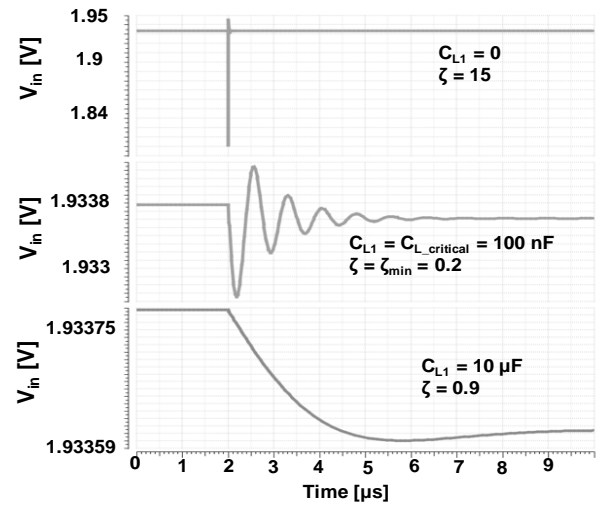


Fig. 4. Input voltage response to a step excitation of 1 mA load current.

As mentioned earlier, the VLDO submodule has the same transfer function as the shunt submodule therefore it can follow the same stability study approach. It is worth noting however that the VLDO's output impedance may become very high if the load current is low or absent. This could make the compensation very difficult, as  $g m_s$  approaches zero. To get around this problem, a fictive load current  $I_F$  is created via transistor  $M_F$ . This transistor guarantees that there is always a minimum current flowing through the pass transistor  $M_P$ . As for high load currents,  $M_F$  will be automatically switched off and will not cost the circuit any additional power. With such a configuration, a reasonable value of  $C_{C2}$  is calculated to stabilize the circuit for all values of  $C_{L2}$ . For best performance, a  $C_{L2}$  of  $10$   $\mu$ F is chosen. Furthermore, an enable transistor  $M_E$  is added giving the possibility to cut off the current from the load. This option ensures proper startup in case of an unknown load behavior.

III. TEST CHIP ARCHITECTURE

A test chip was designed and fabricated in a TowerJazz 0.18  $\mu\text{m}$  CMOS technology. The standard epitaxial process has been modified as described in [13] to increase pixel performance and radiation tolerance. The chip has a total dimension of 3.97 mm  $\times$  1.88 mm as illustrated in Fig. 5. The shunt regulator is designed to power a monolithic CMOS pixel chip that requires a total current up to 1.26 A. Therefore, the regulator consists of 126 elementary modules, divided into four domains. Domains separation means that while all the shunt submodules are in parallel, the VLDO submodules are connected commonly only within the same domain. This allows for better noise immunity and reduces noise coupling between different domains.

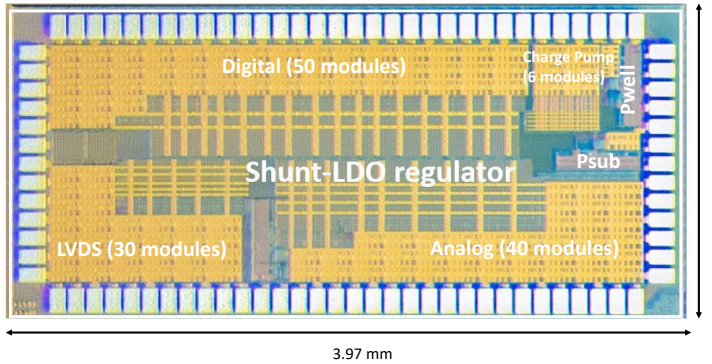


Fig. 5. Microscope photo of the shunt regulator test chip

The four domains are: the ‘Digital Domain’ (50 modules) the ‘Analog Domain’ (40 modules), the ‘LVDS Domain’ (30 modules), and the ‘Charge Pump Domain’ (6 modules). These domains together form what is called the ‘Main Domain’ and they have one common bandgap that provides the reference potential. The center of the test chip is filled with decoupling capacitors.

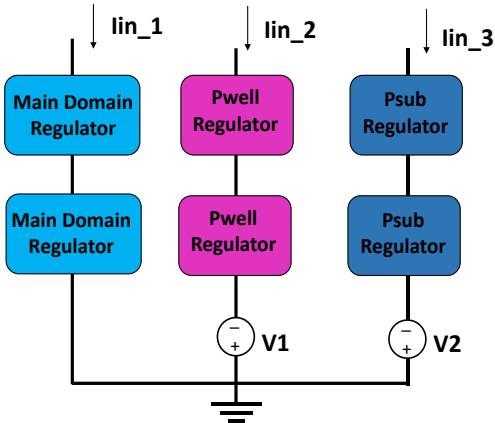


Fig. 6. Illustration of the concept of the sensor bias in a serially powered system

On the right side of the chip, two independent regulators, namely Pwell and Psub, are implemented each with its own bandgap circuit, and each consisting of only one regulator module. These regulators are designed to polarize the Pwell and Psubstrate of the CMOS pixels, to address a sensor bias problem in the serial powering scheme. The Pwell and the Psubstrate constitute the anode of the pixel sensing diode, and they must be kept at a constant potential with respect to the module’s ground potential. Such a problem does not exist in a parallel powering scheme as a fixed voltage source can be used for all anodes, as all modules share the same ground potential. This constant polarization

solution is not adapted to a serially powered system, as each module has its own relative ground potential, and therefore a different potential difference will be applied to each sensor, depending on its location in the serial chain. In the case of hybrid pixel modules, a fixed polarization solution is tolerated as the sensor bias can be as high as several hundreds of volts. In that case, a ground potential shift by a few volts will constitute a relatively small difference in the sensor bias. However, in the case of a monolithic CMOS pixel modules, this solution is not tolerated as the sensor bias can be as low as a few volts, which needs to be kept constant for all modules. Therefore, an adapted solution is needed to produce a sensor bias that shifts with the module’s relative ground.

The proposed solution is to shift the ground potentials of the Pwell and Psub regulators with respect to the Main Domain regulator using two negative voltage sources ‘V1’ and ‘V2’ as shown in Fig. 6. In that case, the output of each Pwell and Psub regulator is shifted by a value of V1 and V2 respectively, with respect to the module’s ground potential. Consequently, the sensor bias remains constant for all serially powered modules.

IV. CHARACTERIZATION RESULTS

A. Measurements on a single module

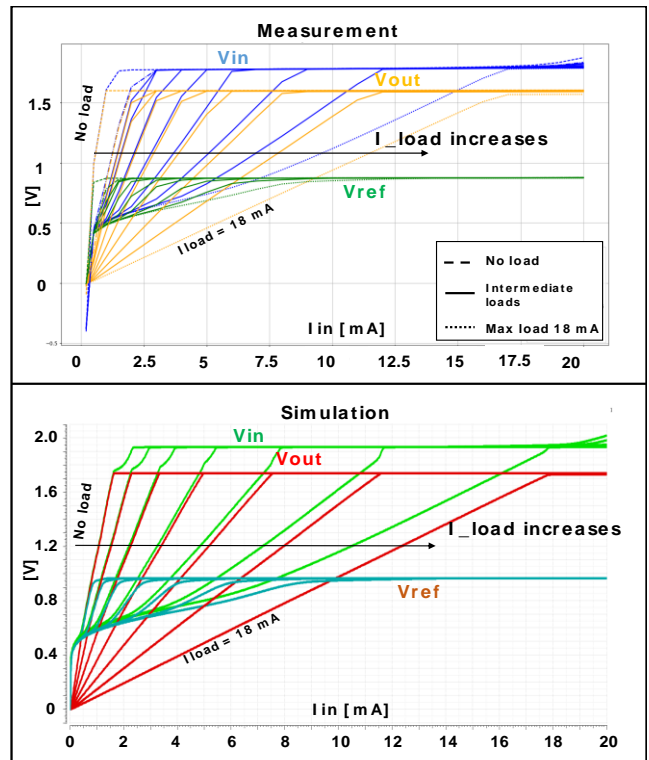


Fig. 7. DC startup measurement (top) and simulation (bottom) of one regulator module for various load conditions

First, a single module was tested independently by testing the Pwell and the Psub regulators as they are identical in structure. The DC input current was swept between 0 and 20 mA. This measurement was done in several load conditions going from no load up to  $I_{load} = 18$  mA by connecting the output with variable resistors (passive load). The measurements and simulations are shown in Fig. 7. The measurements agree well with the simulation, with the exception that the bandgap value is different. Various measurement on different bandgaps of different chips showed that

the reference voltage  $V_{ref}$  measurements are consistent among themselves with a mean value of 870 mV, which is less by around 100 mV than the simulated value. This offset can be easily corrected in future submissions.

The nominal operation current for one module is 10 mA, but it can operate efficiently for a large range of input currents between 3 mA and 18 mA with a constant voltage drop of 200 mV between  $V_{in}$  and  $V_{out}$ . Therefore, the module's consumption can be easily adapted to the load. To measure the regulation, the input current was fixed to  $I_{in} = 12$  mA, and the output voltage was measured for variable load currents up to 10.6 mA. The measurement results, shown in Fig. 8 indicate that the output voltage is stable with respect to the input current, with a relatively small variation of 14 mV which represents 0.9% of the DC value. This regulation corresponds to an equivalent series resistance of 1.32  $\Omega$ . In simulations, the series resistance of one module  $R_0$  is in a range between 81 m $\Omega$  and 281 m $\Omega$  depending on the load current. The measured difference could be attributed to wire bonding resistance and other parasitic resistances coming from the board and the test setup. A single wire bond resistance is estimated to be 200 m $\Omega$ , therefore it is difficult to measure the intrinsic series resistance of the regulator with a good accuracy.

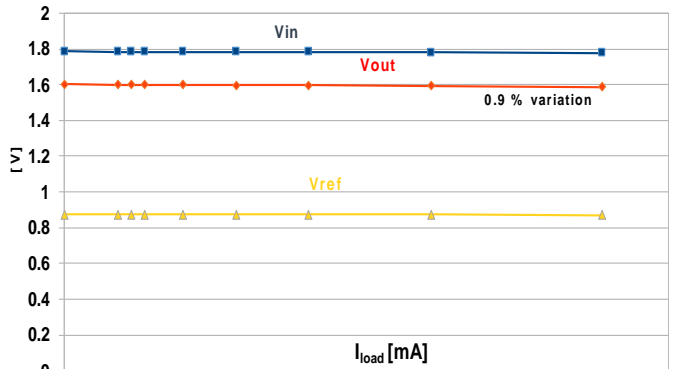


Fig. 8. Measured voltages as a function of load current for one module

**B. Measurement on the Main Domain**

The first Main Domain tests showed unexpected behavior at high current levels. Investigation with a thermal camera showed that there was an overheat problem due to the used setup; the chip

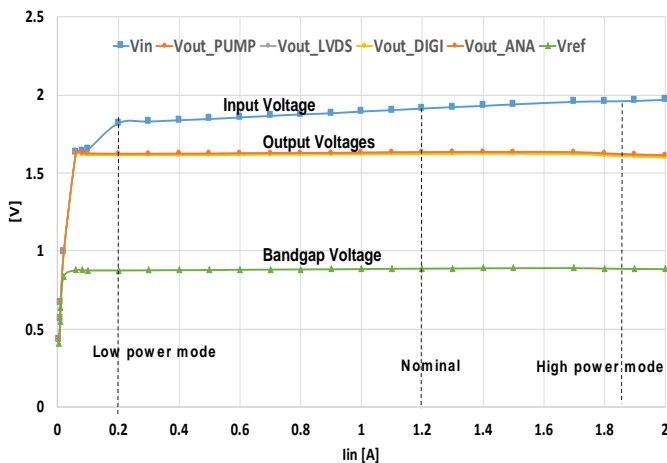


Fig. 9. DC startup of the Main Domain regulator

temperatures exceeds 230 °C at  $I_{in} = 2$  A without cooling. Indeed, at this level of input current, the power density is 54 W/cm<sup>2</sup>, which largely exceeds the specifications for the ATLAS ITk modules of 0.7 W/cm<sup>2</sup>. This high-power density is mainly due to the fact that all of the regulator modules are placed in a relatively small area; that of the test chip. When the regulator will be implemented in a full-size CMOS chip of approximately 2 cm × 2 cm, the regulator modules should be distributed alongside the periphery to reduce the power density. In addition, this strategy allows better supply distribution with less voltage drops with respect to the solution where only one full sized regulator is placed in the periphery. It is also worth mentioning that the case where the regulator shunts the entire input current is a rare case, as most of the power should be dissipated in the pixel matrix. It is however a case to be foreseen and must be addressed in the final chip. For test purposes, the chip was cooled with a cooling spray to perform the DC tests at high currents. Other tests were performed at relatively low currents to avoid chip damage. A new test setup is being prepared to allow cooling with a Peltier device.

DC startup of the Main Domain is shown in Fig. 9. The test shows that the Main Domain can operate properly with an input current ranging from 0.2 A to 2 A, with a low drop-out. The regulator performs as expected by simulation with the exception that the input voltage increases linearly with the input current with a slope corresponding to a parasitic resistance of 82 m $\Omega$ .

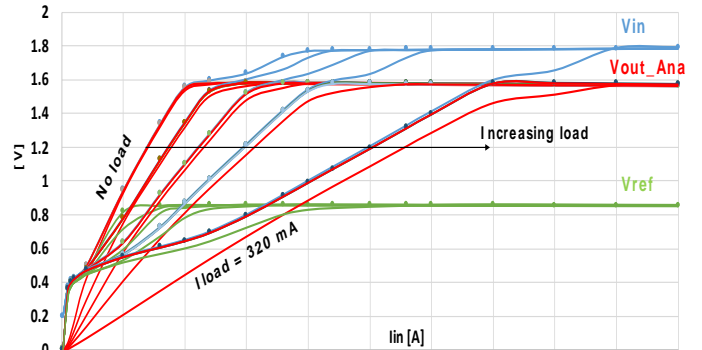


Fig. 10. DC startup of Main Domain regulator with various load currents

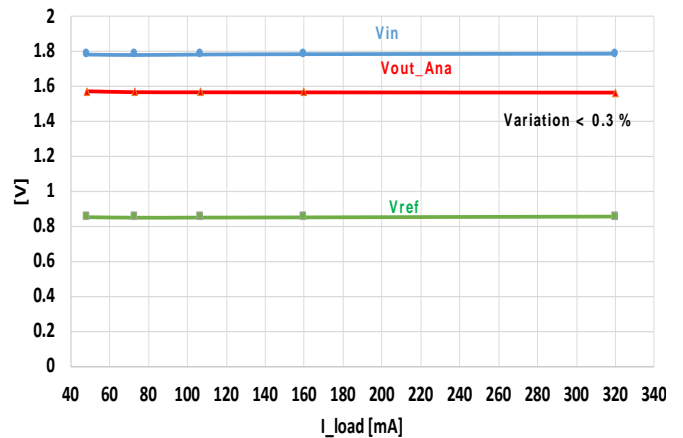


Fig. 11. DC regulation of the Analog Domain regulator

The chip startup was also tested successfully with various load currents as shown in Fig. 10. In this test the load was applied to the output of the Analog Domain regulator ‘Vout\_ANA’. Fig. 11 shows the regulation performance when applying a load current

up to 320 mA, knowing that the total input current is 450 mA. The output voltage is measured to be stable with a variation of 4 mV, corresponding to less than 0.3% variation of the output DC value. The output slope corresponds to a series resistance  $R_{0\_ANA} = 15 \text{ m}\Omega$ . In fact, when combining  $N$  regulator modules in parallel, their total series resistance  $R_{tot}$  is equivalent to  $R_0/N$ ,  $R_0$  being the single module's series resistance equivalent to 100 m $\Omega$ . Given the very low series resistance of the Analog Domain regulator ( $N = 40$ ), the measurement is once again limited by the setup parasitic resistances. It is worth mentioning that multiple input and output pads were used for the Main Domain (80 pads in total) in order to reduce resistive as well as inductive parasitics.

### C. Serial powering

Two test boards were powered serially with an input current up to 500 mA. The voltages were measured with respect to the absolute ground, i. e. the ground of the second test board B2 as shown in Fig. 12. The measurements show that the two test boards start up correctly, as expected by simulations.

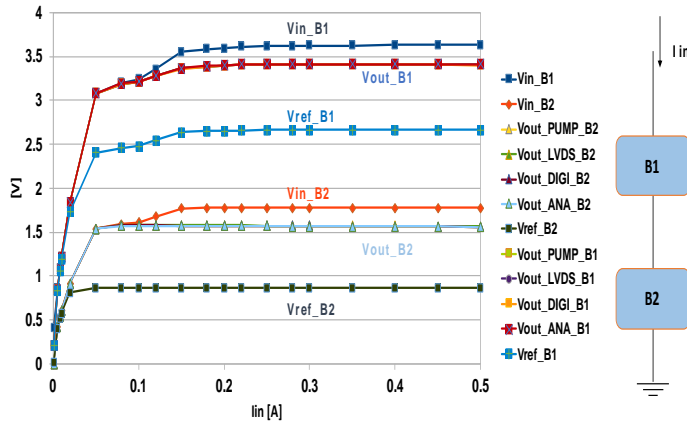


Fig. 12. Serial powering of two test boards

### D. Parallel powering

In a serially powered chain, if one element fails, the functionality of the whole chain is at risk. Therefore, in ATLAS Inner Tracker, it has been decided that each pixel detector module must contain four CMOS chips in parallel, each having its own shunt regulator. This ensures that if a chip fails, the other three chips should remain functional and relay the current to the next module. This significantly reduces the system failure risk. The technical difficulty of this solution is to guarantee the even distribution of input current between the four parallel shunt regulators.

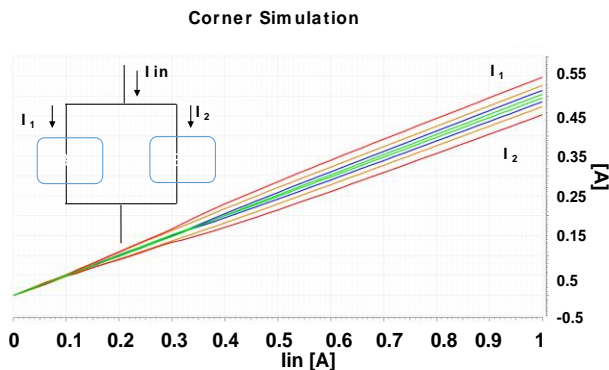


Fig. 13. Corner simulation of two regulators in parallel

As discussed in section II, some design measures have been adopted to reduce mismatch effects between parallel regulator modules. Corner simulations predicted a current mismatch within  $\pm 10\%$  for an input current of 1 A distributed between 2 parallel Main Domain regulators as shown Fig. 13. In order to confirm simulation predictions, characterization measurements were performed in a parallel powering scheme. Two boards were powered with the same current source, and the current in each circuit branch was measured using two similar ammeters. 'V<sub>ref</sub>' and 'V<sub>G\_shunt</sub>' signals were put in common as previously described in Section II. Measurements for parallel powering of two test boards named B1 and B2, consuming currents  $I_{B1}$  and  $I_{B2}$  respectively, are shown in Fig. 14. These measurements indicate a proper startup and an even distribution of current between the two test boards. It is worth mentioning that the test setup must be as symmetrical as possible for this kind of test.

These measurements were repeated for other test boards and the current mismatch was found to be less than  $\pm 17 \text{ mA}$  for an input current of 1 A representing 3.4%. More measurements will be carried out in the future to obtain better statistics. Up till now, all measurements indicate a proper startup and a proper functioning with a current distribution within the corner simulation limits.

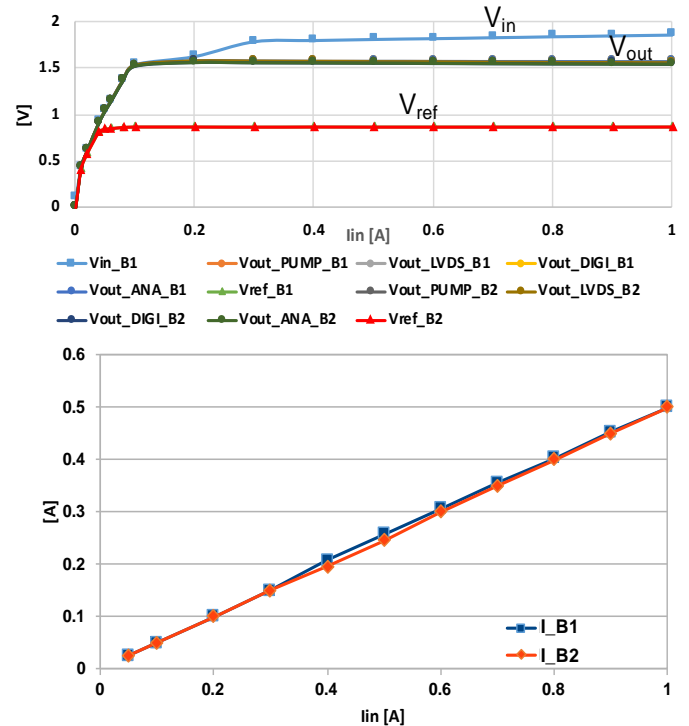


Fig. 14. Parallel powering of two test boards

### E. Transient test

The transient response of the Digital Domain regulator within the Main Domain was tested using an active load. A current pulse was drawn from the circuit output with an amplitude of 100 mA for duration of 500 ms, knowing that the input current was set to 400 mA and the slew rate was 5 A/ $\mu\text{s}$ . Off-chip capacitors of 10  $\mu\text{F}$  were used to filter the input voltage, output voltage and the bandgap reference voltage. The output transient response is illustrated in Fig. 15, where the signal was averaged to suppress the setup noise. A voltage variation of 2.8 mV is measured in response to the current pulse. No overshoot or undershoot are observed in the averaged signal.

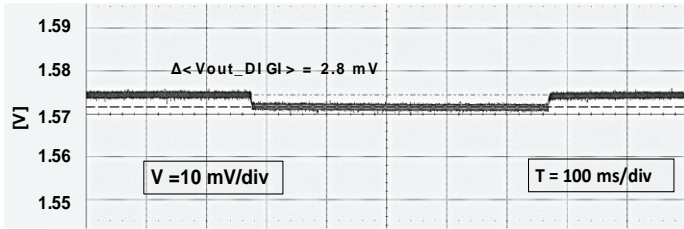


Fig. 15. Transient response of the Digital Domain regulator to a current pulse of 100 mA.

## V. IRRADIATION TESTS

### A. Test Setup

The irradiation tests were performed at IM2NP laboratory in Marseille using an X-ray machine powered at 20 kV and 20 mA. The shunt regulator test board was placed inside the X-ray chamber and fixed on a table whose coordinates were controlled by computer. The device under test (DUT) was centered at a distance of 20 mm under the X-ray beam. At these settings, the expected dose rate is 15 kRad/min. The positioning and the dose rate were previously calibrated using a photodiode.

The DUT was powered using two current sources to independently test the Pwell regulator (1 module) and the Main Domain regulator (126 modules). The two current sources shared the same ground potential, which was connected to the common substrate. A Labview program controlled the current sources, as well as a multi-channel voltmeter that was placed inside the X-ray chamber. Both regulator domains were powered at a nominal current of 10 mA for Pwell domain, and 200 mA for the Main Domain. Without cooling, the chip temperature was about 40 °C as measured by a thermal camera.

During irradiation, an automatic follow-up of the input voltages was set for both domains with a reading every 5 minutes. At several doses, the irradiation was paused to perform DC scans. These doses are: 0.1, 1, 3, 18, 38, 61 and 125 MRad. While scanning one domain, the other domain was kept at its nominal operation point. The DUT was irradiated up to 125 MRad.

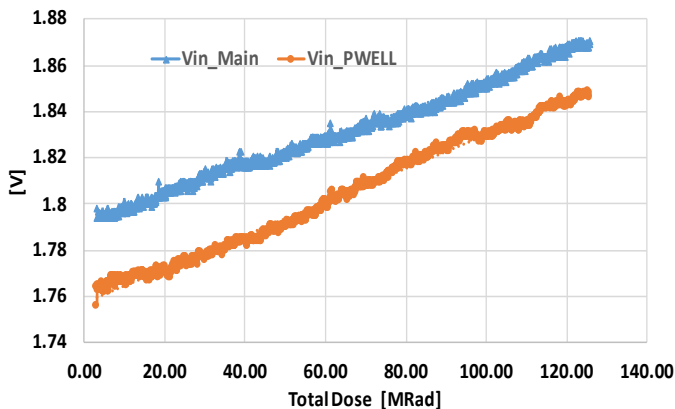


Fig. 16. Regulators input voltages follow up during irradiation

### B. Test Results

The input voltages follow up is shown in Fig. 16. Both the Main Domain and the Pwell input voltages increase slightly with irradiation at an average rate of 0.7 mV/MRad and 0.6 mV/MRad respectively.

### 1) Results for a single module

For the Pwell regulator (1 module), the output voltage 'Vout\_Pwell', and bandgap reference voltage 'Pwell\_Vref' scans at various irradiation doses are presented in Fig. 17 and Fig. 18 respectively. In all curves, the voltage levels tend to increase within the limit of 8% after 125 MRad in comparison to the corresponding value before irradiation (pre-Rad). Fig. 19 plots the variation of the input and output voltages as a function of the bandgap reference voltage as it increases with the irradiation dose. A strong correlation is observed, as the input and output voltages follow the increase of Vref\_Pwell linearly. The slope of the linear fit corresponds to the resistive ratios  $\alpha_1$  and  $\alpha_2$ .

Indeed, the input and output voltages are directly proportional to the bandgap reference potential as described in section II. In order to assess the irradiation impact on the shunt regulator itself, the contribution of the reference voltage was removed in post-processing, i.e. the calculated contribution of  $V_{ref}$  is subtracted from  $V_{in}$  and  $V_{out}$ . The results presented in Fig. 20 show that the regulator's response is stable with respect to the dose with an intrinsic variation of the input and output voltages less than 0.9% and 0.4% respectively.

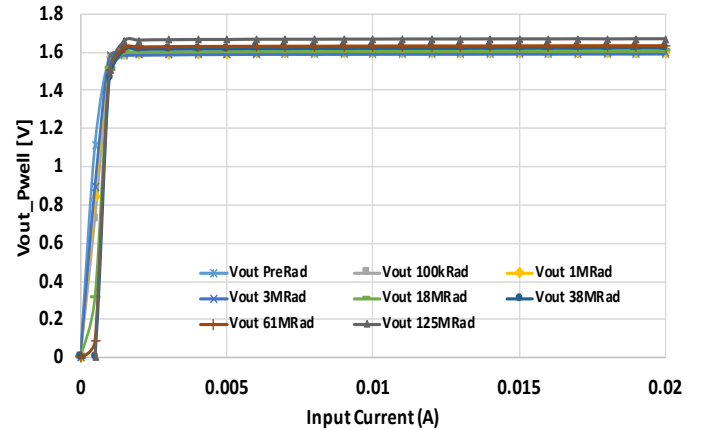


Fig. 17. Output voltage of the Pwell regulator at various irradiation doses

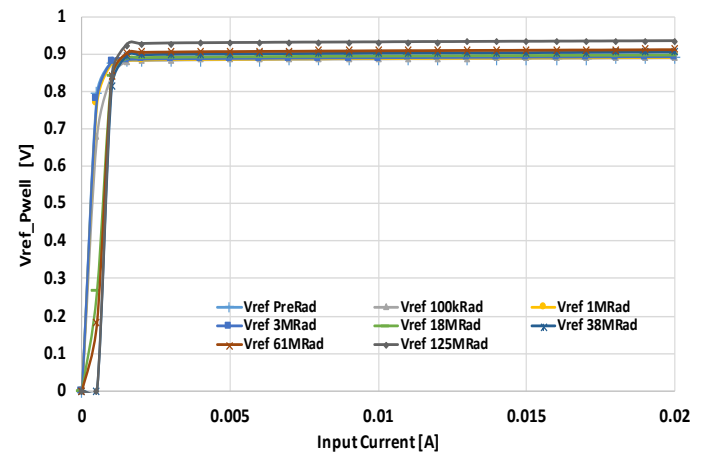


Fig. 18. Bandgap voltage of Pwell regulator at various irradiation doses

### 2) Results for the Main Domain

Fig. 21 shows the variation of the input, output and bandgap reference voltages with respect to the irradiation dose. The input and output voltages increase with dose by less than 8% at 125 MRad. Following the same analysis as in the previous section, the bandgap voltage contribution is removed in post-processing, and



the intrinsic Main Domain regulator performance is proven to be stable with irradiation with a variation less than 1.9 % for the input voltage and less than 0.6% for the output voltage.

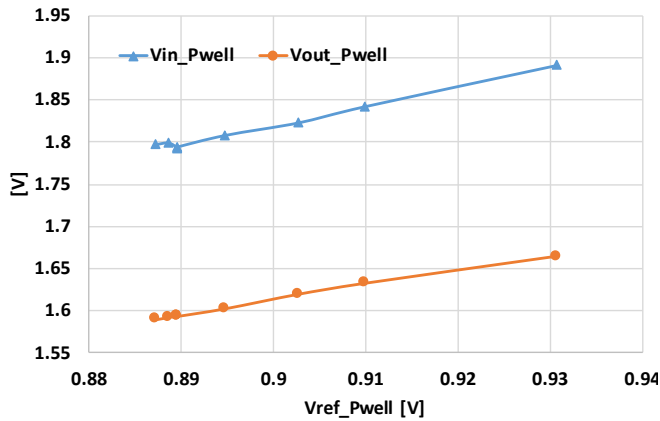


Fig. 19. Input and output voltages as a function of the bandgap voltage

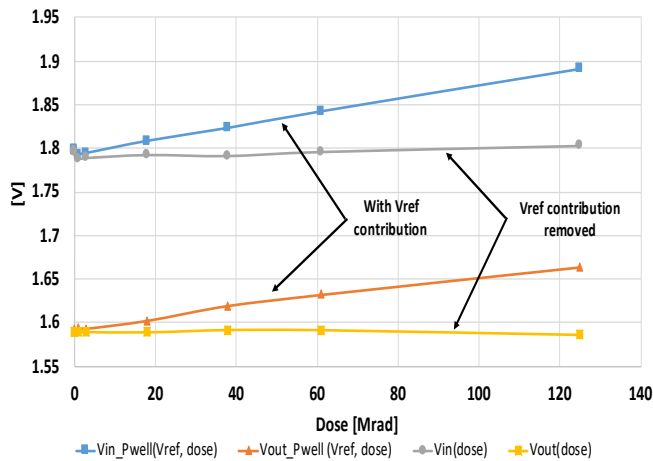


Fig. 20. Input and output voltage of Pwell regulator with and without the effect of the bandgap reference voltage

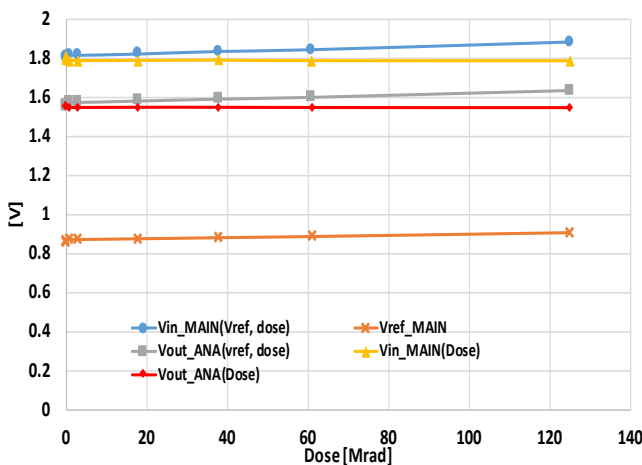


Fig. 21. Irradiation results for the Main Domain regulator, with and without the effect of the bandgap reference voltage

## VI. CONCLUSION

This work presents a solution for serially powering the pixel CMOS modules in ATLAS ITk or in other future applications, thus allowing a significant reduction in power losses and material

budget. The shunt regulator is based on a modular structure, which gives flexibility in design, and is advantageous for heat power dissipation. The module circuit design was presented with a stability analysis that leads to a design choice including on-chip compensation capacitors and off-chip decoupling capacitors. The elementary module was designed to deliver a nominal output current of 10 mA. Each module can operate with an input current between 3 mA and 18 mA with voltage drop-out of 200 mV. The input power can thus be adjusted to the load in order to minimize losses. A test chip was designed in CMOS 0.18  $\mu\text{m}$  technology and includes a total of 128 modules and 3 bandgaps, connected in different manners to construct separate domains. Characterization measurements show that all domains start up correctly as expected by simulations. The bandgap value is however different by 100 mV and will be corrected in future submissions. For a regulator formed by 40 modules, the equivalent series resistance is measured to be 15 m $\Omega$ . The test chips were successfully tested in serial powering mode. In parallel powering mode, the current mismatch between two test chips was measured to be less than 3.4 % for an input current of 1 A. Moreover, transient tests showed the system to be stable and performing as expected by the theory. An overheat problem was identified which will be addressed in the next PCB design. Finally, irradiation tests confirm the proper functioning of the regulator after a total dose of 125 Mrad. A variation of less than 8% was measured in the regulator output voltage. This variation was found to be mainly due to variation in the bandgap reference voltage. After signal processing, the intrinsic variation of the shunt regulator output voltage is found to be less than 0.6%, once the bandgap contribution is removed.

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