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# SIMULATIONS, MEASUREMENTS AND EQUIVALENT CIRCUIT FOR A CPW-CPW VERTICAL INTERCONNECTION

Janusz Rudnicki<sup>\*</sup>, Camilla Kärnfelt<sup>#</sup>, J. Piotr Starski<sup>#</sup>

## **Abstract:**

*Computer simulations and measured results for vertical interconnections between a CPW transmission line and a CPW chip (CPW-CPW) are presented. An equivalent electrical circuit, containing frequency independent elements, was extracted up to a frequency of 65GHz and is also presented.*

## **Introduction:**

Flip chip technology is presently a major trend in packaging of RF circuits. For a flip chip assemble the chip is mounted on the carrier with the active surface of the chip turned downwards to the carrier. The connections between the carrier and the chip are achieved by metal posts (bumps) placed on the special metallised areas (bump pads).

Flip chip interconnections have several advantages over the wire bonding. The main advantage is the bump's inductance, which can be less than 10% of a similar wire bond. This is especially significant in high speed and high frequency applications. Another advantage of flip chip technology is that the bumps can be located on the entire surface of the carrier and the chip. For the wire bonded structures the pads for wire connection should be located along the edges of the chip in order to minimize the length of the connecting wires.

Fig. 1 shows a CPW-CPW flip-chip bonded circuit used in the measurements. This structure contains two CPW-CPW structures (upper and lower part of structure). As shown in Fig. 2, 37 samples with two CPW-CPW structures were used in measurements. The upper and lower CPW-CPW structure was measured, and 74 measurement results were obtained.

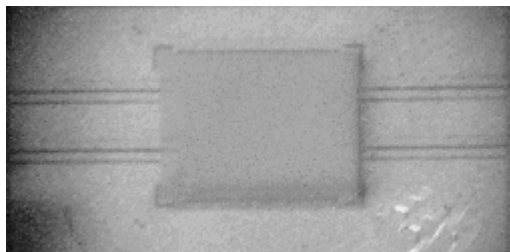


Fig. 1. Structure used in the measurements.

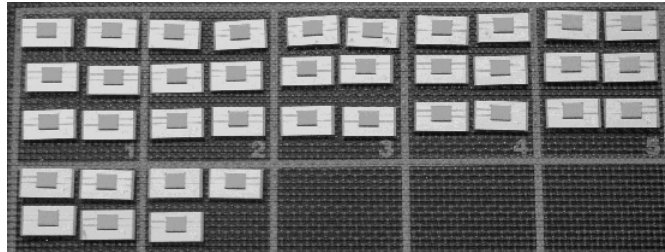


Fig.2. 37 samples used in the measurements.

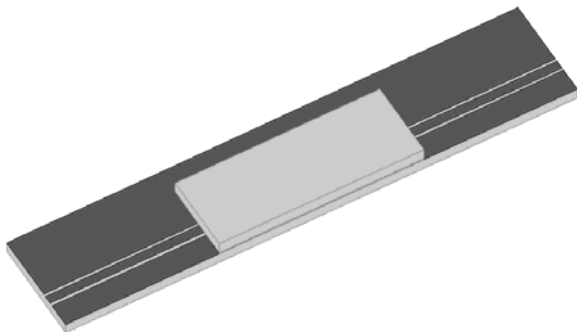


Fig. 3. Structure used in simulations.

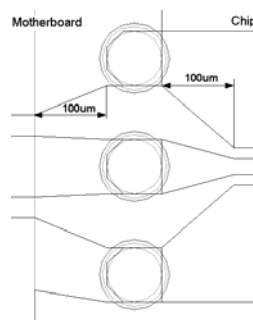


Fig. 4. 100µm taper length on motherboard and on the chip.

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In simulations the upper part of the structure presented in Fig. 1 was used, as shown in Fig. 3. All simulations were performed with the QuickWave 3D FDTD Simulator [1]. The lines on the substrate and on the chip are designed as 50Ω CPW. For the CPW transmission line and the CPW chip the alumina substrate thickness is 254μm, the strip width is 84μm and the metallisation thickness is 3μm. In the calculations we use a CPW transmission line with length of 5 mm on each side of the chip. The CPW chip is 2 mm long. On the motherboard all pads are 75μm x 75μm and square. On the chip all pads are 75μm x 75μm with octagonal shape. On the carrier and on the chip we use smooth transition from motherboard to bump pads with 100μm length, as shown in Fig. 4.

## Measurements

Measurements and simulation results are presented in Figs. 5-6. Solid lines represent measurement results for 58 structures. Based on the measurement results two flip-chip technology parameters can be defined:

- repeatability – percentage of the circuits with compared results
- reliability – percentage of good circuits

The 40 measurement results are close to each other (the difference is less than 3dB, Fig. 5), and we can calculate the repeatability of the flip-chip technology, defined by:

$$\text{repeatability [\%]} = \frac{\text{no. of comparable measurement results}}{\text{no. of all measurement results}} * 100\%$$

The reliability for the CPW-CPW structures can be defined by:

$$\text{reliability1 [\%]} = \left( 1 - \frac{\text{no. of bad structures}}{\text{no. of all structures}} \right) * 100\%$$

The reliability for the samples with two CPW-CPW structures can be defined by:

$$\text{reliability2 [\%]} = \left( 1 - \frac{\text{no. of bad samples}}{\text{no. of all samples}} \right) * 100\%$$

The calculated repeatability of the flip-chip technology is about 54 percent (for 40 curves, Fig. 5). There were 4 samples with one broken CPW-CPW structure and 4 samples with both structures broken. That implies that 12 structures and 8 samples were bad. It means, that the reliability of the 74 CPW-CPW structures is about 84 percent, and the reliability of the 37 samples is about 78 percent.

As shown in Fig.5 and Fig. 6, measured CPW-CPW connection shows good results up to 60 GHz, and the measurement results are in good agreement with the field simulated results, marked as a cross.

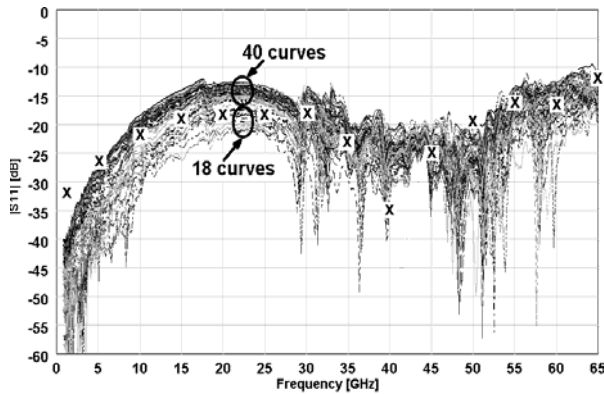


Fig. 5. Measurement results for |S11|.

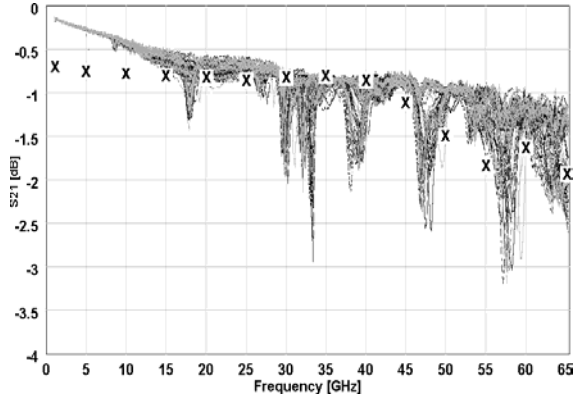


Fig. 6. Measurement results for |S21|.

## Equivalent circuit

An equivalent electrical circuit for CPW-CPW transition containing frequency independent elements, up to a frequency of 65 GHz was developed. Fig. 7 shows, where the equivalent circuit's elements for bumps section are placed in the CPW-CPW structure. Fig. 8 shows the equivalent circuit for bumps section. Each bump is represented by a parallel link of the capacitance  $C_p$  (capacitance between upper and lower bump pad) and inductance  $L_b$  (bump inductance). Capacitance  $C_p$  depends on the bump pad size (area of the bump pad outside the bump) and on the bump height. Inductance  $L_b$  depends on the bump height and bump diameter. The capacitance  $C_c$  represents capacitance between bump pads (i.e. between strip bump pad and ground bump pad), and depends on the bump pitch, bump pad size and bump pad shape. The ground on the motherboard is the 'real' ground. The ground on the chip is not the same ground as on the motherboard – it is connected to the 'real' ground through the ground bumps (capacitance  $C_p$  and inductance  $L_b$  in parallel).

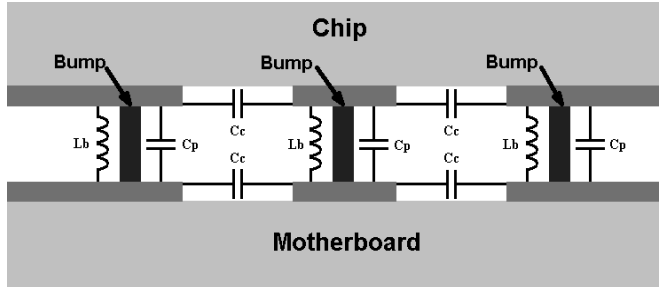


Fig. 7. Location of inductances and capacitances in the bump section for a CPW-CPW transition..

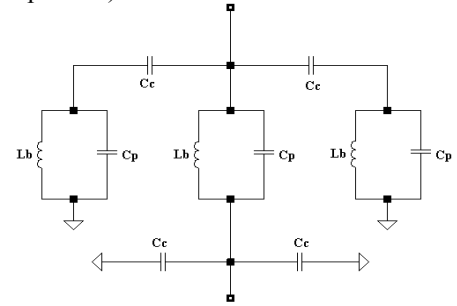


Fig. 8. Equivalent circuit for a bump section.

Simulations of the equivalent circuit were performed with the ADS [2]. In simulations the model of coplanar lines represents the coplanar lines on the motherboard and on the chip and the bump pads section. Because there is no model for smooth CPW transition between CPW transmission line and bump pads, we use the staircase approximation, as shown in Figs.9-10. We use a five CPW transmission lines with  $20\mu\text{m}$  length and equal stepped width of the signal line and gap.

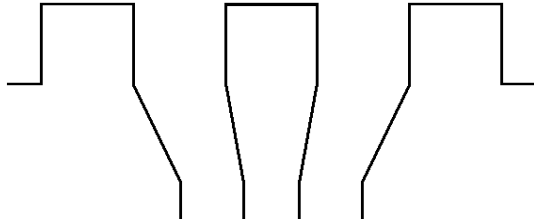


Fig. 9. Smooth transition between CPW transmission line and bump pads.

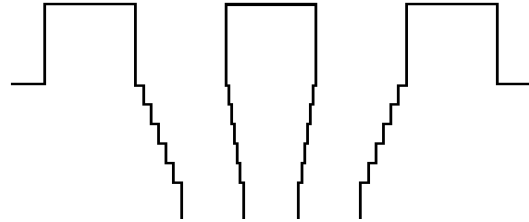


Fig. 10. Smooth transition approximated by five CPW transmission lines.

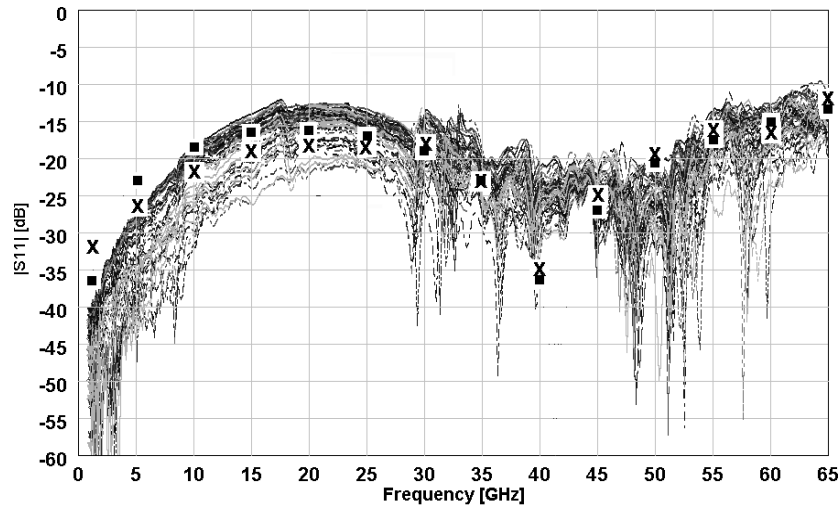


Fig. 11. Comparison of the measurement results (solid lines), field simulated results (cross) and simulated results for equivalent circuit (squares)

Fig. 11 presents the measured results for the CPW-CPW structures (solid lines) compared to the full wave simulated results (crosses) and to the simulated results for the equivalent circuit. The results for the equivalent circuit are in very good agreement with field simulation results and measured results from 20 GHz up to 65 GHz. Although the agreement is very good, the parameters of the equivalent circuit are not dependent on the dimensions of the CPW-CPW structure (mainly on bumps and bump pads dimensions). It remains as a topic for a future investigation

## Conclusions

The measured results for CPW-CPW structure were presented and compared to the field simulation results. The measured results are in good agreement with the field simulation results. Two parameters, repeatability and reliability of the flip-chip technology, were calculated.

We have also proposed an equivalent circuit for the considered CPW-CPW structure containing frequency independent elements. The simulation results for the equivalent circuit are in good agreement with the measured results and field simulation (full wave) results.

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