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# Nonuniformly Distributed Electronic Impedance Synthesizer

Yangping Zhao *Member, IEEE*, Simon Hemour, *Senior Member, IEEE*,  
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**Abstract**—Benefiting from advantageous features of fast tuning, small size, and easy integration, the electronic impedance synthesizer (EIS) has been developed for on-wafer load–pull characterization systems, tunable matching networks, reconfigurable devices and systems, and so on. The previous designs of the EIS were mostly based on the empirical data instead of a closed-form design. Moreover, incomplete figures of merit (FOM) were chosen to optimize and evaluate the EIS. In this paper, we propose and present, first of all, a semiclosed-form design procedure for the distributed EIS. Then, a particle swarm optimization method is introduced to optimize the proposed nonuniformly distributed EIS, which comprises an adjusting circuit and a nonuniformly distributed circuit. Experimental results demonstrate that the proposed nonuniformly distributed structure can not only improve the Smith chart coverage but also reduce the size, compared to the uniform counterpart. The fabricated nonuniform EIS operating from 0.8 to 2.5 GHz, exhibits a good agreement between theory and measurement. Furthermore, the most comprehensive FOM are presented to evaluate the fabricated EIS.

**Index Terms**—Electronic impedance synthesizer (EIS), electronic tuner, load–pull, nonlinear transmission line (NLTL), particle swarm optimization (PSO), reconfigurable device, tunable matching network (TMN).

## I. INTRODUCTION

THE ever-growing number of wireless communication devices sold per year requires the suppliers of power amplifiers (PAs) or radio modules to dramatically increase their testing capabilities. Positioned at the output of a PA or radio module, an antenna generally has a limited area and is susceptible to load-pulling effects such as human touch and proximity environment. As a result, a whole set of

specifications of the PA or radio module must be evaluated with a quick stress test under different impedance conditions simulating a mismatch of the antenna.

The industry has been using an electromechanical impedance tuner, a well-established technique for field or on-site testing. This equipment allows for a very high level of mismatch and power but at the expense of an extremely low tuning speed. For on-wafer measurement, the electromechanical impedance tuner can only be placed far away from the device under test (DUT) due to its large size and weight. Additionally, the adjustable positioner also limits the flexibility and accuracy of measurements. Therefore, the industry has shown a special interest in the development of a fast tuning electronic impedance synthesizer (EIS) for many years. The tuning speed of EIS is in the range of milliseconds, whereas the tuning speed of electromechanical impedance synthesizer is in the range of seconds. The synthesis rate is almost instantaneous and can reduce the measurement time dramatically. This is very important for a full-range testing of several direct current (dc) and radio frequency (RF) parameters of PA or radio module in production runs, especially when a large throughput is required.

Beside the applications expected in a device characterization system, EIS has also been widely used as a tunable matching network (TMN) for reconfigurable devices or systems [1]–[9]. The development of software-define radio and new generation communication systems requires a number of reconfigurable devices and components which can operate in different frequency bands compatible with different communication standards. In a reconfigurable PA, TMN can be placed both in the input and output of the PA to match the impedances so as to improve the power transfer gain and efficiency. In a reconfigurable antenna, TMN can improve the maximum radiation power [9].

A traditional digital EIS is made by a set of switches combined with fixed capacitors, which are placed periodically along a transmission line. The switches can be p-i-n diodes [2], [3], varactors [4], [5], [10], [11], monolithic microwave integrated circuits or transistors [12]–[17], and microelectromechanical systems (MEMS) switches [1], [6]–[8], [18]. The position of a capacitor can be varied virtually along the transmission line by choosing an appropriate switch. In such a configuration involving  $N$  switches, the EIS can only provide a limited number of impedance states ( $2^N$ ) by combing different states of switches: ON and OFF. The EIS

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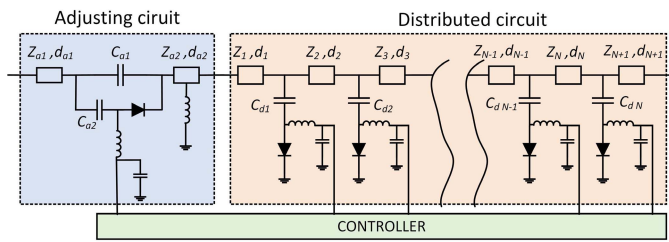


Fig. 1. Topology of nonuniform EIS consists of an adjusting circuit and a distributed circuit.

was mostly developed based on the topology of single-stub, double-stub, triple-stub [19], pi-structure [5], [9], [20], T-structure [21], as well as multiple artificial transmission lines [15] and transmission line with tunable impedance [22].

The topology for the distributed transmission line technique has been shown to have a better performance than double- or triple-stub topologies [1], [7], [14], [16], [19], [23]–[25], mainly because of the physical features of such a distributed structure. In the distributed double-slug EIS [1], 80 sections of minimal-contact MEMS varactors are located periodically along the transmission line. Although it has a uniform Smith chart distribution, a limited voltage standing wave ratio (VSWR) is realized, and a large number of varactors and control signals are needed for low frequency, which increases the complexity of the control circuit.

In fact, the uniform topology always presents a compromise solution even though it does not guarantee the best performance. The nonuniformly distributed structure has been demonstrated in sampling vector network analyzers (VNAs) [26] with better performance than the traditional uniform topology. The distance between two sections decreases along the propagation direction, the Bragg cutoff frequency increases so as to have a sharper rise time or fall time for the sampling. Although the application is different, the concept of nonuniformly distributed topology could be considered and implemented for EIS.

A type of nonuniformly distributed EIS has been presented in a patent [25], in which only one p-i-n diode is turned ON at any time, and it is not fully turned ON. The p-i-n diode in series with a grounded capacitor somehow acts as a varactor but with a large series resistance, which results in a large dissipation loss. Although this EIS can be applied to wideband applications, the nonfully turned ON p-i-n diode will cause a serious intermodulation distortion (IMD) problem for high-power applications [27]. Based on the same nonuniformly distributed topology in [25], EIS comprising two arrays of a solid-state tuner and a combiner network has been proposed [23]. The combination of two arrays with a total of  $2^*N$  switching elements can only generate  $N^2$  impedance states in lieu of  $2^N$ , somehow it is a waste of resources and space. In both works reported in [23] and [25], the prime number relationship was proposed for the physical lengths of transmission lines to avoid generating repeated reflection coefficient. However, this relationship does not guarantee the best Smith chart coverage.

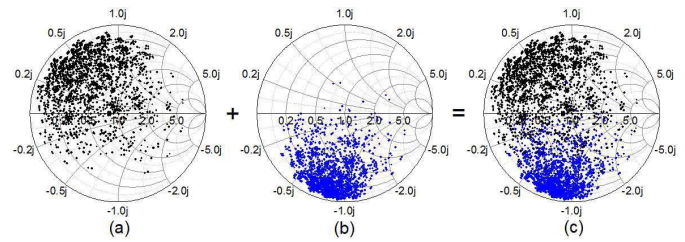


Fig. 2. Illustration of the effect of the adjusting circuit at 1.5 GHz. Impedance distribution on Smith chart when p-i-n diode is (a) ON and (b) OFF. (c) Total effect of the adjusting circuit on the improvement of Smith chart coverage.

In this paper, we propose and investigate a nonuniformly distributed EIS, which consists of an adjusting circuit and a nonuniformly distributed circuit (Fig. 1). Not only the transmission line length but also the impedance and loading capacitance for each section are nonuniform. The distributed circuit comprises a high-impedance transmission line nonuniformly loaded with different values of capacitors. The adjusting circuit comprises a small value capacitor (e.g., 2 pF) in parallel with a combination of a large value capacitor (e.g., 30 pF) in series with a p-i-n diode. When the p-i-n diode is turned ON, the total capacitance is around 32 pF, it almost does not have an impact on the impedance distribution of the distributed circuit [Fig. 2(a)]. By contrast, when the p-i-n diode is turned OFF, the total capacitance is around 2 pF, which can rotate the impedance distribution in the counterclockwise direction on the Smith chart [Fig. 2(b)]. As illustrated in Fig. 2, the role of the adjusting circuit is to compensate the uncovered area so as to improve the Smith chart coverage, at the same time to keep the total circuit length as short as possible. The adjusting circuit can be replaced by a variable phase shifter or the combination of several different transmission lines with switches, which can rotate the distributed points in the clockwise direction. However, the circuit proposed in this paper is simpler and smaller.

So far, except the double-slug distributed EIS [1], [28], it is difficult to have a closed-form design process for other topologies due to the unpredictable jumping of impedance states. This paper addresses the design and optimization issues of the proposed nonuniformly distributed EIS. In Section II, a semiclosed-form-enabled design procedure is proposed for distributed EIS. Then, a particle swarm optimization (PSO) process is developed in Section III for the multiparameter optimization problem of an EIS. The definition of the Smith chart coverage developed in [27] is chosen as the fitness function of PSO.

In Section IV, the theory is validated by experiments. The experimental results show the effectiveness of the proposed nonuniform topology and the PSO method. Although Zhao *et al.* [27] has investigated the power-handling and non-linearity responses of a typical uniformly distributed circuit, no clues were given on the design nor the optimization strategy. The goal of this paper is to devise an efficient way to design and optimize a nonuniform EIS for general industrial applications.

The most meaningful and comprehensive figures of merit (FOM) are summarized and classified in Section V to

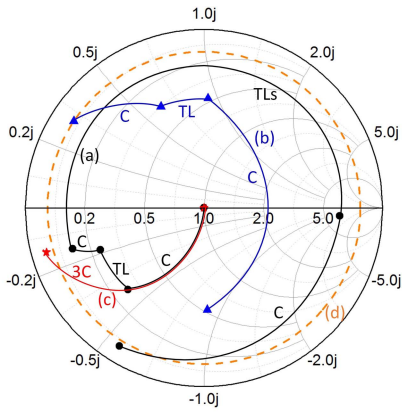


Fig. 3. Schematic of impedance movement when (a) loading capacitance over the capacitive part of Smith chart, (b) loading with  $C \cdot N/4$  ( $N = 12$ ), (c) loading with capacitance over the inductive part of Smith chart. (d) Required constant reflection coefficient circle.

fully evaluate the fabricated EIS. In [27], the loss definition at two different scenarios is discussed, while four scenarios are discussed in this paper, which can show the overall perspective for the applications of EIS. In addition, the voltage distribution theory developed in [27] is utilized to investigate the power-handling capacity and nonlinearity of the proposed nonuniform EIS.

## II. SEMICLOSED-FORM DESIGN PROCEDURE

A semiclosed-form design procedure is proposed for a distributed topology in order to obtain the initial values and boundaries for multiple parameters. The range of loading capacitance is first determined from an estimation of the maximum reflection coefficient. Then, the maximum distance  $d$  between each two sections is determined by the Bragg cutoff frequency according to the nonlinear transmission line (NLTL) theory [7], [28], [29], while the minimum distance  $d$  is determined by a rule in which the total length should be larger than a half-wavelength of the lowest frequency so as to have a large Smith chart coverage. A quantitative analysis of Smith chart coverage, which describes the percentage of the Smith chart covered by an EIS, is helpful for the evaluation and optimization of the EIS. The detail of the definition of the EIS has been described in our previous work [27].

### A. Determination of the Range of Loading Capacitance

As shown in Fig. 1, input admittance  $Y_{in}$  of the EIS can be calculated from the load side easily. In order to simplify the scenario which is similar to a real calibration condition, the admittance of source and load are set as  $Y_s = Y_L = 0.02$ . Fig. 3 illustrates how the impedance moves on the Smith chart when multiple capacitors are loaded along the transmission line. As can be seen in Fig. 3(a), only when the impedance is located over the capacitive part of the Smith chart, the loaded capacitance can further increase the reflection coefficient. To figure out the maximum  $\Gamma$ , we need to focus on the capacitive part of the Smith chart. Since the total length of a transmission line having  $N$  sections should be longer

than a half-wavelength of the minimum frequency of interest, the capacitance will be loaded over the capacitive part of the Smith chart at least  $N/4$  times at each frequency. Therefore, the maximum  $\Gamma$  can be estimated by only one transmission line loaded with  $C \cdot N/4$ . Then, the input admittance can be calculated by

$$Y_{in} = Y_L + j\omega C \cdot N/4. \quad (1)$$

The estimated maximum reflection coefficient  $\Gamma$  can be expressed as

$$\Gamma = \frac{Y_s - Y_{in}}{Y_s + Y_{in}} = \frac{-j\omega C \cdot N/4}{2Y_s + j\omega C \cdot N/4}. \quad (2)$$

The magnitude of the estimated  $\Gamma$  needs to be larger than the required reflection coefficient  $\Gamma_{req}$

$$|\Gamma| = \frac{\omega C}{\sqrt{(8Y_0/N)^2 + (\omega C)^2}} \geq |\Gamma_{req}|. \quad (3)$$

As such, we can obtain the lower boundary of the loading capacitance

$$C_d \geq \frac{4Y_s}{N\pi f} \frac{|\Gamma_{req}|}{\sqrt{1 - |\Gamma_{req}|^2}}. \quad (4)$$

To have a Smith chart coverage as large as possible, and also to keep the impedance points distributed in the Smith chart as uniform as possible, another condition will be imposed. When only one capacitance  $C$  is loaded, the reflection coefficient should be smaller than the required  $\Gamma_{req}$ . Otherwise, most of the impedance points will distribute at the edge of the Smith chart. This can be expressed as

$$|\Gamma| = \frac{\omega C}{\sqrt{(2Y_s)^2 + (\omega C)^2}} \leq |\Gamma_{req}|. \quad (5)$$

Subsequently, we can obtain the upper boundary of the loading capacitance

$$C \leq \frac{Y_s}{\pi f} \frac{|\Gamma_{req}|}{\sqrt{1 - |\Gamma_{req}|^2}}. \quad (6)$$

For a requirement of  $|\Gamma_{req}| = 0.875$ , the maximum and minimum loading capacitances are plotted in Fig. 4 as a function of frequency for an EIS with 12 sections. A proper capacitance can be chosen ideally to have more than one octave operation bandwidth. In practice, the results on the two sides of the frequency band are not always satisfactory. At low frequency, the impedance distribution will be concentrated at the center of the Smith chart due to the low loading capacitance, while the impedance distribution at high frequency will be close to the edge of the Smith chart because of the relatively large loading capacitance. As a matter of fact, the operation bandwidth of a real circuit is smaller than one octave, which is limited by the parasitic parameters from the commercial p-i-n diode and capacitor as well as pads.

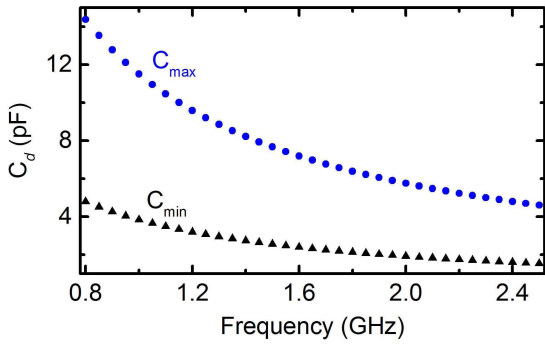


Fig. 4. Lower and upper boundaries of loading capacitance.

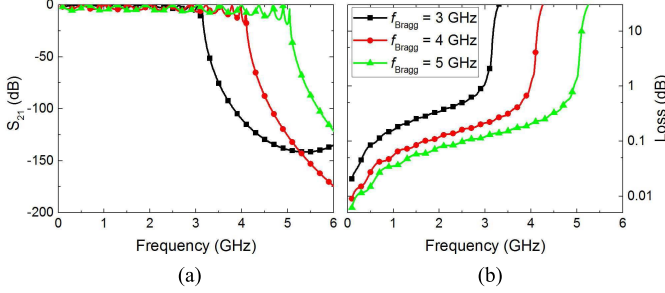


Fig. 5. (a) Transmission response and (b) loss feature of EIS with  $f_{\text{Bragg}}$  of 3, 4, and 5 GHz. Only conductive loss and dielectric loss are taken into consideration in the total loss. The ripples in transmission response are caused by the mismatch at this impedance state. Note that it is only the response of the impedance state with all the p-i-n diodes which are turned ON.

### B. Determination of the Range of Distance $d$

When all of the p-i-n diodes are turned ON, the distributed circuit (Fig. 1) is similar to a conventional NLTL [30], and the Bragg cutoff frequency will be applied due to the low-pass property [7], [29], [31]

$$f_{\text{Bragg}} = \frac{1}{\pi d} \frac{1}{\sqrt{K}} \frac{c}{\sqrt{\epsilon_{\text{reff}}}} \quad (7)$$

where  $d$  denotes the distance between two sections,  $c$  is the speed of the light, and  $\epsilon_{\text{reff}}$  is the effective dielectric constant of unloaded transmission line. The scaling factor  $K$  is expressed as

$$K = 1 + \frac{C}{d} \frac{cZ_0}{\sqrt{\epsilon_{\text{reff}}}} \quad (8)$$

where  $C$  is the loading capacitance, and  $Z_0$  is the impedance of unloaded transmission line. The cutoff frequency should be larger than the highest operation frequency  $f_{\text{Bragg}} > f_H$ ; otherwise, it will cause a serious loss problem (Fig. 5). Then, the upper boundary for the distance  $d$  can be expressed as

$$d < \frac{c}{2\sqrt{\epsilon_{\text{reff}}}} \left[ \sqrt{(C \cdot Z_0)^2 + \left( \frac{2}{\pi f_{\text{Bragg}}} \right)^2} - C \cdot Z_0 \right]. \quad (9)$$

The effect of the Bragg cutoff frequency is illustrated in Fig. 5, where the transmission response and loss feature with different  $d$ , respectively, leading to  $f_{\text{Bragg}}$  of 3, 4, and 5 GHz are shown. The loss will increase dramatically after

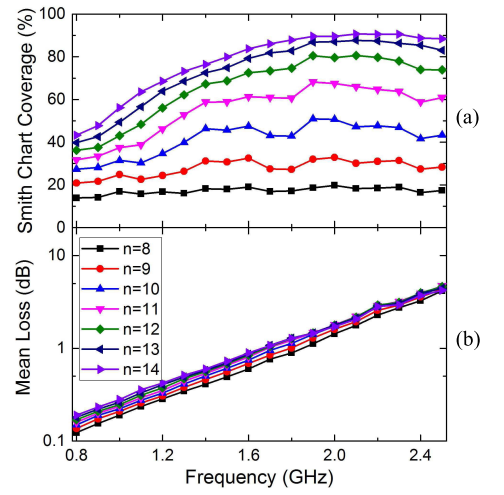


Fig. 6. Investigation of (a) Smith chart coverage and (b) mean loss of EIS with a different number of sections while keeping  $f_{\text{Bragg}}$  as 4 GHz. Mean loss is the average loss for the selected impedance points. Reactive parasitic parameters from commercial p-i-n diode and capacitor are not taken into consideration in the loss.

the cutoff frequency, and a higher cutoff frequency will result in a lower loss in the operation frequency band, but at the cost of a smaller  $d$ . In other words, more sections will be needed to have a high Smith chart coverage, which in turn increase the total loss, so that a tradeoff needs to be made. In this paper, a cutoff frequency of 4 GHz will be chosen for the EIS with an operation frequency band of 0.8–2.5 GHz.

To guarantee that there are enough impedance points at the starting frequency point, the total length of the transmission line should be larger than a half-wavelength of the lowest frequency. Then, the distance between two sections should be

$$d > \lambda_{\text{max}}/2(N + 1). \quad (10)$$

Compared to the strict limiting factor in (9), the lower boundary of  $d$  is more flexible. If a low starting frequency and a high Bragg cutoff frequency are chosen, a conflict will occur between (9) and (10). In this case, the restriction of (9) should be followed. In the general case, (9) and (10) will limit  $d$  to a small range, which is critical for design.

The Smith chart coverage and mean loss are investigated for the EIS with a different number of sections (Fig. 6) while keeping  $f_{\text{Bragg}}$  as 4 GHz. As can be seen that when  $d$  is limited by (9), the Smith chart coverage can be improved by increasing the number of sections but with the sacrifice of loss.

It can be also seen in Fig. 6 that the minimum coverage within a certain bandwidth always occurs at both sides of the frequency range. Therefore, the relationship between the minimum coverage for a certain bandwidth and the number of sections  $N$  could be obtained, which can be used as a preliminary guidance to determine the minimum  $N$  according to the required coverage.

### C. Selection of p-i-n Diode and Determination of $Z_0$

The p-i-n diode has a wide intrinsic layer; therefore, it can handle a high RF voltage [32], thus having a good

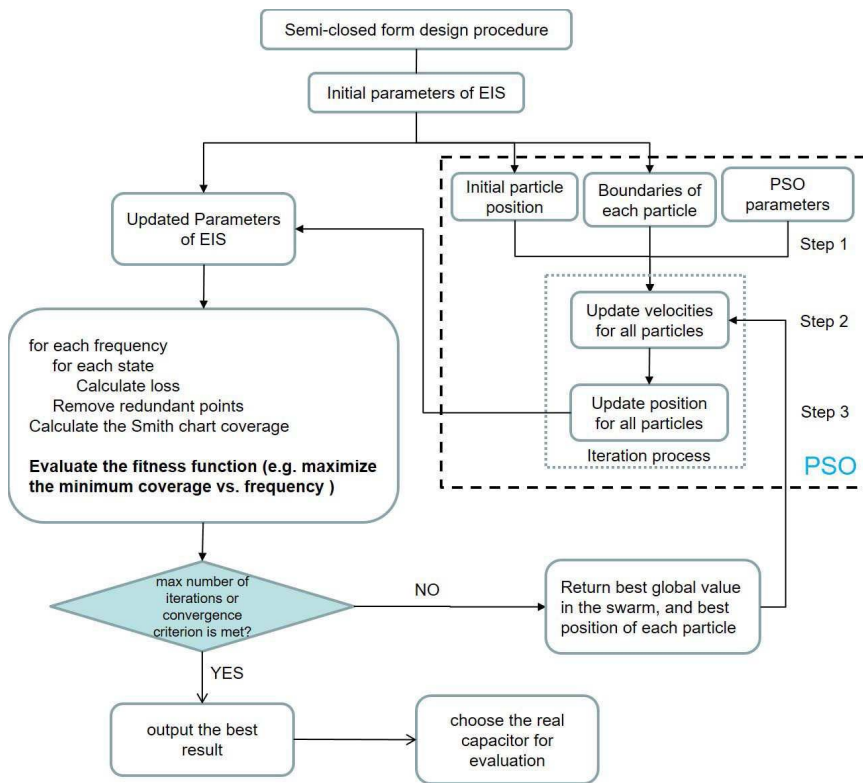


Fig. 7. Diagram of optimization process using PSO.

linearity [27]. In addition, a p-i-n diode has a fast switching time [33], [34]. In this paper, commercial p-i-n diodes are selected for the design of an EIS mainly based on two aspects: parasitic parameters and power-handling capacity. A tradeoff needs to be made between series resistance and capacitance since they have an opposite relationship with respect to the junction area. The details about power-handling capacity and nonlinearity analysis were presented in our previous work [27]. In this paper, SMP1320-079LF from Skyworks Solution Inc. with  $8\ \mu\text{m}$  intrinsic layer and BAR95-02LS from Infineon Technologies with  $19\ \mu\text{m}$  intrinsic layer are chosen for our experiments to handle at least  $0.5\ \text{W}$  continuous wave power.

In a similar way as in the NLTL theory, the initial impedance of the unloaded transmission line  $Z_0$  is set to be a high value, in order to keep the loaded impedance close to  $50\ \Omega$  after loading the capacitors. Increasing  $Z_0$  improves the Smith chart coverage of the EIS, but a high  $Z_0$  leads to a narrow trace, where soldering the commercial components becomes challenging.

### III. OPTIMIZATION

For an EIS with  $N$  sections (Fig. 1),  $3 \times N + 6$  variables will be involved in the optimization process, including  $N$  loading capacitors,  $N + 1$  lengths of the transmission line and  $N + 1$  impedances for the distributed circuit, two capacitors, and 2 lengths of  $50\text{-}\Omega$  transmission line for adjusting circuit. The complexity of such an optimization problem is more pronounced with the number of sections. This paper is the

first to introduce PSO to solve the multiparameter microwave design problem of an EIS, which can dramatically shorten the development cycle.

PSO is an emerging heuristic search method, which is inspired by the collaborative behavior or information sharing mechanism of biological populations, such as flocks of birds and schools of fish. As a population-based search method, the best solution can be discovered by moving around a population (swarm) of candidate solutions (particles) in the multidimensional search space. The movement of each particle is guided not only by its local best-known position but also by the best-known positions of the entire swarm so as to move the swarm toward the best solution after several iterations.

#### A. Definition of Fitness Function

A fitness function is an FOM that indicates how close the design solution is to the goal. The Smith chart coverage will be considered as the fitness function since it is the most important criterion to evaluate an EIS. It should be noted that several criteria such as uniformity factor, loss, and power handling (discussed in Sections V-A2, V-C, and V-D) can also be integrated into the fitness function according to different applications.

#### B. Description of Optimization Process of PSO

Fig. 7 shows the diagram of the optimization process of an EIS, the engineering problem with multiple parameters can be considered as a multidimensional space in PSO, and each combination of parameters will be a position in the space.

The PSO algorithm consists of three steps, namely, generating particles' positions and velocities, velocity update, and position update. In a basic PSO algorithm, the initial position  $x_{k,i}$  and velocity  $v_{k,i}$  of each particle are generated randomly based on the upper and lower bounds of each particle. In this paper, we directly use the initial parameters that are obtained from the semiclosed-form design procedure. The initial position will dramatically reduce the searching time for the best solution.

In the second step, the velocity of particle  $i$  at time  $k + 1$ ,  $v_{k+1,i}$ , is updated from its current velocity  $v_{k,i}$  by the following equation [35]:

$$v_{k+1,i} = c_0 v_{k,i} + c_1 r_p \frac{p_i - x_{k,i}}{\Delta t} + c_2 r_g \frac{g_k - x_{k,i}}{\Delta t} \quad (11)$$

where  $p_i$  stands for the best position for particle  $i$ , while  $g_k$  represents the best global position value in the current swarm. It shows that the next search direction for each particle is influenced not only by its best position but also the best position in the swarm. Three weight factors are introduced to express the portion of influence for each term, namely, the inertia factor  $c_0$ , self-confidence factor  $c_1$ , and swarm confidence factor  $c_2$ . In addition, two uniformly distributed random parameters  $r_p$  and  $r_g$  are applied to guarantee a good coverage and avoid local optimal. The last step of PSO in each iteration is to update the position with the following equation:

$$x_{k+1,i} = x_{k,i} + v_{k+1,i} \Delta t. \quad (12)$$

The updated parameters after PSO are used to evaluate the fitness function. One important step to calculate the Smith chart coverage is to remove redundant impedance points and choose useful points. Several restriction conditions on loss, a uniformity factor and power handling can be applied in this step for a specific application. In order to have a high coverage over the whole frequency band of interest, we will find out the minimum coverage versus the frequency in each iteration. Then, in PSO, we will define the optimization goal as maximizing the minimum coverage. The best solution will be obtained when the maximum iteration is reached or the optimization goal is satisfied. It should be noted that the developed optimization method can be applied to optimize the specific area on the Smith chart if a special requirement is asked in the application.

Optimization results show that the difference of impedance of the  $N + 1$  transmission line does not improve the results obviously. Therefore, we can remove some optimization variables in order to reduce the optimization time. PSO is inherently a continuous optimization method, one can modify it to handle discrete design variables according to the commercial value of capacitors. Actually, a slight change of capacitance does not have much effect on the performance of an EIS. Therefore, we can just replace the optimized capacitance with the closest practical capacitor value.

As for the computational efficiency of PSO, an optimization with 27 parameters takes averagely 1.5 s for each iteration when the number of particles is set as one. In this paper, the number of particles of PSO is set up as 20, the optimal value can be reached after 20 iterations, which means 10 h for the optimization of an EIS with 27 variables. It is worthwhile

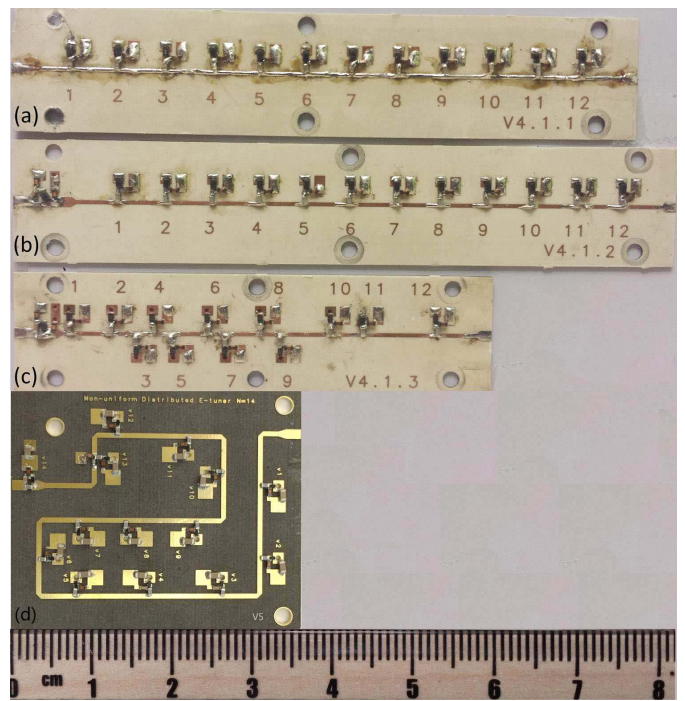


Fig. 8. Fabricated uniform and nonuniform circuits, biasing wires are not shown. (a) Circuit 1: 12 sections uniformly distributed topology without adjusting circuit. (b) Circuit 2: 12 sections uniformly distributed topology with one section of adjusting circuit. (c) Circuit 3: 12 sections nonuniformly distributed topology with one section of adjusting circuit. (d) Circuit 4: New 13 sections nonuniformly distributed EIS with one section of adjusting circuit.

to note that the total optimization time decreases when the number of parameters reduces.

#### IV. EXPERIMENT

In order to validate the design procedure as well as the optimization method, three general-purpose EISs [Fig. 8(a)–(c)] are proposed for 0.8–2.5 GHz. Only Smith chart coverage and loss are considered in the fitness function of optimization to simplify the verification of the theory. As shown in Fig. 8, three circuits are optimized and fabricated on the Rogers 6002 substrate with a thickness of 20 mils. Circuit 1 is a 12 sections uniformly distributed topology with  $d = 5.71$  mm,  $C_d = 1.8$  pF, and  $Z_0 = 83 \Omega$  [Fig. 8(a)]. Based on circuit 1, circuit 2 adds an adjusting circuit [Fig. 8(b)], in which  $C_{a1}$  is 1.8 pF, and  $C_{a2}$  is 30 pF (Fig. 1). All the parameters of circuit 2 are optimized nonuniformly [Fig. 8(c)], the distance  $d$  in circuit 3 varies from 1.48 to 9.16 mm, while the loading capacitance  $C$  varies from 0.7 to 9.1 pF. It is apparent that the circuit 3 has a smaller size than circuits 1 and 2.

The three circuits [Fig. 8(a)–(c)] are measured automatically with the software FDCS provided by Focus Microwaves Inc., and a controller is dedicated to switching the states of EIS. The measured and theoretically calculated Smith chart coverages of these three circuits are depicted in Fig. 9. Theoretical result of circuit 2 has a Smith chart coverage 10% better than circuit 1, which has validated the effect of the adjusting circuit. Theoretical result of nonuniform circuit 3 further improves the Smith chart coverage compared to circuit 2.

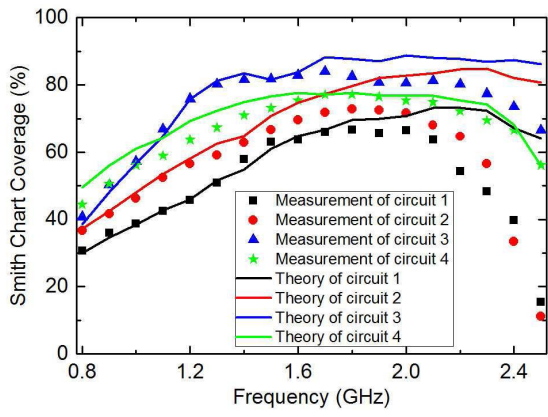


Fig. 9. Comparison of measured and theoretically calculated Smith chart covers for four fabricated circuits.

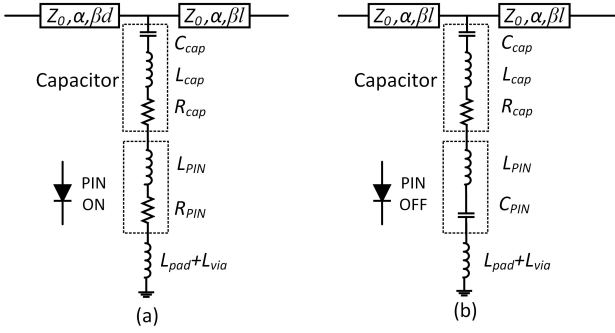


Fig. 10. Equivalent circuit model of a unit circuit when p-i-n diode is turned (a) ON and (b) OFF.

However, the measurement results for all the three circuits deviate from the theory at high frequency. Measurement results prove the effectiveness of the nonuniform topology and PSO method, even though the deviation is observed between theory and measurement. Parametric studies are carried out to investigate the intrinsic reason of the deviation, showing that the series inductance and series resistance are the two main factors resulting in the deviation in Fig. 9.

The EIS is sensitive to every parasitic parameter in the real circuit, so the equivalent circuit model of a unit circuit of the EIS is necessary to be built. As depicted in Fig. 10, the commercial capacitor is modeled by a series circuit of  $RLC$ .  $L_{cap}$  is around 0.4 nH for a capacitor with 0402 footprint, which is obtained by fitting the self-resonance frequency of the capacitor. The p-i-n diode at ON state can be modeled by series inductor  $L_{p-i-n}$  and series resistor  $R_{p-i-n}$ , while OFF state is modeled by series inductor  $L_{p-i-n}$  and series capacitor  $C_{p-i-n}$ .  $L_{p-i-n}$  is dependent on the footprint selection of the p-i-n diode. The effects of connection pads and via holes can be modeled as an inductor, which is around 0.2–0.4 nH obtained from modeling the measured S-parameter of a unit circuit.

Among the parasitic parameters, the series inductance from the p-i-n diode, the capacitor, and the connection pads and via holes has a critical influence on the performance of an EIS, since it will resonate with the loading capacitor near the operation frequency band. The effect of the parasitic inductance is

studied at the impedance state with all the p-i-n diodes that are turned ON. When the total parasitic inductance  $L$  is 0, the Bragg cutoff frequency dominates. When  $L$  increases to 0.8 and 1.5 nH, the resonance frequency starts to dominate. The consequence is that the loss increases dramatically near the resonance frequency. The effect of parasitic inductance on the performance of an EIS is also studied for all the impedance states. The Smith chart coverage at high frequency is distorted seriously due to the increases in the parasitic inductance, and the mean loss at high frequency becomes worse.

Except the parasitic inductance, the series resistance is also a critical factor leading to the degradation of performance at high frequency. In a circuit with a high standing wave, a small parasitic resistance will cause an obvious loss problem due to the multipath loss. The sweep of resistance from 0 to 3  $\Omega$  leads to an increase in loss before the resonance frequency. The parametric study of the series resistance on the performance of EIS for all impedance states shows that the increase in resistance reduces the Smith chart coverage by more than 20%, and increases the loss more than 10 times at high frequency.

In circuits 1–3, the p-i-n diode labeled as SMP1320-079LF from Skyworks Solution Inc. is chosen, which has a series inductance around 0.7 nH. Therefore, the total parasitic inductance should be around 1.5 nH after considering the inductance from a commercial capacitor (0.4 nH) and the inductance from the connection pads and via holes (0.4 nH). It will resonate with the loading capacitance near the operation frequency band. However, only 0.9 nH parasitic inductance was considered in the first experiment due to the inaccurate modeling for the parasitics. In addition, the total series resistance should be around 3  $\Omega$  after taking into account  $R_{p-i-n}$  of 1  $\Omega$  from the p-i-n diode, and the series resistance of 2  $\Omega$  from the commercial capacitor and the connection pads. However, only 1- $\Omega$  parasitic inductance was considered in the first experiment. In summary, the inaccurate modeling of series inductance and series resistance leads to the deviation between theory and measurement at high frequency for circuits 1–3.

After considering the parasitic parameters in the design of a p-i-n diode-based EIS, some degree of correction should be made on (4), (6), and (9). However, these complicated corrections can be done in the optimization process instead of the design procedure. By contrast, the EIS based on MEMS [1], [7] does not suffer from the parasitic problem, so that it can be designed at the millimeter-wave frequency band.

The first experiment [Fig. 8(a)–(c)] shows that the nonuniform topology not only has a smaller physical size but also has a better Smith chart coverage than the uniform counterpart, which has validated the effectiveness of the proposed nonuniform topology. In order to further eliminate the gap between the measurement and theory at high frequency, a new nonuniform circuit is designed and optimized [Fig. 8(d)]. Two steps are carried out to reduce the parasitic inductance. First, the p-i-n diode of BAR95-02LS from Infineon Technologies with the parasitic inductance of 0.2 nH is selected. Then, shorter and smaller connection pads and larger via are made to have a minimum parasitic inductance around 0.2 nH. Even so, the total parasitic inductance is around 0.8 nH, and the



TABLE I

FINAL DIMENSION OF NONUNIFORMLY DISTRIBUTED EIS. UNIT: CAPACITOR: pF; IMPEDANCE:  $\Omega$ ; AND DISTANCE: mm

$C_{a1}$	2	$d_1$	8.26	$d_8$	5.49
$C_{a2}$	30	$d_2$	8.82	$d_9$	8.55
$Z_{a1}, Z_{a2}$	50	$d_3$	8.62	$d_{10}$	8.55
$Z_1 - Z_4$	74.4	$d_4$	8.82	$d_{11}$	7.98
$C_{d1} - C_{d13}$	2	$d_5$	8.82	$d_{12}$	8.58
$d_{a1}$	3	$d_6$	8.27	$d_{13}$	4.64
$d_{a2}$	2	$d_7$	8.75	$d_{14}$	8.82

total parasitic resistance is around 3  $\Omega$ . However, they are not avoidable if commercial components are used.

Since the minimum parasitic inductance of 0.8 nH is determined, the maximum loading capacitance will be limited to 2 pF so as to keep the resonance frequency at 4 GHz. From Fig. 4, we can see that this restriction will largely narrow the choices of loading capacitance. In other words, a small selectable capacitance will reduce the Smith chart coverage in the desired frequency band, especially at low frequency. As illustrated in Fig. 6, one solution to improve the Smith chart coverage is to increase the number of sections. In this paper, we choose total sections of 14, which include one section of adjusting circuit and 13 sections of distributed circuit. One reason is that the improvement of Smith chart coverage is not obvious with section number more than 14. Another reason is that the test limitation with the tuner controller from Focus Microwave Inc. is 14 bits. It should be noted that the fabrication on the wafer will not have such a large limitation, thanks to a small parasitic inductance, e.g., MEMS technique.

In circuit 4 [Fig. 8(d)], we use the same capacitance of 2 pF for all the capacitors in a nonuniform topology. Then, PSO is applied to optimize the distances between sections, and the optimized circuit dimensions are listed in Table I. Compared to circuit 3, the limitation of a fixed loading capacitance in circuit 4 leads to a larger  $d$  in order to have the Smith chart coverage as large as possible. The circuit is bent to reduce the total size. Fig. 11 depicts a good match between the measured and theoretical results of S-parameters for two impedance states with all the p-i-n diodes that are turned ON and OFF, respectively.

## V. EVALUATION

A variety of FOM have been presented to evaluate the TMN [1]–[3], [6], [7] and the EIS [8], [18], [36], [37] in the previous works. Indeed, the core of a TMN is an EIS; therefore, the evaluation FOM for a TMN and an EIS can be studied together. Table II lists all the FOM that have been used to evaluate TMN or EIS. Certain FOM can be selected from them for a specific application.

### A. Tuning Range

For either optimization or evaluation of an EIS, a quantitative criterion is always helpful. The tuning range of EIS usually can be represented by the Smith chart coverage [2], [3],

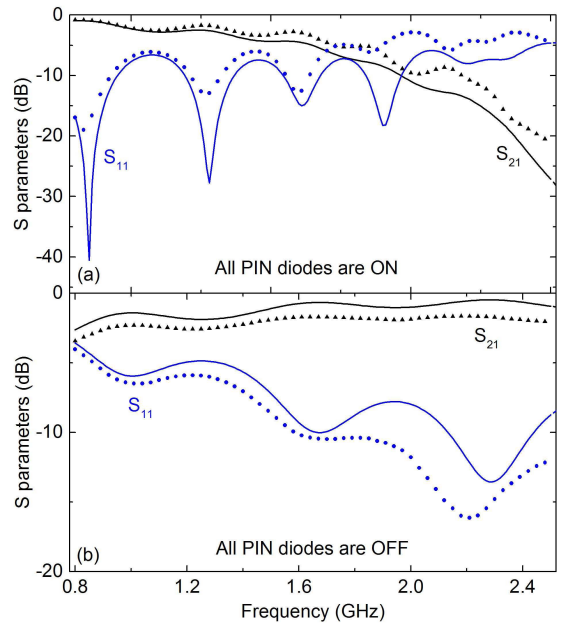


Fig. 11. Comparison of measured and theoretical S-parameters for impedance states with all the p-i-n diodes that are turned (a) ON and (b) OFF. Dot: measurement. While solid line: theory.

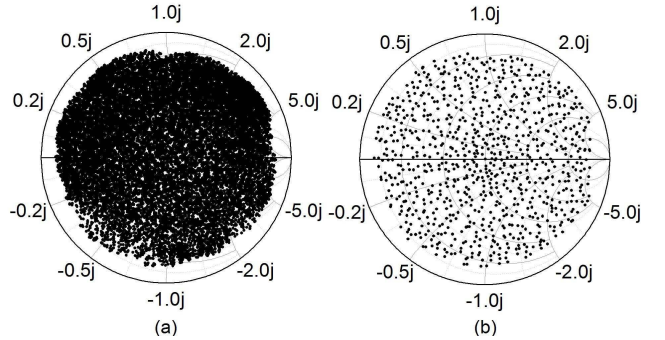


Fig. 12. (a) All 16384 measured impedance points. (b) Selected points for the calculation of Smith chart coverage.

uniformity factor [6], maximum VSWR [1], or maximum Gamma [38]. Most of the published work used one or two of them; however, each criterion has its own pros and cons. None of them can describe the tuning range alone. In this paper, we list all of them according to their significance

1) *Smith Chart Coverage*: Following the procedure in [27], useful impedance points are selected from the measured points, as depicted in Fig. 12(a) and (b). The Smith chart coverage is calculated by the ratio of the selected useful points to the total predefined points. The measured and simulated Smith chart coverages are compared in Fig. 9. The Smith chart coverage of circuit 4 exhibits lower than circuit 3 mainly because of the limitation of loading capacitance. However, the measured results show a good match with simulations after eliminating the impacts from the Bragg cutoff frequency and resonance problem, the difference is within 5%. In other words, the design of the EIS is reliable after considering the accurate parasitic parameters.

TABLE II  
SUMMARIZATION OF CRITERIA TO EVALUATE TMN AND EIS

Reference Criteria		Tunable Matching Network (TMN)					Electronic Impedance Synthesizer (EIS)				
		[7]	[1]	[6]	[2]	[3]	This work	[36]	[37]	[18]	[8]
Tuning Range	Smith Chart Coverage (Subjective)	x							x	x	
	Smith Chart Coverage (Numerical)				x	x	x				x
	Maximum VSWR Constant Circle		x				x				
	Uniformity Factor			x			x				
	Maximum Reflection Coefficient						x	x	x		
	Bandwidth						x	x	x		x
	Loss	x	x	x	x		x	x			x
	Case Study	x									
Power Handling	Voltage Distribution	x					x			x	
	1dB Point Test						x		x		
Nonlinearity	Linearity Test	x					x	x			
	Noise Figure						x	x			
Other Concerns	Tuning Accuracy						x		x		
	Tuning Resolution						x	x	x		
	Tuning Speed						x	x	x		
	Size, weight, easy integration						x	x	x		
	Others: spurious oscillations, temperature drift						x	x			

The measured and theoretical impedance distributions on the Smith chart at several frequencies are compared in Fig. 13. Since the impedance generated by the EIS is sensitive to the parasitic parameter, it is difficult to have exact point-to-point matching between the theory and measurement, especially for the EIS with soldered commercial components. For the p-i-n diode-based EIS, the acceptable differences presented in Figs. 11 and 13 indicate that the theory can be used to predict the real performance approximately and statistically.

2) *Uniformity Factor*: The Smith chart coverage criterion can provide a total number of useful points, but it does not show where those points are distributed on the Smith chart. A high coverage does not guarantee a uniform distribution. An ideal distribution should have a Smith chart coverage as high as possible, at the same time, have a uniformity factor as low as possible. A lower uniformity factor indicates a better distribution on the Smith chart, which can be understood as the same number of impedance points distributed over an equal area. We propose to apply the criterion of a uniformity factor from TMN [6] into the EIS so as to compensate the deficiency of the Smith chart coverage. It is a numerical solution to roughly estimate the uniformity of distribution on the Smith chart; therefore, it also can be used as a restriction condition in optimization. A lower value indicates a better distribution over the entire Smith chart.

The uniformity factor-related calculation process is described as the following. The Smith chart will be divided first into  $N_r$  and  $N_\theta$  subsections from radius and phase directions, respectively (Fig. 14). It should be noted that a

nonuniform division will be done in the radius direction in order to ensure that each subsection has the same area. Then, the number of impedance points  $N(i, j)$  in each subsection will be counted. Finally, the uniformity factor can be expressed by calculating the variance

$$U_F = \frac{\sum_{i=1}^{N_r} \sum_{j=1}^{N_\theta} (N(i, j) - \frac{N_{total}}{N_r N_\theta})^2}{N_r N_\theta}. \quad (13)$$

$N_r$  of 16 and  $N_\theta$  of 64 are chosen to divide the Smith chart from radius and phase directions, respectively. As shown in Fig. 15, the measurement results show a good match with theory.

3) *Maximum VSWR*: In practical applications, it is important to have enough points for each constant VSWR circle, which is useful to check the performance of a DUT by varying the phase while the VSWR keeps constant. The VSWR is larger than 15 for 1.5–2.2 GHz, and larger than 10 for 1.2–1.4 GHz and 2.3–2.5 GHz. In fact, this criterion is not so accurate because of the subjective judgment on the irregular distribution.

4) *Maximum Reflection Coefficient*: The maximum reflection coefficient  $\Gamma$  refers to the radius of the farthest point away from the center of the Smith chart. Compared to the previous three criteria, the maximum  $\Gamma$  is the most meaningless criterion, since it is only one impedance point that carries on a very limited information. Fig. 16 depicts the comparison of required, estimated, theoretical, and measured maximum  $\Gamma$ . As can be seen that the measurement results are close to the theory, both of them are higher than the required  $\Gamma$ . The estimation of maximum  $\Gamma$  using (2) is lower than the

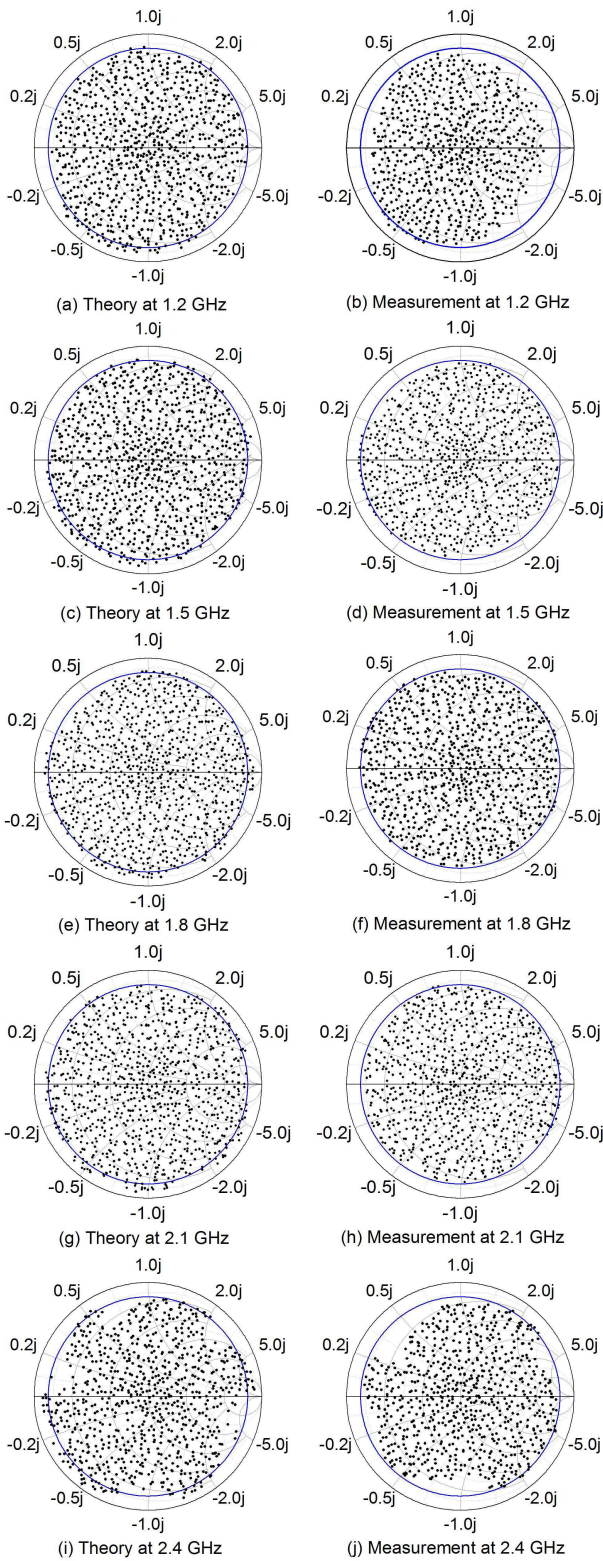


Fig. 13. (a) Measured and (b) theoretical impedances distribution at 1.2 GHz. (c) Measured and (d) theoretical impedances distribution at 1.5 GHz. (e) Measured and (f) theoretical impedances distribution at 1.8 GHz. (g) Measured and (h) theoretical impedances distribution at 2.1 GHz. (i) Measured and (j) theoretical impedances distribution at 2.4 GHz. Blue circle: constant VSWR = 15 circle ( $|\Gamma| = 0.875$ ).

required  $\Gamma$  particularly at low frequency, because the parasitic inductance limits the loading capacitance to 2 pF which is too small at low frequency (Fig. 4). If no restriction is applied to

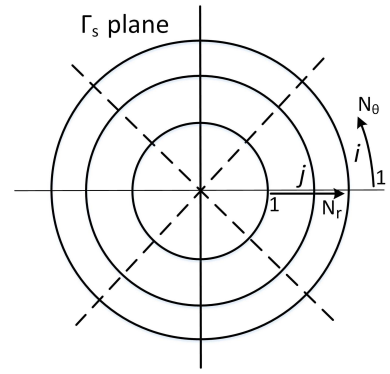


Fig. 14. Division of Smith chart to calculate the uniformity factor.

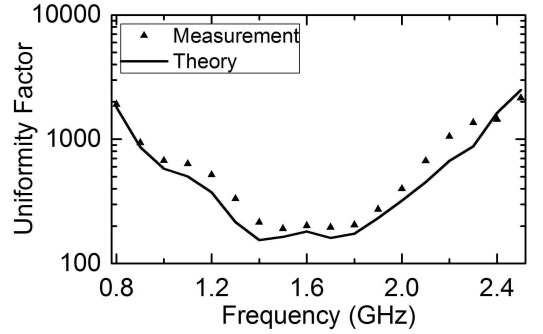


Fig. 15. Comparison of measured and theoretically calculated uniformity factor.

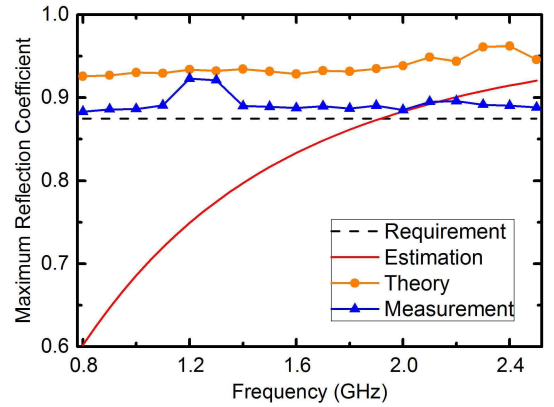


Fig. 16. Comparison of required  $\Gamma$  (black dashed line), estimated maximum  $\Gamma$  (red solid line), theoretical maximum  $\Gamma$  (orange solid line with circle marker), and measured maximum  $\Gamma$  (blue solid line with triangle marker).

the loading capacitance, the estimated maximum  $\Gamma$  should be larger than the requirement.

### B. Bandwidth

Bandwidth describes the frequency range over which a minimum given Smith chart coverage, maximum uniformity factor, and maximum VSWR are satisfied. Bandwidth must not be wide when satisfying these harsh criteria. Nevertheless, we could choose different values for those three criteria according to different applications. For the nonuniform

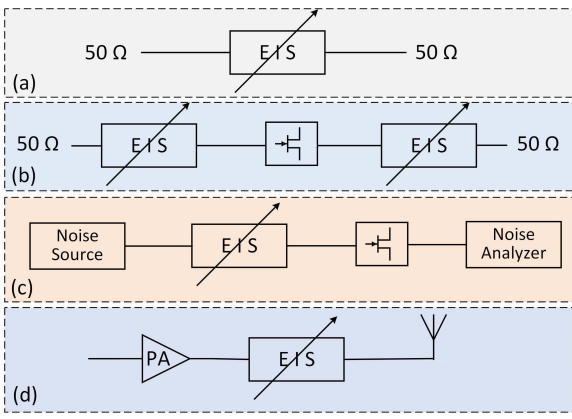


Fig. 17. Four different scenarios to use EIS. (a) Calibration with VNA. (b) Load-pull characterization system. (c) Noise measurement. (d) TMN for reconfigurable PA or antenna.

topology in Fig. 8(d), the bandwidth is 800 MHz when we choose a minimum Smith chart coverage as 60%, a maximum uniformity factor as 500, and a maximum VSWR as 10.

### C. Loss

Three loss definitions, transducer power gain  $G_T$ , power gain  $G_P$ , and available power gain  $G_A$  [39], can be utilized for a mismatched two-port network in either logarithm [1], [2], [6] or linear format [7], [8]. The selection of loss definition depends on the different scenarios as explained in Fig. 17.

Except acting as a one-port variable load, EIS is normally used as a two-port network in four scenarios (Fig. 17). In the calibration process [Fig. 17(a)], the EIS will be connected to a 50- $\Omega$  VNA, then we have  $\Gamma_S = \Gamma_L = 0$ . As discussed in [27], the power gain  $G_P$  is chosen for this scenario

$$G_P = \frac{|S_{21}|^2}{1 - |S_{11}|^2}. \quad (14)$$

When the EIS is used as a load tuner in the load-pull characterization system [right side in Fig. 17(b)], the impedance at the output port of DUT is unknown (but not 50  $\Omega$ ), then we have  $\Gamma_S \neq 0$  and  $\Gamma_L = 0$ . Power gain  $G_P$  only can be calculated and it has the same simplified form as (14). In practical applications, the impedance of the EIS will be swept until the maximum power is detected by the power meter that is placed at the output of the EIS, then we consider the output of DUT and the input of the EIS are conjugation matched. From power gain  $G_P$ , we can estimate the output power from the DUT. In fact, the optimal impedance and maximum power at the output port of DUT are what one expects from a load-pull system. Since the load tuner scenario shares the same loss equation with the calibration scenario [Fig. 17(a)], the loss from the calibration process can be considered as a reference for the load tuner.

In a source tuner scenario [left side in Fig. 17(b)] or noise measurement [Fig. 17(c)],  $\Gamma_S = 0$  and  $\Gamma_L \neq 0$ , we will select the available power gain  $G_A$  that is defined by the ratio of power available from the EIS and power available from

the source.  $G_A$  can be simplified as

$$G_A = \frac{|S_{21}|^2}{1 - |S_{22}|^2} \quad (15)$$

from which we can estimate the power output from EIS or the power input to DUT if the conjugation matching is considered.

When an EIS is used as a TMN for reconfigurable devices [Fig. 17(d)], both sides are probably not 50  $\Omega$ , which means  $\Gamma_S \neq 0$  and  $\Gamma_L \neq 0$ . As discussed in [27], we select transducer power gain  $G_T$  for this scenario

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (16)$$

where

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}.$$

From the above analysis, one knows that the loss is not always describing the power dissipated inside the EIS. As used in most of the works, the definition of (14) is also chosen in this paper for two reasons: 1) it is similar to a real calibration process with both sides terminated by 50  $\Omega$  and 2) although it is not suitable for all the scenarios, it is the only measurable loss compared to others, and the measured results can be used to verify the theory.

The sources of loss of the EIS includes dielectric loss, conductive loss, parasitic  $R_{p-i-n}$  from the p-i-n diode and equivalent resistance of capacitor and connection pads. In addition, parametric studies show that it will be largely affected by the resonance caused by the parasitic inductance and loading capacitance. Fig. 18(a) and (b) shows the theoretical and the measured losses for the selected impedance states at 1.5 GHz. It can be seen that the loss increases with the increase in reflection coefficient because of the multipath loss under high reflection condition. The comparison of measured and theoretical mean loss at different frequencies [Fig. 18(c)] presents a good match between them.

### D. Power-Handling Analysis

Voltage distribution theory has been developed for a uniform distributed EIS [27], a similar theory can be applied to the proposed nonuniformly distributed EIS, and the maximum peak voltage at the position of each diode can be monitored. The voltage distribution of two limiting  $\Gamma$  states, called the highest  $\Gamma$  (0.91) and lowest  $\Gamma$  (0.01), with 0.5 W input power is shown in Fig. 19(a) and (b). Simulations with ADS have been presented to validate the theory, because it is not able to measure the voltage distribution in the real circuit. It can be seen that the theory matches the simulation very well. Due to the inhomogeneous property, the standing wave that presents at the input port (steady state) is not the same as the one existing along the transmission line. In addition, a large peak voltage always occurs at the position of the p-i-n diode with OFF state [27].

The nonlinearity of EIS is mainly caused by those p-i-n diodes with OFF states. A larger maximum peak voltage existing on the transmission line will lead to a lower power-handling capacity. Under a linear operation power,

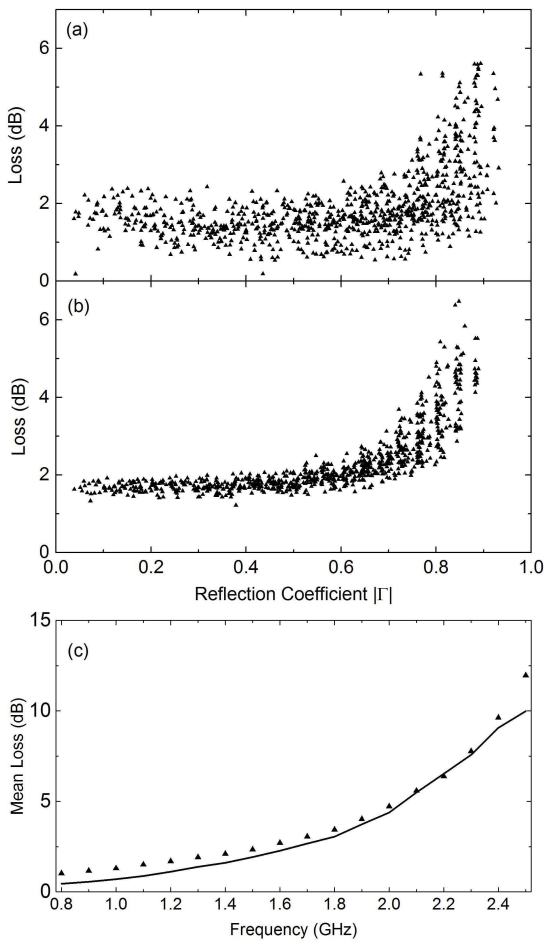


Fig. 18. (a) Theoretical and (b) measured losses for the selected impedance points at 1.5 GHz. (c) Comparison of theoretical and measured mean losses over frequency.

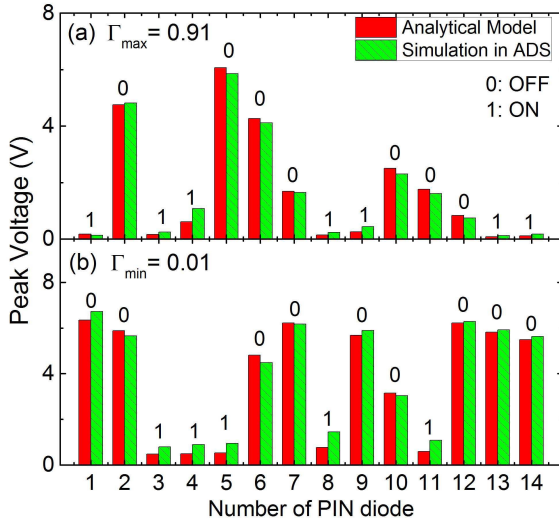


Fig. 19. Comparison of theoretical and simulated voltage distributions along the transmission line under average power of 0.5 W for the (a) highest  $\Gamma$  state ( $|\Gamma| = 0.9$ ) and (b) lowest state ( $|\Gamma| = 0.01$ ).

the maximum peak voltage is proportional to the input power (dBm). The voltage distribution theory has been proven to be able to predict the P1 dB without doing the

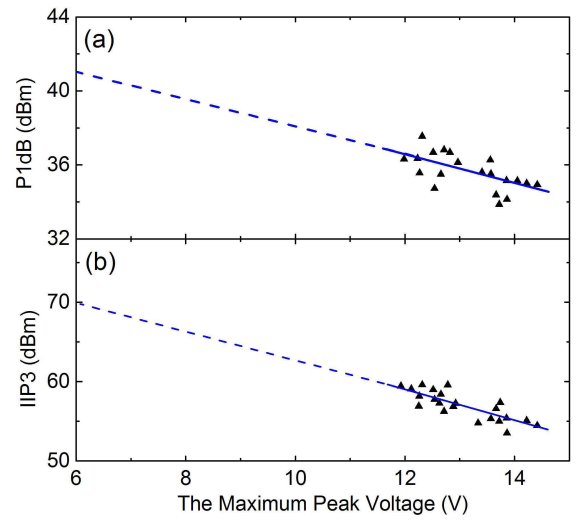


Fig. 20. Simulated relationship of (a) P1 dB and (b) IIP3 with the maximum peak voltage along the transmission line for 20 impedance points under input power of 0.5 W. Solid line: linear fitting curve of the selected 20 points. Dashed line: extension of the fitting curve.

actual power-handling test [27]. As depicted in Fig. 20(a), 20 impedance states with large maximum peak voltage have been chosen for harmonic balance simulation in ADS with input power of 0.5 W. Then, linear fitting (solid line) is applied for the 20 simulations, and the extension line (dashed line) can be used to predict the P1 dB for impedance states with low maximum peak voltage. It shows that the p-i-n diode-based nonuniform EIS has P1 dB higher than 33 dBm. In other words, the EIS can handle the 0.5-W average power linearly. This criterion can be integrated into the optimization, and we can further improve the power handling of EIS by limiting the maximum peak voltage to a certain level (e.g., 14 V).

### E. Nonlinearity Analysis

Ideal EIS should be made as linear as possible. The input third-order intercept point (IIP3) can be applied to express the nonlinearity of EIS [27]. Similar to the prediction of P1 dB, the IIP3 can also be estimated from a small amount of simulation in ADS without doing the actual IMD measurement. As illustrated in Fig. 20(b), the IIP3 of the p-i-n diode-based nonuniform EIS is higher than 53 dBm.

### F. Noise Figure

For any active device, high noise figure stands for significant influence on the noise performance of the system. The EIS will introduce noise to the practical application; therefore, the noise performance of the EIS itself is significant. In this paper, a noise source, noise analyzer, and tuner controller along with an automation program are presented to measure the noise figure of EIS automatically. Fig. 21 shows the results for 816 selected useful impedance states. It can be seen that the noise figure of EIS increases while the reflection coefficient increases. Although the EIS has a maximum noise figure of 17.5 dB at 1.5 GHz, it can be calibrated in the noise

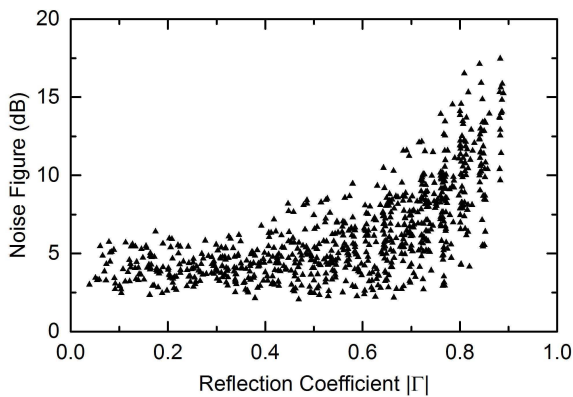


Fig. 21. Noise figure of the proposed nonuniform EIS at 1.5 GHz for 816 selected impedance states.

characterization system without affecting the accuracy of the noise figure test for the DUT.

### G. Other Concerns

1) *Repeatability*: Repeatability indicates the differences of S-parameters among several time measurements for the same impedance state. It shows how well the EIS can repeat each impedance state. The EIS used in the nonreal-time measurement system requires precalibration. Therefore, it is critical for the EIS to repeat the same impedance state, which means that the EIS should be stable. The repeatability test must be done over a large number of impedance states and a range of frequencies to find the worst case. The proposed nonuniform EIS exhibits at least 55 dB repeatability. It will make the test data precise enough when evaluating the PA or radio module.

2) *Tuning Resolution*: Tuning resolution of EIS refers to the resolution of impedance points generated by the EIS. An EIS with a high resolution is important for precision measurements. Traditional EIS exhibits an irregular impedance pattern with unpredictable jumping of impedance states so that it is difficult to have an exact value for tuning resolution. However, the tuning resolution can be described by the predefined density in the discretization process when the Smith chart coverage is calculated.

3) *Tuning Speed*: Tuning speed is the time taken by the impedance synthesizer that moves from one impedance state to the next. The switching time of the selected p-i-n diode is in the order of  $0.1 \mu\text{s}$ , so the switch time of EIS from one state to another is also in the same order. In the precalibrated procedure, the speed is mainly limited by VNA and also the reading via the general-purpose interface bus interface, in the order of 0.1 s. In the real applications, the speed is limited by the controller, which is in the order of 10 ms. Even so, it only needs a few seconds to complete the measurements with 1000 useful impedance states, which is much faster than an electromechanical tuner. In other words, the EIS can be used in the applications where a high measurement throughput is required.

4) *Temperature Drift*: Temperature drift can describe how the performance of EIS changes when temperature varies.

Experiments with thermotank show that when temperature varies from  $-40$  to  $40^\circ\text{C}$ , the repeatability still keeps 50 dB, which means that the EIS works stably when temperature changes in this range.

5) *Cost, Size, Weight, and Easy Integration*: The advantages of EIS compared to the electromechanical tuner and active tuner are its size and weight. They are essentially designed for on-wafer tests. Although the size of EIS in this paper is around  $36 \text{ mm} \times 32 \text{ mm}$ , the whole circuit can be further integrated on the wafer for high-frequency applications if other switching technique, e.g., MEMS, can be adopted.

## VI. CONCLUSION

We have presented a semiclosed-form design procedure for distributed EIS. Initial values and boundaries of multiple parameters have been determined in this procedure. Then, a PSO method is introduced to solve the multiparameter optimization problem of the proposed nonuniform EIS. The effectiveness of the proposed nonuniform topology and the optimization method are validated by experiments. Experimental results show that the proposed nonuniformly distributed topology not only has a better Smith chart coverage but also has a smaller size than a uniform topology. Parametric studies demonstrate that an inappropriate consideration of parasitic parameters can degrade the performance at high frequency. With accurately modeling of parasitics, the measurements of nonuniform EIS present a good match with the theory.

This paper provides a computer-aided design for the nonuniform EIS. The successful utilization of PSO can shorten the development period of an EIS to a few hours. Different criteria can be configured in the fitness function of the optimization process so as to satisfy specific requirements for different applications. Furthermore, comprehensive FOM are studied and summarized, different FOM can be chosen to evaluate the EIS according to their applications. Although we designed a general-purpose EIS in this paper, the PSO and complete list of FOM provide a more freedom in the design of EIS for different purposes.

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