



HAL
open science

A model of GTO compatible with power circuit simulation

Corinne Alonso, Thierry Meynard, Henri Foch, Christophe Batard, Hubert Piquet

► **To cite this version:**

Corinne Alonso, Thierry Meynard, Henri Foch, Christophe Batard, Hubert Piquet. A model of GTO compatible with power circuit simulation. 5th European Conference on Power Electronics and Applications, EPE'93, Sep 1993, Brighton, United Kingdom. <hal-02523157>

HAL Id: hal-02523157

<https://hal.science/hal-02523157v1>

Submitted on 28 Mar 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization



A MODEL OF GTO COMPATIBLE WITH POWER CIRCUIT SIMULATION

C. Alonso, T.A. Meynard, H. Foch, C. Batard, H. Piquet

Laboratoire d'Electrotechnique et d'Electronique Industrielle, U.R.A. au C.N.R.S. n°847, FRANCE.

Abstract. In the field of power device simulation, different approaches can be found. Our purpose is to find models able to represent both the static and dynamic behaviour of semiconductors taking account of the external circuit (in chopper or inverter operation).

These models should be of the "circuit" type to be compatible with a simulation software capable of handling whole converters, like, in our case, SUCCESS.

Our models for minority carrier devices are based on their physical structure. Each junction of the component is represented by a standard junction model. The model of each component is then derived as a combination of these junction models.

In this paper, we will focus on the modelling of the GTO which is a three-junction device. First, we will identify the parameters of each junction with specific tests which will be detailed. Then, the behaviour of the model will be compared with experimental results in conventional conditions.

Keywords. component, PN junction, carriers, GTO, modelling, simulation.

About fifteen years ago, the challenge of simulation in power electronics was to predict and understand the global behaviour of various topologies of converters. A simple binary resistor (R_{on}/R_{off}) was enough to represent the operation of any switching device and determine the main characteristics of a given converter with a very good accuracy (peak and RMS currents, output power, output characteristics,...).

Nowadays, the ever increasing calculation power of computers allows representing the switches more accurately to aid the design of the switching section (design of the snubbers, prediction of the current and voltage overshoots, study and optimization of the losses in the switches ?,...).

However, the modelling techniques are certainly not that advanced ; on the one hand, some physics-rooted models allow predicting the device behaviour but the simulated circuit must be very simple (Leturq (1)), and on the other hand, comportemental models can be used in more realistic circuits but they might be wrong in special operating modes.

Our approach is an attempt to put basic physics in a circuit-type model that could be used in a static converter simulation software.

Works have already been carried out in our team on this subject and a model has been proposed for the PN junction and applied for the bipolar transistor (Batard (2) and Batard (3)). As a first step, we will describe briefly this model of a PN junction. Then, we will show how this model can help modelling a multi-junction component like the GTO thyristor.

PN JUNCTION MODELLING

In power electronics applications the important characteristics of a diode are :

- the low on-state voltage as a function of the forward current I_f ,
- the low reverse current in off-state as a function of the reverse bias,

- the maximum reverse recovery current I_{rrm} at turn-off,
- the vanishing of the current after I_{rrm} (soft or snap-off behaviour),
- the reapplied voltage (dV/dt) at turn-off.

Each of these characteristics is modelled as simply as possible. For example, though it is possible to model the $V(I)$ static characteristics with one or several threshold voltage(s) and a variable series resistor, we will keep the usual R_{on}/R_{off} representation which is acceptable in most of our applications.

What we will try to improve is the representation of the charges which are of high interest in power applications. These charges are represented by a parallel capacitor ; it is well known that the charges are not a linear function of the voltage, which can be interpreted as a variable capacitor. Former studies showed that a two-state capacitor (C_T/C_r) gives a fairly good representation of the variation of the charges versus voltage. To avoid energy discontinuity the commutation between the two capacitors must be done at the very moment when the junction commutates from the on-state to the off-state and vice-versa. For this reason, the model of figure 1 was introduced.

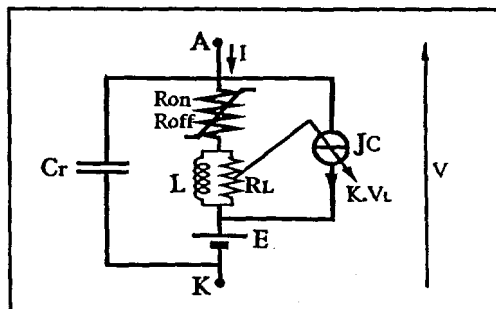


Figure 1 : Model of a PN junction

A very small inductor is connected in series with the binary resistor to create a voltage drop proportional with the

derivative of the current flowing through the resistor, which is in turn proportional with the dV/dt across the device. Controlling a current source by this voltage gives a current in the form of:

$$I = (K L/R_d) * dV/dt \tag{1}$$

Thus, this controlled current source behaves as a capacitor of which value is inversely proportional with R_d (High value when the diode is conducting, low value when the diode is blocking).

It can also be shown that this model allows representing the "softness" of the diode by means of the second time constant L/R_d .

As a conclusion on this diode model, we can say that it gives a very good representation of the current and voltage waveforms in various operating conditions. For example, it has been checked that the reverse recovery current of a BYT08400 was correctly represented (errors < 10%) in a wide region of operation (I_f from 5 to 50 A, dI/dt from 10 to 100A/ μ s). However, it should be noted that a 1% error on the voltage and current waveforms can give errors as high as 100% on the losses ; for this reason this model is not capable of predicting the losses (3).

To a lesser extent, the turn-off dV/dt is also a weak point of this model. Knowing these limits, this kind of models for diodes and bipolar transistors have been intensively used in several research laboratories and already proved their usefulness to understand complicated phenomena and to aid the design of some parts of the commutation section. We will now show that this technique can also be used to create a model for the GTO thyristor.

GTO MODELLING

Basics of GTOs

The operation of GTOs is often explained by means of a two-transistor model as shown in figure 2.

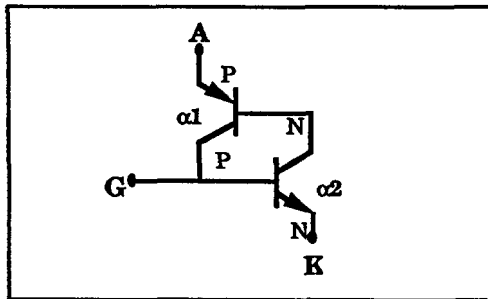


Figure 2 : Two-transistor model of the GTO

The three junctions of the GTO can be considered as forming a PNP transistor with gain α_1 and a NPN transistor with gain α_2 . The main properties of GTOs can be derived from this model.

As an example, it can be seen that α_1 must be very small to obtain an important gain at turn-off, which is the main difference with conventional thyristors. In order to reduce this gain α_1 , two main technologies have been developed : life time control (gold-platinum diffusion or electron-gamma irradiation) and anode shorting.

Principle of the model used for GTOs in our team

A model that is more firmly rooted in the device physics was chosen. In fact, the GTO is composed of three junctions and each of the "external" junction has a certain current gain on the central junction (figure 3).

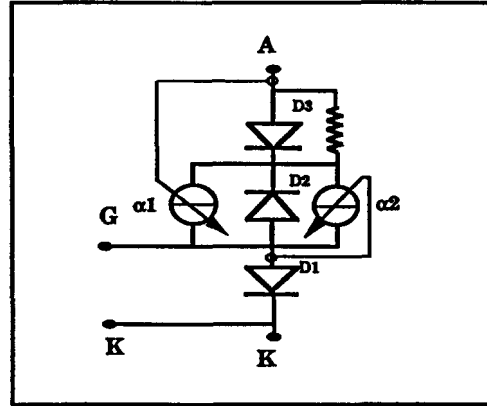


Figure 3 : Three-junction GTO model

To represent each junction and the corresponding charges, the junction model described in section PN JUNCTION MODELLING is used (simplified whenever possible).

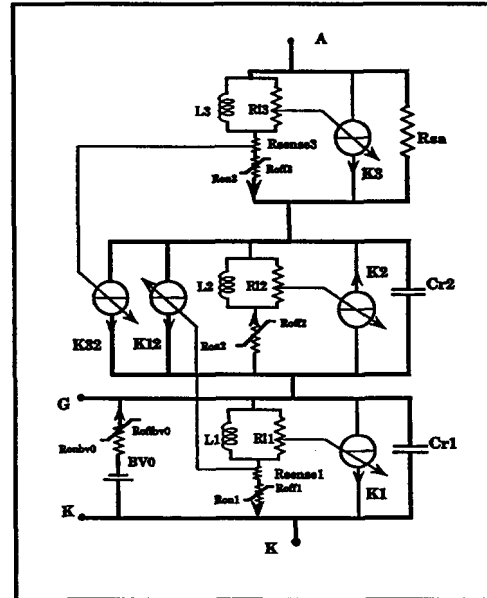


Figure 4 : Whole model of the GTO

In addition, the gains are represented by means of controlled current sources. Only the forward gains are represented here, because at that point of the study, we cannot think of a mode of operation that would activate the reverse gains. At last, avalanching of the Gate-Cathode junction is simply represented by a pure voltage source and a binary resistor. The whole model of an anode-short GTO is given in figure 4.

This piecewise linear model can be considered as a poor representation of the strong non-linearities of real GTOs (3). However, it has the advantage of being directly usable in simulators involving other components modelled with the same precision. It is capable of showing the main phenomena related to GTO commutations such as current tail I_{tail} and spike voltage V_s .

This model (figure 4) is only qualitative. In order to determine all of its parameters, a systematic method has been developed. It will be explained in the next section.

PARAMETERS IDENTIFICATION

Given the number of parameters in the model, a systematic method is needed to determine the model parameters of the GTO. An objective in our method is to identify each parameter separately from the others. So, special tests to evaluate junction by junction the values of the different parameters have been developed.

In this section, these tests and the corresponding parameters identification are detailed. Some of the parameters can be determined by others tests. If they give roughly the same value for a given parameter, the confidence in the parameters model is increased. But they will not be detailed here.

The following method deals with anode-short GTOs. This experimental method cannot be directly extended to gold-doped GTOs because some parameters in the central junction of gold doped GTOs cannot be measured from the terminals.

The GTO under test is rated $I_{TQM} = 600$ A. $V_{DRM} = 1600$ V. Its parameters are determined for a given temperature, namely 25°C.

Identification of the parameters in the anode junction

In a GTO, the measurable quantities are the anode current I_a , the gate current I_g , the anode-cathode voltage V_{ak} and the gate-cathode voltage V_{gk} . The first test is based on these four values.

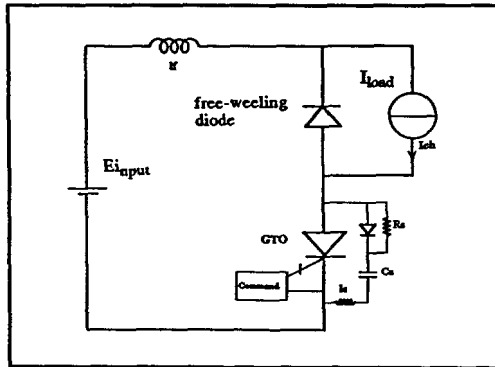


Figure 5 : chopper circuit used for tests

The simplest circuit including switching of a GTO is studied : a chopper (figure 5). The GTO is protected by a 1μF snubber at turn-off. In order to reveal the intrinsic behaviour of the GTO, snubberless operation will also be studied in the following. For this reason, this chopper has to be a high current/low voltage design. The free-wheeling diode used in the chopper is rated $I_{F(AV)} = 300$ A, $V_{RRM} = 400$ V and its Q_{rr} is very low ($Q_{rr} = 4 \mu C$). This

design makes the chopper the worst component of this chopper which is the best way to test the GTO : all the other components can be considered as ideal components.

The turn-off commutation can be represented like in figure 6.

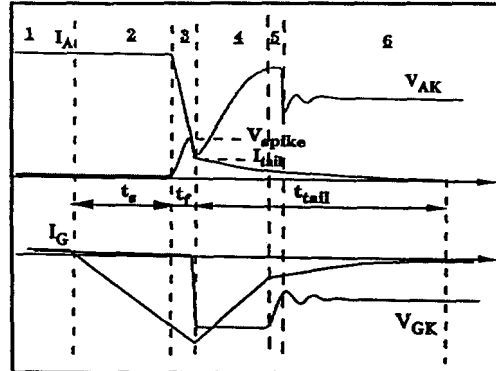


Figure 6 : Turn-off switching under standard conditions

Determining $K3, L_3, R_{13}$. At the beginning of mode 3, V_{ak} appears as the central junction turns off. The beginning of mode 4 is defined as the time when the gate cathode junction turns off. So, during t_{tail} , only the anode junction is conducting and at that time, the charges stored in this junction can be deduced.

With this chopper, several points of operation can be chosen. In this section, the more important is to have the same point for all the tests. We choose $I_{load} = 180$ A with $E_{input} = 125$ V. At this point, $t_{tail} = 7 \mu s$.

It can be seen in the model that : $t_{tail} = 3 (R_{on} + R_{sense3}) C_{f3}$ (2)

with C_{f3} , the forward capacitance representing charges stored in the anode junction.

Its value can be derived from relation : $C_{f3} = K3 * L_3 / R_{on}$ (3)

Substituting for C_{f3} from equation (3) in equation (1), we can determine $K3 * L_3$. L_3 / R_{13} must be a very low time constant. If $L_3 = 1$ nH, we get $K3 = 2330$.

Determining $K32$. Physically, among the carriers injected through the anode junction, those which do not recombine create a reverse current through the central junction. This current gain is represented by α_1 in the model of figure 3 and by a controlled current source J_{32} with its gain $K32$ in the model of figure 4. The relation between them is :

$K32 = 2 \alpha_1 / R_{sense3}$ (4)

To establish this relation, we suppose that the short-circuit resistor R_{sa} and the anode junction $R_{on3} + R_{sense3}$ are equal.

In order to determine α_1 , the same test than before was used. In fact, α_1 can be roughly deduced from figure 6.

During the conduction, the current I_a creates through the central junction a reverse current ($J32$), its value is $\alpha_1 * I_a$.

The value of I_a at the beginning of mode 3 will be noted $I_{a(63)}$. I_a at the beginning of mode 4 will be noted I_{tail} . At this moment, only the anode junction is conducting. As t_f (fall time of I_a) is very small compared to t_{tail} , the current J32 is roughly constant during mode 3. So, I_{tail} can be considered equal to J32. If we measure $I_{a(63)}$ and I_{tail} , we can determine α_1 with the relation (5).

$$I_{tail} \approx \alpha_1 * I_{a(63)} \tag{5}$$

Then, at the chosen point, $I_{tail} = 14,5$ A, $I_a = 180$ A. So, $\alpha_1 = 0,08$.

The values of the anode parameters are listed below :

$R_{on3} = 0,5m\Omega$	$R_{sens3} = 0,5m\Omega$	$R_m = 1m\Omega$
$L3 = 1nH$	$R_{j3} = 100 \Omega$	
$K3 = 2330$	$K32 = 322$	

In addition to the parameters of the anode junction, this test helps deriving the parasitic inductor of the snubber (L_s) from the spike voltage V_{spike} .

With $dI_a/dt = 533$ A/ μs and $V_{spike} = 63$ V, $L_s = 0,12 \mu H$.

For the parameters in the other junctions, more specific tests must be carried out.

Identification of the parameters in the gate cathode junction

To have more information about the physical behaviour, a GTO turn-off switching without protections is studied in the same chopper as in the first test.

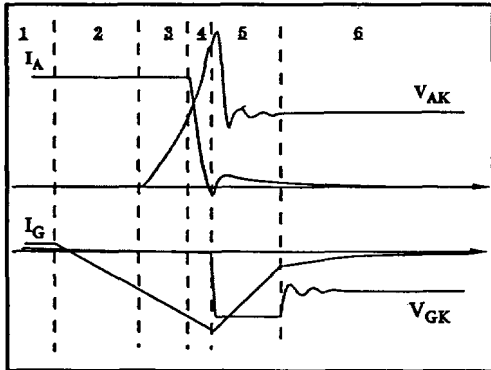


Figure 7 : snubberless turn-off

The overvoltage is now proportional to the load current. The limitation of the overvoltage at turn off without protections for our application is V_{spike} (for this GTO, $V_{spike} = 400$ V). So, a low input voltage like $E_{input} = 125$ V allows snubberless operation of the GTO which is the best way to characterize the GTO itself. The snubberless turn-off is represented in figure 7.

Determining $K1, L_1, R_{j1}$. The determination of the gate cathode parameters can be made if the voltage and the current through the junction are known. The voltage is measured directly at the G and K terminals. But the current must be determined indirectly.

From figure 3, we have :

$$I_a = I_g + I_{D1} = I_k \tag{6}$$

where I_{D1} is the current through the gate cathode junction. In figure 8, I_{D1} is represented with I_a and I_g at the same conditions.

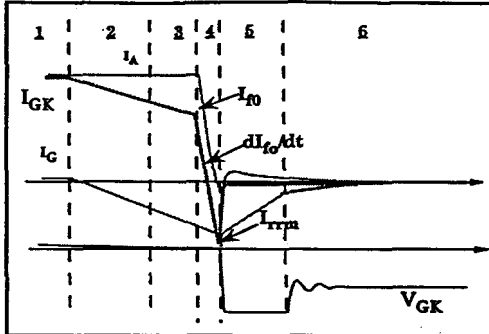


Figure 8 : current and voltage of the gate cathode junction

The waveforms in figure 8 allow the determination of the charges stored in the gate-cathode junction.

$I_{fo} = 180$ A, $dI_{fo}/dt = 711$ A/ μs , $I_{com} = -75$ A.
We fix $L_1 = 1$ nH and $R_{j1} = 100 \Omega$, Then $K1 = 110$.

Determining C_{r1} and C_{r2} . With this type of commutation (figure 7), we can also determine the reverse capacitances of the central junction and of the gate cathode junction. In mode 5 of the snubberless commutation, V_{ak} oscillates. The parasit inductance of the power circuit L_f (figure 5) is determined in others tests. Measuring the period T_2 of the V_{ak} oscillation, the reverse capacitance of the central junction C_{r2} can be determined.

$L_f = 0,35 \mu H$, $T_2 = 218,5$ ns, then $C_{r2} = 3,5$ nF.

A similar process gives the reverse capacitance of the gate cathode junction C_{r1} . The period T_1 of the V_{gk} oscillation is measured in mode 6 and with I_{com} determined before, the value of C_{r1} is determined.

$I_{com} = 0,25 \mu H$, $T_1 = 515$ ns, then $C_{r1} = 27$ nF.

Determining BVO for the gate cathode junction. The value of this breakdown voltage is directly simulated by a voltage source and an ideal diode.
 $BVO = -18$ V, $R_{onbvo} = 0,5$ m Ω , $R_{offbvo} = 10^4 \Omega$

The parameters of the gate cathode junctions are :

$R_{on1} = 0,5$ m Ω	$R_{sens1} = 0,5$ m Ω	$BVO = -18$ V
$L_1 = 1$ nH,	$R_{j1} = 100 \Omega$,	$K1 = 110$
$R_{onbvo} = 0,5$ m Ω ,	$R_{offbvo} = 10^4 \Omega$	

With these parameters, we have all of the gate cathode parameters except the forward gain $K12$ of the current source J12. $K12$ represents directly α_2 .

Identification of the parameters in the central junction

For the central junction, one solution involves forcing this junction to work in the forward mode.

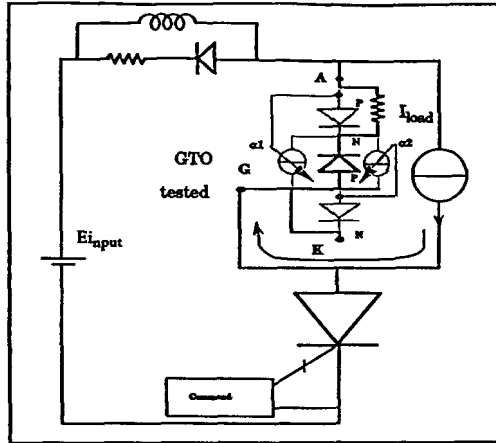


Figure 9 : Chopper circuit modified for determining central parameters

In fact, it is operated as a "free-wheeling diode". Then, the GTO central junction conducts in forward mode while the two other junctions are inhibited.

The experimental set-up is the same chopper in which the free-wheeling diode is replaced with the GTO thyristor. The global circuit is represented in figure 9. To neutralize the gate cathode junction, it is short-circuited as close to the case as possible. Then, the current inside the GTO is forced so that it flows through the central junction and the anode short. It should be noted that the anode and gate junctions are not conducting so that the gains are not activated. The dI/dt is limited by a series inductor and load current is 10 A (a rough estimation of the current flowing through the central diode of the model in normal operation).

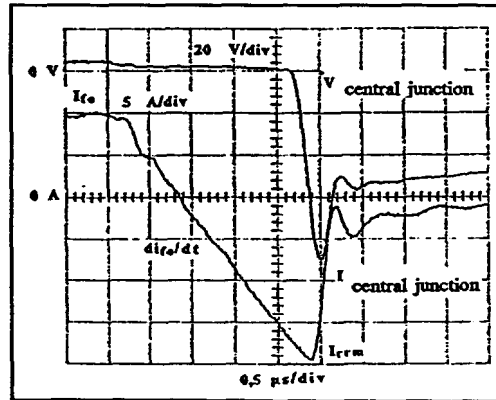


Figure 10 : Current and voltage through the central junction

The experimental current and voltage are shown in figure 10. The maximum reverse recovery current $I_{rmm} = -20$ A and the "softness" time $t_f = 0,25 \mu s$ corresponding to the initial current $I_0 = 10$ A and a dI/dt of $13,3$ A/ μs allow determining L_2 , R_{12} and K_2 of the central junction D_2 .

We obtain:

$$\begin{matrix} R_{on2} = 0,5m\Omega & R_{off2} = 10^5\Omega & t_f = 0,25\mu s \\ L_2 = 1nH & R_{12} = 4m\Omega & K_2 = 2900 \end{matrix}$$

Identification of the static forward gains

The last model parameter to be determined is K_{12} . For that, a static test is carried out (figure 11). When the GTO unlocks, we can determine the static gain G_s . The power circuit drawn in figure 11 is realised for this test.

The GTO is initially turned on by a positive gate current delivered by an auxiliary circuit (not shown in figure 11), so that current I_a flows through the GTO. Then, a small DC current is extracted from the gate and slowly increased. At a certain level of current (I_{glim}) the GTO turns-off and current I_a flows through the three series-connected diodes that limit the voltage across the GTO to approximately 5V.

Theoretically, when D_2 turns off, we obtain from model figure 3, the relation between G_s , α_1 and α_2 is :

$$G_s = I_{glim}/I_a = (\alpha_1 + \alpha_2 - 1) / \alpha_2 \quad (7)$$

With $I_a = 180$ A, we measure $I_{glim} = 18,5$ A. So $G_s = 0,103$.

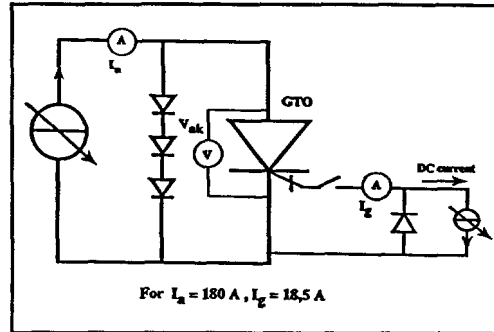


Figure 11 : Static power circuit

To reduce the on-voltage drop of the GTO, the sum $\alpha_1 + \alpha_2$ must be maximized. However, α_1 must be as low as possible to limit the current tail. (see section Basics of GTOs). So, α_2 must be close to 1. Assuming $\alpha_2 = 1$, gives $G_s = \alpha_1 = 0,10$. This value is to be compared to that derived from the current tail measurement ($\alpha_1 = 0,08$). The difference between these two values (roughly 20%) can be easily explained by the measurement of I_{tail} which is very difficult to achieve (offset, rindings, ...).

The values used in the simulation presented in the following section are :

$$\begin{matrix} \alpha_2 = 1, & \alpha_1 = 0,08, \\ K_{12} = 2000, & K_{32} = 322. \end{matrix}$$

Identification conclusion.

We have determined all of the GTO model parameters in this part. The second point of the study is the global validation of the model. So we fix the model with its parameters and we place this model in its simulation environment.

In the next section, we describe how we validate the model and its limits. It should be noted that the parameters of the model used are those given by the method described above and they are never modified to achieve some sort of "curve-fitting".

EXPERIMENTAL AND SIMULATED WAVEFORMS COMPARED.

First, we validate the model at the same point chosen for the parameters identification. Then with fixed parameters, several simulations are made at different voltage and current levels. Finally, we compare the experimental and simulation results.

For example, a turn-off of the real GTO and its corresponding simulation are represented in figures 12 and 13. Figure 12 displays the experimental results obtained at turn-off with a snubber. This is achieved at 125 V input voltage and 180 A load current. The initial di_g/dt is 40A/ μ s, and I_{rrm} is equal to 75A. This can be considered as a fast turn-off with a turn-off gain of only 2. The snubber is composed of a 1 μ F capacitor and a 15 Ω resistor.

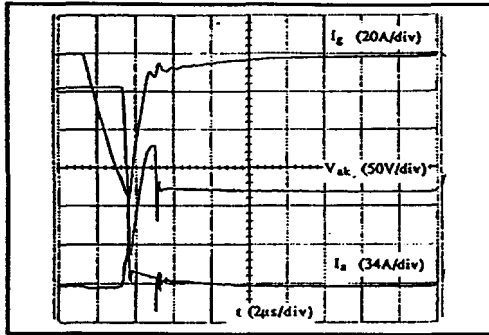


Figure 12 : Experimental turn-off of a GTO

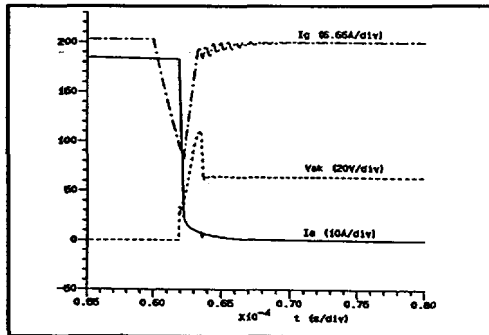


Figure 13 : Simulation turn-off of a GTO

Figure 13 shows the turn-off simulation results obtained with a 1 μ F snubber, $I_{load} = 180$ A, $E_{input} = 125$ V. As can be seen from these waveforms, the main phenomena are represented and have a reasonable amplitude.

With the different simulations made, we can directly compare simulated current and voltage values with experimental results. For example, we have :

$$\begin{aligned} di_g/dt_{simul} &= 560 \text{ A}/\mu\text{s}, & di_g/dt_{exp} &= 525 \text{ A}/\mu\text{s}; \\ I_{rrmsimul} &= 75 \text{ A}, & I_{rrmexp} &= 70 \text{ A}. \end{aligned}$$

The figures 14 and 15 sum up the behaviour of several variables over a wide region of operation. For the snubberless operation a similar study is made with experimental and simulated results compared.

The simulated current values like di_g/dt and I_{rrm} have a good behaviour. The difficulties are in the representation of the dV/dt at turn-off in relation to the reverse capacitor.

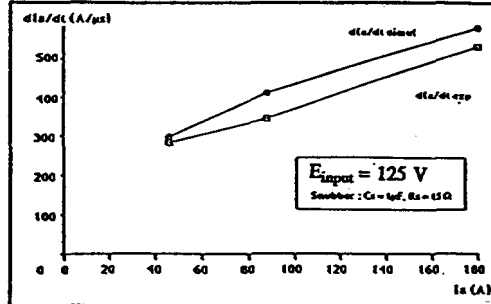


Figure 14 : Experimental and simulated di_g/dt compared

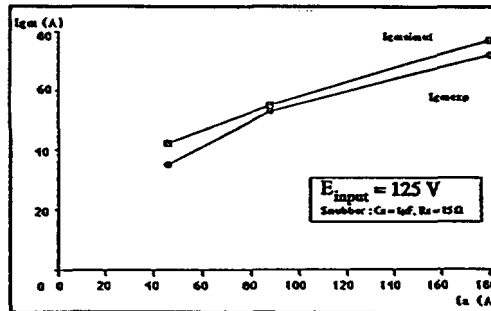


Figure 15 : Experimental and simulated I_{gm} compared (I_{rrm})

CONCLUSION

We can say that most quantities are in agreement with experimental results but there remains certain difficulties concerning dV/dt s in snubberless operations. This particular operation is not used in conventional operation, in particular when it is necessary to optimise the power circuit. Presently, we cannot have a good idea of losses but can predict the global behaviour.

REFERENCES

1. Leturq, Ph., Khatir, Z., Gaubert, J., 1989, Recherche Transport Sécurité. juin 89. "Simulation des thyristors Gate-Turn-Off."
2. Batard, C., Meynard, T.A., Foch, H., Massol, J.L., 1991, Congrès EPE 91 Florence. "Circuit-oriented simulation of power semiconductor using SUCCESS. Application to diodes and bipolar transistors."
3. Batard, C., 1992, Thèse de docteur de ITNP Toulouse. "Interactions composants-circuits dans les onduleurs de tension. Caractérisation-Modélisation-Simulation."
4. Pascal, J.P., 1986, Thèse de doctorat d'état es Sciences Physiques présentée à l'université Pierre et Marie CURIE. Paris VI. "Etude des circuits d'aide à la commutation de thyristors GTO montés en série pour des applications à la traction ferroviaire."