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Influence of different peripheral protections on the breakover voltage of a 4H-SiC GTO thyristor

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4H-SiC asymmetrical gate turn-off (GTO) thyristors have been developed using a PP-NP+ epitaxial layer structure, where P is a 35 μm thick p-type drift layer doped at $5 \times 10^{14} \text{ cm}^{-3}$. The process sequence, described in details elsewhere, uses plasma etching steps (ECR and RIE) in order to expose interdigitated devices with a recessed gate structure. Knowing the difficulty in reaching the theoretical forward blocking capability of $V_b = 6 \text{ kV}$, determined by numerical simulations using the finite element code MEDICITM, three different device terminations are realized. The first and simplest termination used is a MESA etched down to 12 μm deep into the drift layer. Better performance was expected by using a combination of MESA and Junction Termination Extension (JTE), but unfortunately, the JTE implantation was not well adjusted. Finally, etched guard ring (EGR) terminations are realized etching five 2 μm wide grooves around the device periphery through the n-base layer. The electric characteristics of the devices with all the three terminations are presented and discussed using the results of numerical simulations. The highest breakover voltage measured amounts to 4.0 kV, approaching the theoretical limit of $0.63 \cdot V_b$, calculated for plane parallel junction.

Today, at ISL, there are pulsed power applications under investigation which handle electric energies up to 10 MJ using spark gaps or silicon based high power semiconductors as switching elements [1]. Since silicon based technology is reaching its physical limits concerning blocking and power handling capability, for compact future military pulsed power systems we are investigating GTO thyristors based on SiC [2, 3]. Like others we are motivated by some excellent results for Schottky diodes [4], thyristors [5] and bipolar diodes [6]. Reaching breakdown voltage of 19 kV, the potential of SiC based devices appears very interesting.

According to preparatory device simulations using the finite element code MEDICI™, the GTO-thyristors developed should be capable of blocking $V_b = 6$ kV. The n-type 4H-SiC wafer material was purchased from Cree, including a PP-NP₊ (from the wafer up to the top) epitaxial layer structure, where p- is a 35 μm thick p-type drift layer doped at $5 \times 10^{14} \text{ cm}^{-3}$ (Fig 1). Finally 10 mm by 10 mm samples with up to 50 interdigitated GTO thyristor structures, having an anode area ranging from $0.7 \times 10^{-3} \text{ cm}^2$ to $5.7 \times 10^{-3} \text{ cm}^2$, have been processed at Aachen University. The process sequence is described in details elsewhere [2, 3]. In this paper we concentrate on the three different device terminations applied (figure 2), namely etched guard rings (EGR), mesa and a combination of mesa with additional single zone Junction Termination Extension (JTE). The different samples processed vary not only in the type of termination applied but also in the parameters: EGR/ mesa etch depth W_{etch} and thickness of the passivation oxide d_{ox} . As it can be seen in figure 3, simulation results indicate that in order to obtain a 5 kV breakover voltage we have to etch in excess of 20 μm . For the ECR reactive ion etching process used, the etch rate is around 200 nm/min, so it requires a long time to obtain an etch depth equals to 20 μm . Some tests have been realized and show the effect on the electrical characteristics.

The electrical characterisation has been performed at CEGELY using either the custom-built set-up described in figure 4 for static characteristics or a Tektronix 370A curve tracer with a custom-built gate driver for on-state tests. The static characterisation used to evaluate the breakover voltage is based on a 12.5 kV high voltage source delivering a maximum current of 0.6 mA (due to protective resistor). Figure 5 shows the breakover voltage attained for the 3 different terminations. The highest breakover voltage measured amounts to 4.0 kV for the mesa protection. According to the simulation results, shown in figure 3, for $W_{\text{etch}} = 12 \mu\text{m}$ and $d_{\text{ox}} = 1.5 \mu\text{m}$ we expect a breakover voltage around 4.8 kV. Thus the devices reach about 83% of the calculated limit. The difference could be explained by the density of defects at the oxide/semiconductor interface, which in the simulation had been ignored. In the final paper, we will discuss the characteristics obtained for all terminations comparing with the results of numerical simulations. Figure 6 is showing on-state characteristics obtained with the curve tracer by switching EGR terminated GTO thyristors with a gate current pulse of 9 mA into the on-state. For an on-state current of 1.3 A the device reveals a voltage drop of 13 V. Using an anode area of $3.8 \times 10^{-3} \text{ cm}^2$ the maximum current density reached equals to 343 A/cm².

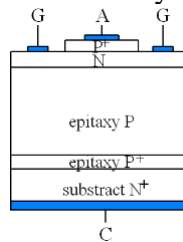


Fig 1. Cross section of the recessed gate thyristor structure with a pp-np+ epitaxial layer structure.

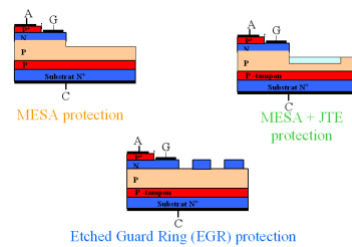


figure 2. The three different peripheral protections used for the 4H-SiC GTO thyristors.

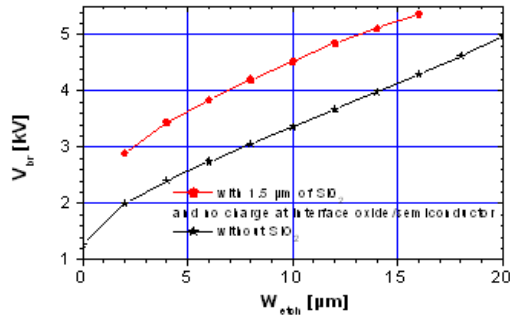


figure 3 : Breakover voltage versus mesa etching depth W_{etch} with and without field oxide calculated for the forward blocking p-n junction using MEDICI™.

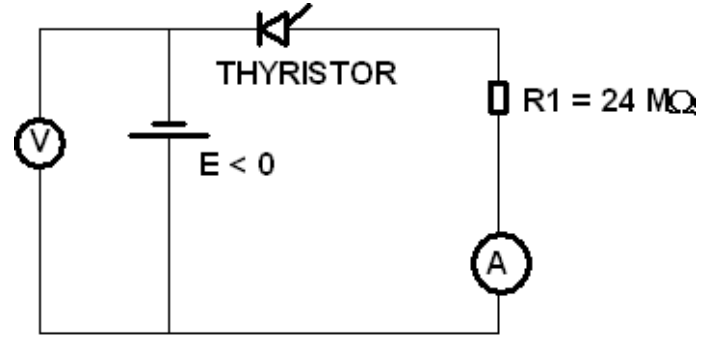


figure 4 : Set-up based on a 12.5 kV high voltage source (HVS) used to measure the breakover voltage of the SiC-thyristors.

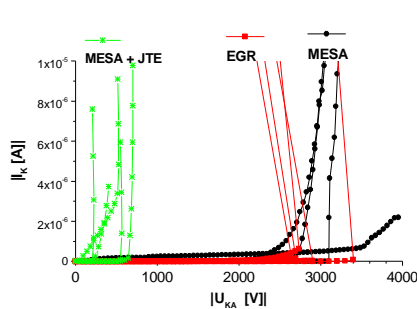


Figure 5 : Typical current voltage characteristics in forward blocking mode for thyristors with three different terminations.

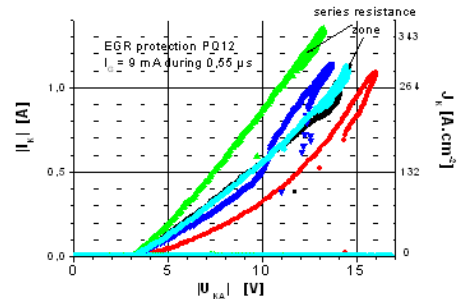


figure 6 : On-State characteristics obtained with the curve tracer.

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