Electrothermal simulations of silicon carbide current limiting devices

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Abstract– **SiC is a semiconductor material that could satisfy the requirements of electrical protective devices. This work presents two devices as current limiters for serial protection application. The first device structure is a vertical power MOSFET-like with an existing N channel. The second is a LVJET with buried p-wells and an additional gate electrode. Their electrical performances were simulated with ISE TCAD tools. A study of their electrothermal behavior is presented, demonstrating the SiC superiority over silicon with regards to this field.**

Index terms— SiC, current limiting device, serial protection, electrothermal simulation, power electronics.

1 Introduction

Silicon carbide (SiC) is a very promising semiconductor material for high temperature, high voltage and also high power applications [1, 2] that can push away the limits of the semiconductor power devices. Specific devices like Fault Current Limiters (FCL) could take advantage of the excellent silicon carbide properties (band gap energy of E_G = 3 eV ; critical electric field of E_c = 2 MV.cm^{-1} ; thermal conductivity at 300 K of λ = 4.9 W·K^{-1}cm^{-1}). Current limiters could be used for serial protection in almost the full range of power applications, from domestic energy distribution market up to traction. I-V characteristics have been simulated with finite element software ISE-DESSIS [3]. For the structures optimized for specific applications, electrothermal simulations have been realized to take into account self heating. Then, two batches of SiC devices have been realized, with two electrode devices in the first run (Accu-MOSFET structure) and three for the second one (Lateral Vertical JFET structure). Electrical characterizations of these devices are also presented in this paper.

2 Basics on serial protection

The place of a serial protection (SP) device inside the circuit is shown in Fig. 1. During normal operation, resistance of this device should be as low as possible, but in case of load failure, current should be limited to a given value under high voltage. Therefore heat power will be generated inside the SP device and temperature will increase quickly. Thanks to its excellent physical properties SiC is well suited for this protective application.

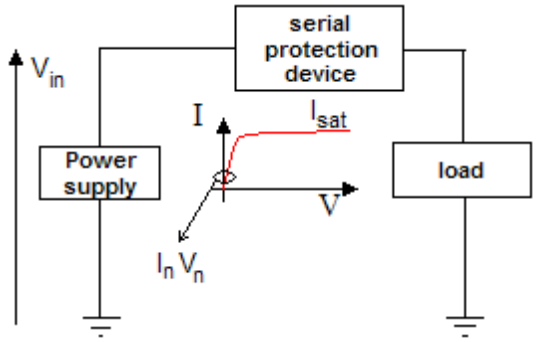

Fig. 1: An usual way to protect the load against overcurrent due to short circuit failure. Expected I-V characteristic of the protective device together with nominal and saturation currents are shown.

3 Accu-MOSFET structure

The design is based on the vertical power MOSFET structure described in [4] with an implanted channel (N type channel) as shown in Fig. 2. The epitaxial layer (6 μm/10^{16} cm^{-3}) is calculated to withstand 600 V. The channel is defined between the P$^+$ buried layer and the SiC/Oxide interface. The periphery protection of the device is realized by guard rings. The device is normally on. During normal operation, current flows from drain to source under low V_{DS} bias. When V_{DS} increases up to V_{in} due to load failure, depletion regions are stretched into the channel and will then reduce channel width. Both this reduction and the self-heating effect can limit and even reduce the current flow inside the device (due to a mobility reduction with increasing temperature).

Electrothermal simulations were performed with ISE-DESSIS to study the effects of the channel technological parameters (doping level, length and depth) on the electrical behavior of the device.

The parameters of the models used for the simulations are presented in Table 1. They are suited to

4H-SiC. The carrier mobility model used is a doping and electric field dependent model [5]. In the electrothermal 2D simulations which have been performed, we took into account the effects of the temperature on carrier mobility [5 - 7], carrier concentration [7], thermal conductivity [8, 9] and ionization coefficients [10].

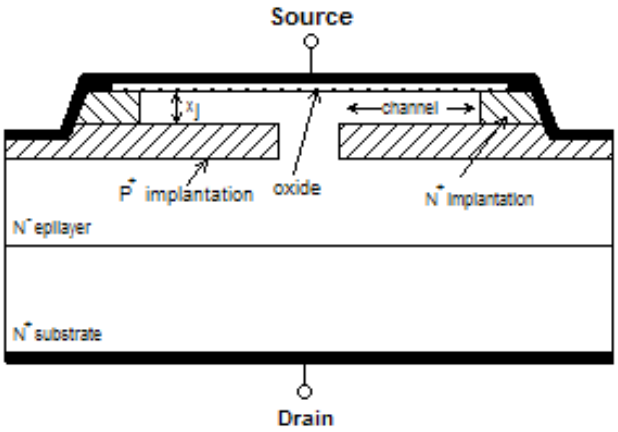

Fig. 2: Cross-sectional view of the current limiting structure based on Accu-MOSFET.

Electron mobility model:

$$\mu_{dop} = \mu_{min1} e^{\frac{P_c}{N_i}} + \frac{\mu_L \left(\frac{T}{300}\right)^{-\xi} - \mu_{min2}}{1+\left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_i}\right)^{\beta}}$$

Parameter	4H-SiC
μ_{min1} [cm²/V.s]	20
μ_{min2} [cm²/V.s]	0
μ_L [cm²/V.s]	700
ξ	3
μ_1 [cm²/V.s]	0
C_r [cm⁻³]	4.5×10¹⁷
α	0.45
C_s [cm⁻³]	3.43×10²⁰
β	2
P_c [cm⁻³]	0

$$\mu(E) = \frac{\mu_{low}}{\sqrt{1+\left(\frac{\mu_{low} E}{v_{sat}}\right)^2}} \qquad v_{sat} = v_{sat,0}\left(\frac{T}{T_0}\right)^{-v_{sat,e}}$$

Parameter	4H-SiC
v_{sat} [cm/s]	2×10⁷
$v_{sat,exp}$	0.5

Impact ionization model:

$$\alpha = \gamma a \exp\left(\frac{-\gamma b}{E}\right) \qquad \text{with} \quad \gamma = \frac{\tanh\left(\frac{\hbar\omega}{600k}\right)}{\tanh\left(\frac{\hbar\omega}{2kT}\right)}$$

Parameter	4H-SiC
$a_{n,p}$	3.09×10⁶ cm⁻¹
$b_{n,p}$	1.8×10⁷ V/cm
Eo	4×10⁵ V/cm
$\hbar\omega$	0.09 eV

Thermal conductivity:

$$\lambda(T) = \frac{1}{a + bT + cT^2}$$

Parameter		4H-SiC
λ	a	0.01 K.cm/W
	b	6×10⁻⁴ cm/W
	c	6×10⁻⁷ cm/W.K
C		3 J/K.cm³

Table 1: 4H-SiC parameters used in models of mobility, impact ionisation and thermal conductivity, introduced in ISE-DESSIS simulator tool.

3.1 Static characteristic

The figure 3 shows simulated characteristics for different Accu-MOSFET structures with different channel depths (X_j ranging from 0.15 μm up to 0.4 μm). A saturation (limiting) current regime occurs at a threshold voltage which depends on the channel depth parameter. For a given value of x_j = 0.3 μm, a saturation current density (J) of 1500 A/cm□ and a specific on-resistance equals to 10 mΩ.cm□ are obtained. For comparison with silicon, a 600 V structure requires an epitaxial layer of 45 μm/10^{14} cm^{-3}, that gives a $R_{drift}=W_{epi}/(nq\mu_n)\approx$250 mΩ.cm□. This result does not take into account the electrothermal effect.

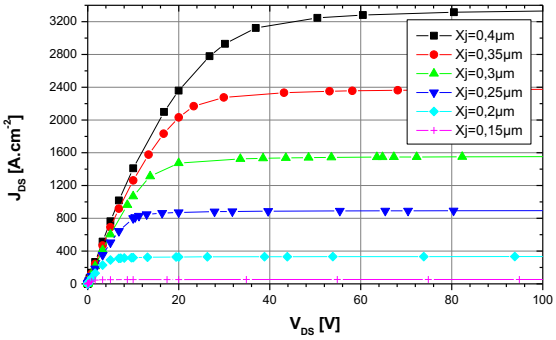

Fig. 3: Static J-V curves at T=300 K (channel depth Xj ranging from 0.15 μm up to 0.4 μm; channel length=4 μm ; channel doping level=2×10^{17} cm^{-3}; distance between P-wells = 10 μm)

3.2 Electrothermal simulation.

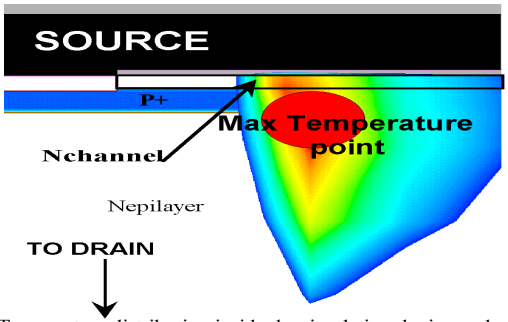

Fig. 4: Temperature distribution inside the simulation device under V_{DS} = 500 V (channel length = 3 μm, channel doping concentration N = 2.5×10^{17} cm^{-3}, channel depth = 0.2 μm).

In case of current surge, the current limiting device has to operate under current and high voltage simultaneously. Therefore, the self-heating of the device generates high temperature spot (see fig. 4) located at the end of the channel, close to the SiC/oxide interface and could induce a thermal runaway failure.

Figure 5 shows an example of the current density versus time and the corresponding maximum temperature inside the device. The V_{DS} waveform is a 500 V/ms ramp during the first millisecond and then a constant bias (500 V). When the temperature increases, the carrier mobility starts to decrease and leads the current to do the same. Then, the stress of the oxide layer is quite important: high electric field (≈5 MV/cm) and high temperature (600 K). Figure 6 shows the average power losses in the device versus time under the same conditions

as previously. The power reached after 1 ms is 80 kW/cm□ and seems to saturate as the current decreases. The device keeps a good behavior even under such high temperature conditions, with a steady state value equal to 920 K.

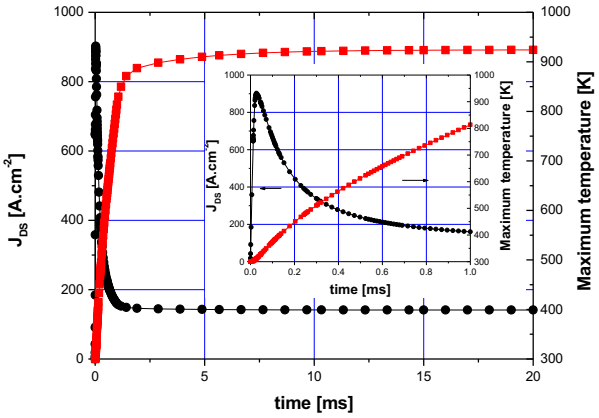

Fig. 5: Current density and the maximum temperature inside the device versus time during a 500 V/ms V_{DS}-ramp. (channel depth=0.3 μm ; channel length=4 μm; doping level=2×10^{17} cm^{-3}, T_A=300 K, R_{TH}=0.5 K.cm□/W at the backside, R_{TH}=∞ at the topside). The inserted figure is a zoom of the first millisecond part.

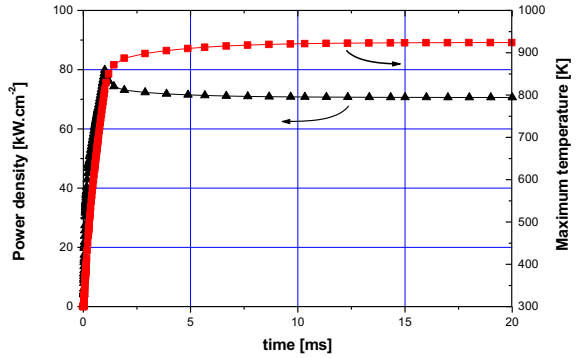

Fig. 6: Average power losses versus time.

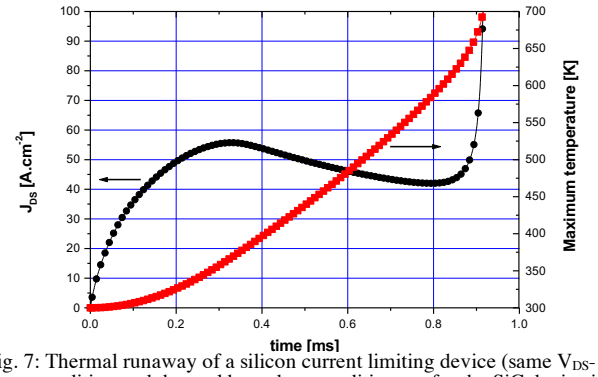

Fig. 7: Thermal runaway of a silicon current limiting device (same V_{DS}-ramp condition and thermal boundary conditions as for the SiC device in Fig. 5).

For comparison with the silicon case, we studied a similar structure with simulation tool only, as there is no commercial silicon current limiting device. The structure was optimized to operate in the range of 20 A/600 V. The silicon device is a power MOSFET with an implanted channel [11], the low doped region is optimized for 600 V (45 μm/10^{14} cm^{-3}). The same thermal boundary condition as for the SiC device is applied for the silicon device: R_{TH}=0.5 K.cm□/W. The resulting saturation current is 60 A/cm□ (figure 7). Contrary to the SiC structure, after 0.9 ms, the internal temperature is so high that a thermal runaway would occur and destroy the silicon device.

To take into account the thermal environment of the semiconductor, different features of heat-sink have been considered. Fig. 8 shows a description of current limiter with different layers (copper and/or ceramic) added on top and back side. R_{TH} is the thermal resistance with respect to the external ambient temperature. The thermal conductivity [3.98 W.cm^{-1}.K^{-1} for copper and 0.167 W.cm^{-1}.K^{-1} for ceramic] and the thermal capacitance [3.42 J.cm^{-3}.K^{-1} for copper and 2.78 J.cm^{-3}.K^{-1} for ceramic] of the heat-sink are considered.

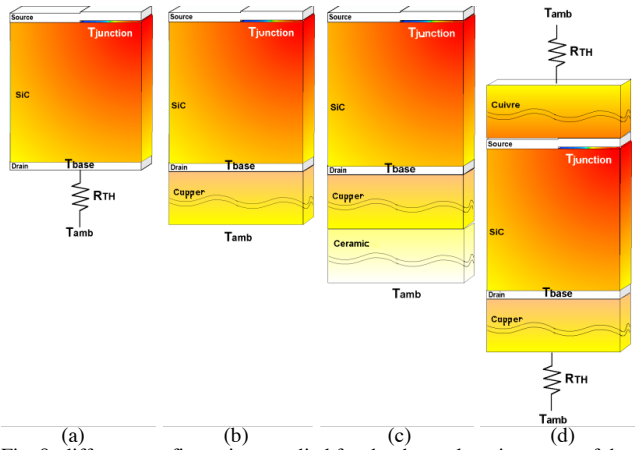

Fig. 8: different configurations studied for the thermal environment of the device : a) R_{TH} (0.1 K.cm^2.W^{-1}), b) copper layer (1 mm), c) copper and ceramic layers (1 + 1 mm), d) sandwich with copper layer (1 mm) and R_{TH} (1 K.cm^2.W^{-1}) on both sides.

Simulations results are shown on Fig. 9. Small changes can be observed between copper layer and thermal resistance. The best case is obtained with sandwich which is normal because heat is exhausted on both sides. Then, the junction temperature in SiC increases up to 820 K after 10 ms.

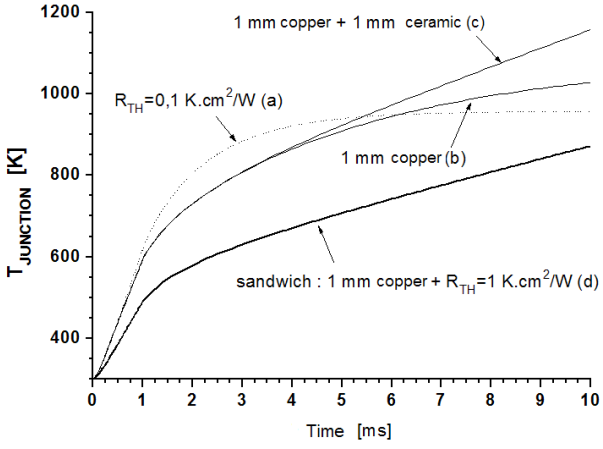

Fig. 9: Maximum junction temperature in the device versus time for different conditions.

Fig. 10 presents temperature distribution in the structure presented in Fig 8 (d) taken at different moments. Symmetrical spreading is due to similar value of thermal conductivity of SiC and copper.
This configuration is closed to the press-pack technology for packaging the current limiter.

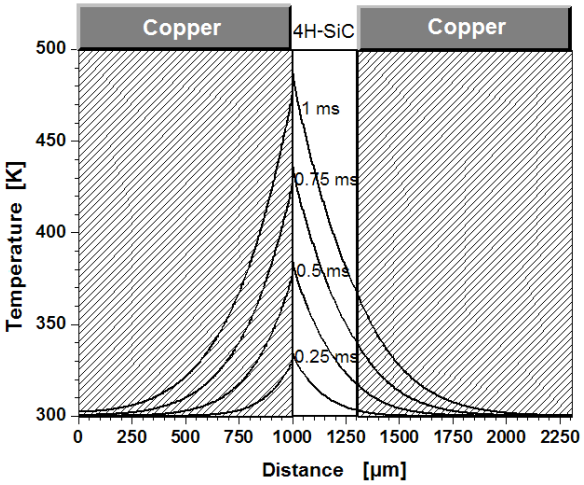

Fig. 10: Temperature distribution in SiC and copper layers on both side of the current limiter.

Although SiC can sustain high working temperature, surge current should be time limited to avoid failure in the neighboring layers.

3.3 Experimental results.

The 4H-SiC wafer used for the fabrication was purchased from CREE Research Inc. It is composed by a N^{++} substrate (ρ=20 mΩcm / 430 μm) and a N type epitaxial layer (4.1×10^{15} cm^{-3} / 7 μm). The detailed process given in [12] requires 6 mask levels. For the mask design, a hexagonal multicell structure was defined.

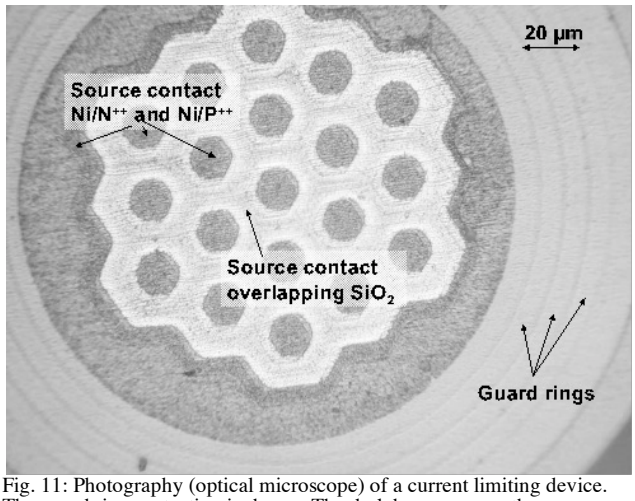

Fig. 11: Photography (optical microscope) of a current limiting device. The guard ring protection is shown. The dark hexagons are the source contact part that reach the SiC N^{++} surface, the white parts (between the dark hexagons) are the source contact that overlay the oxide layer.

The electrical characterizations are made with a curve tracer Tektronix 370. The devices are tested with probes. The results are shown in figure 12. The simulated J-V characteristic (using technological projected data) is also plotted on the graph for comparing with the real J-V curve. We find a good match between the simulation curve and the real curve in the case of a step-by-step measurement.

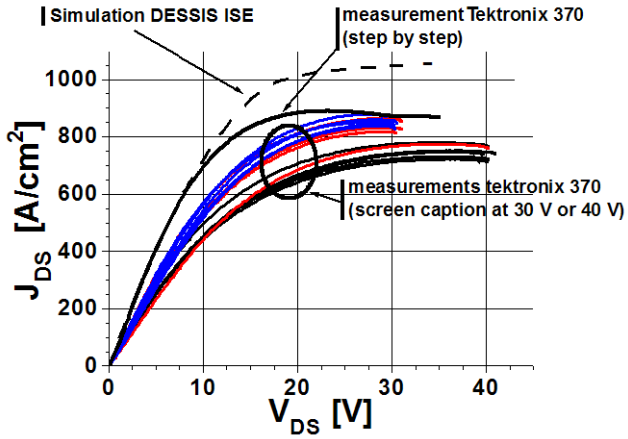

Fig. 12 Experimental and simulated J-V characteristics of current limiting device with 4 μm for the channel length value. The saturation voltage is 15 V. The current density is calculated considering the entire source contact area.

This fabricated Accu-MOSFET has a specific on-resistance of 13 mΩ.cm² and can sustain a 600 V forward bias, which place it as one of the best device in this range of voltage [13].

4 Lateral Vertical JFET structure

Based on the same principle, the additional gate electrode of the JFET structure [14] (shown in Fig. 13) allows to modulate the saturation current during active mode. P-wells are realized by ion implantation with higher energy, which determines a deeper channel (x_j = 0.6 μm).

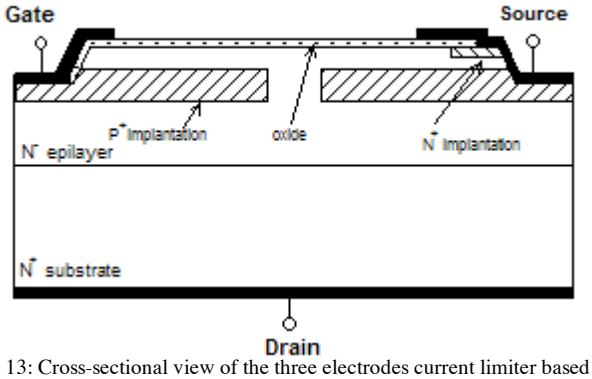

Fig. 13: Cross-sectional view of the three electrodes current limiter based on a VJFET structure.

4.1 Static characteristic

Static simulations have been carried out to optimize geometrical parameters of the LVJFET.
Figure 14 shows simulated electrical characteristics depending on the geometry of the device (channel length L, and inter-P wells spacing S). Simulations are based on the same physical models as described previously.

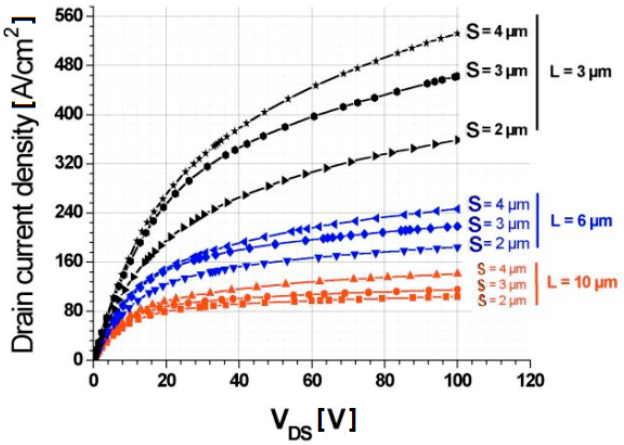

Fig. 14: Simulated static J-V characteristics on LVJFET current limiter.

4.2 Electrothermal simulation.

As in the case of the Accu-MOSFET structure, the current limiting device has to operate under high current and high voltage simultaneously. Figure 15 presents both the current density distribution within the device and temperature repartition.

As in the case of the Accu-MOSFET, we can see a hot thermal point closed to the vertical channel, where current density is at its maximum value (10^4 A/cm^2).

Therefore, electro-thermal transient simulations were done to estimate a safety operation area of the device. A step voltage of 400 V was applied to the device for various rising times (4 μs, 60 μs, 0.1 ms, 1 ms, 10 ms).

A maximal working temperature of 900 K was set, Figure 16 shows the maximum temperature and current density reached at the end of this pulse.

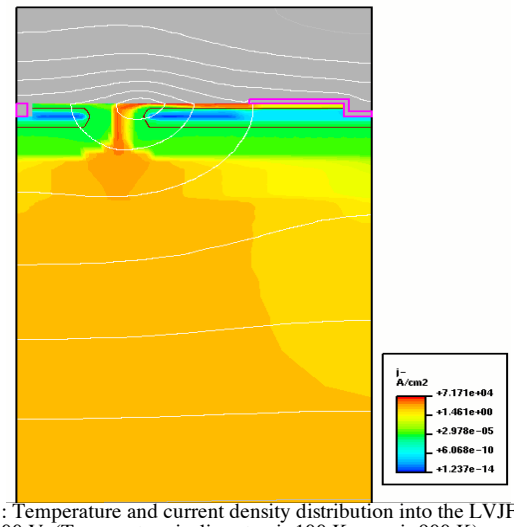

Fig. 15: Temperature and current density distribution into the LVJFET @ V_{DS}= 400 V. (Temperature isoline step is 100 K, max is 900 K).

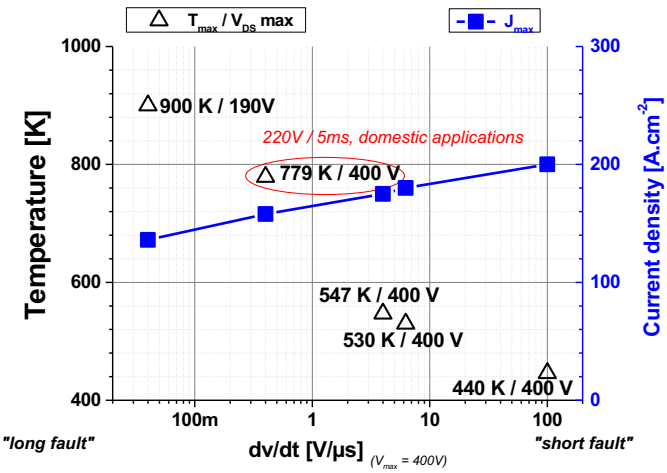

Fig. 16: Simulated estimation of electro-thermal capability of the VJFET @ V_{DS}= 400 V

From those simulations we can conclude that the current limiter is suitable for domestic application (220 V for 5 ms) as the maximal temperature reached in case of short-circuit is about 780 K.

4.3 Experimental results.

Based on those simulations, this device has been fabricated and shows a current limiting capability with a maximum dissipated power of 144 kW/cm□. (Fig. 17).

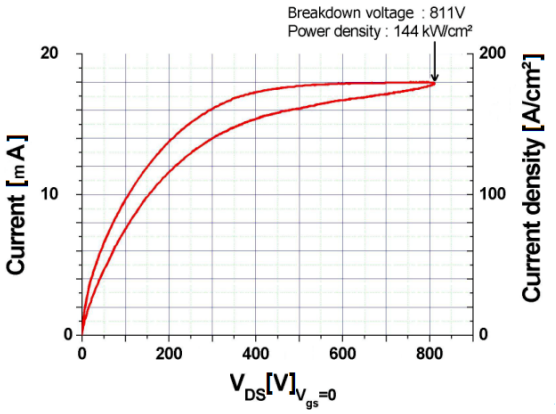

Fig. 17: High voltage current limiter I-V and J-V characteristics. Measurements correspond to a 0.5 s pulse, with drain bias up to 800 V

Further thermal measurements were done using a packaged device. A heat sink was used to extract power appearing during active state (Figure 18). A sensing element [15] has been included closed to the current limiter to measure SiC temperature rising in case of short circuit.

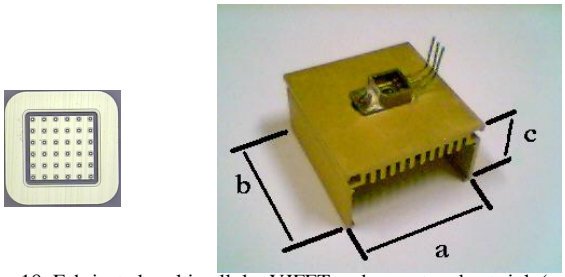

Fig. 18: Fabricated multi-cellular VJFET and mount on heat sink (a= 42 mm, b=44 mm, c= 21 mm).

In this configuration, a high voltage (320 V) was applied and hence a high current density (2580 A/cm^2 in the

channel) was estimated by simulation. Then the power density dissipated into the device is about 20 kW/cm^2, corresponding to a maximum estimated temperature of 215ºC.

5 Conclusion

In order to satisfy the requirements of serial protection, two different structures have been extensively studied to realize silicon carbide limiters. Electrothermal simulations have been performed to optimize the very sensitive channel features (doping level and geometry). Different hypothesis have been taken into account for the environment of the current limiter. For a comparative study, a silicon device has also been studied but thermal runaway was observed in the same conditions showing that silicon is not adapted for this kind of application. The fabricated SiC Accu-MOSFET shows good characteristics closed to the expected electrothermal simulations with a low on-state resistance (13 mΩ.cm^2) in passive state and high voltage capabilities (600 V rated device). Similar characteristics were measured with the three terminal device, the SiC LVJFET. Device was packaged, the maximum temperature inside was estimated to 215°C thanks to an additional thermal sensor. Finally, we may conclude that SiC is well suited for fault current applications with electrical power levels which are not allowed by silicon devices.

Acknowledgments

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