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Current limitation with SiC devices

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Abstract

This paper reports the different solutions we have studied to integrate current limiters with SiC-based devices. Current limiters are highly needed for serial protection in almost the full range of power applications, from telecommunication market to traction and energy distribution. Two types of structures are presented, with two and three terminals, respectively. The two terminal device is based on an ACCUMOSFET structure optimised for current limiting application. The three terminal device is a special JFET design for efficient current pinch-off. Both structures have been optimised using numerical simulations and then fabricated, characterized and checked in a real circuit. The current limiting capability has been demonstrated and the superior potential of SiC is experimentally demonstrated.

Introduction

There exists a great deal of fault current limiter devices for serial protection, from polymer-based devices [1], regulation systems to other complex devices such as circuit breakers, mechanical switches or more conventional fuses. Nevertheless, only few semiconductor based current limiter structures have been proposed [2,3] up to date. Although current regulative diodes are available in the market [4,5], their voltage and current capabilities ($V_{BR} = 100$ V, $I_{max} = 10$ mA) do not allow to use them in power systems. On the other hand, SiC-based devices are very suitable for high current and high voltage applications. Promising applications of SiC-based devices are the current limiting devices for power system protection, which benefits from its high thermal conductivity ($\lambda = 4,9$ W·cm⁻¹·K⁻¹) and wide band gap ($E_g=3.1$ eV). Most of the conventional Si switches have been fabricated in SiC, showing excellent electrical and thermal characteristics such as those of the SiC Schottky diode, MOSFET and MESFET. Recently, we have proposed a specific SiC-current limiter [6,7], which shows the potentiality of SiC devices for high dissipation applications. In this paper we report the last results we have obtained on this topic. Two structures have been studied, a two-terminal ACCUMOSFET structure and a JFET with buried gate and gate control.

Proposed structures

The ACCUMOSFET

Specific devices have been designed in order to obtain normally on devices, with an on-state voltage drop as low as possible and with both high current and voltage capabilities. The main requirement lies on the fact that a current limiter must respond as fast as possible in case of short-circuit or over-current without any electronic control system. Therefore, a modified ACCUMOSFET structure has been studied [6] firstly.

The design of the ACCUMOSFET structure allows the integration of a simple two terminal current limiter. The proposed structure is shown in Fig. 1. It corresponds to an ACCUMOSFET with a wide channel and the gate short-circuited to the source. This structure shows a low on-state voltage drop and a current limiting capability. Devices have been fabricated with a 7-lithographic level process technology. The ACCUMOSFET cross-section is shown together with the guard ring termination, the implanted N-channel and the P⁺-implanted layer.

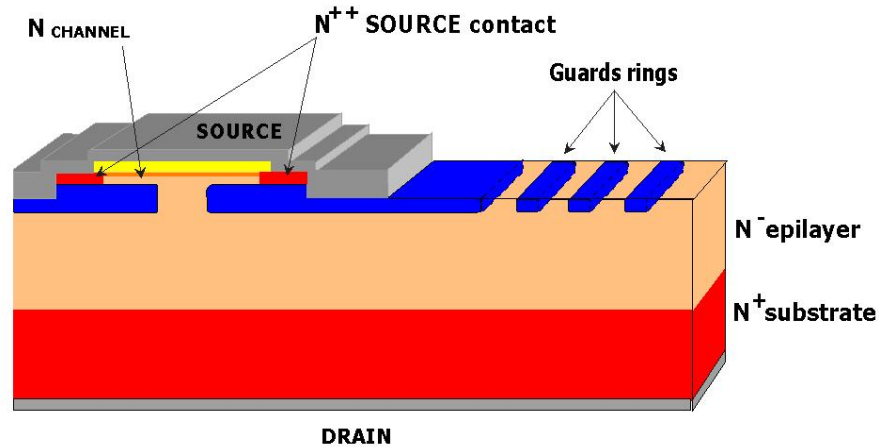


Fig. 1.- Cross-section of the two terminal current limiting structure based on the modified ACCUMOSFET.

The devices are 600V rated. The experimental I-V characteristics for different layouts are shown in Fig. 2. As it can be seen from this figure, the experimental results are close to those predicted by the simulations (DESSIS ISE [8]).

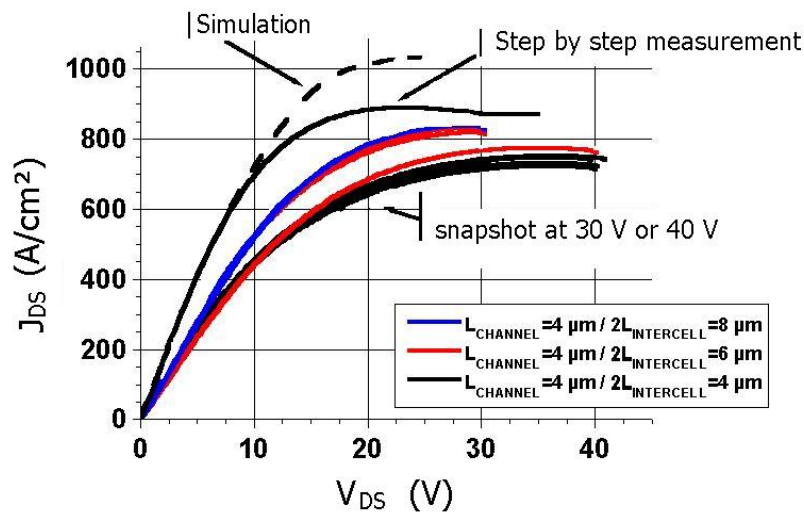


Fig. 2.- Experimental and simulated I-V characteristics of current limiter for different layouts. The simulated structure: $L_{\text{CHANNEL}} = 4\mu\text{m}$, $2L_{\text{INTERCELL}} = 8\mu\text{m}$.

The device shows an on-resistance of 13 mohm.cm² in the active region, and starts limiting the current at 10V at a current density in the range of 600-800 A/cm², depending on the self-heating effect. The device has been tested in the current limitation mode up to 400V.

The JFETstructure

A three terminal device has been also proposed, which is based on a specific JFET design. The novelty of this device consists in the buried gate. (Fig. 3). The P-buried layer is designed so that the VJFET is normally-on and shows a low specific on-resistance. Layout and technological parameters

have been adjusted so that the JFET shows a pentode-like characteristics even at high voltages. Moreover, a gate electrode has been implemented in order to modulate the current in both conducting and limiting operation modes.

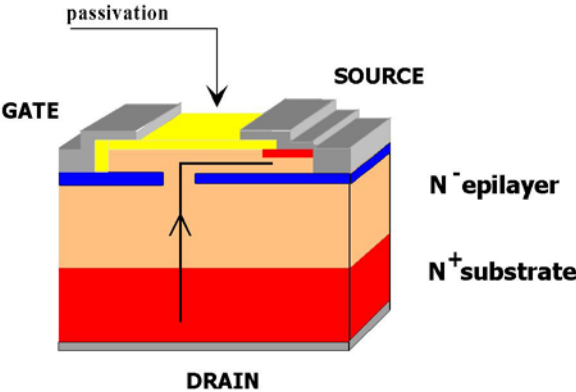


Fig. 3.- Three terminal current limiter based on a VJFET structure.

Various structure layouts have been fabricated to validate both the process technology and the device performances. The measured electrical characteristics of a 1D device is shown in Fig. 4. Measurements correspond to a 0.5 s pulse ($f = 2\text{Hz}$), with drain bias up to 800 V. The maximum dissipated power density in the limiting device is 144 kW/cm^2 . Current limiting capability was also measured for a bi-directional device made of two unidirectional devices head to tail connected. The highest breakdown voltage measured in current limiting operation mode was 811 V.

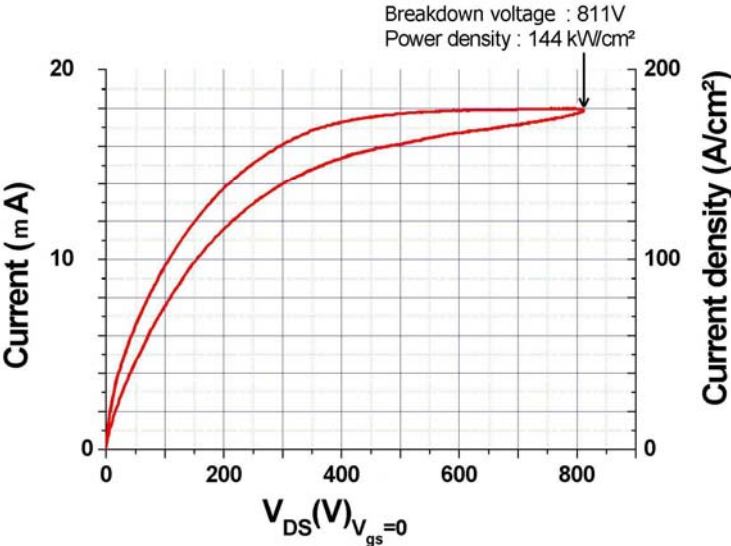


Fig.4.- High voltage current limiter I - V characteristics

Different layouts have been implemented: square cells with the source in the middle and the buried gate surrounding the source (Fig. 5-a); and a matrix array of square sources individually surrounded by a buried gate (Fig. 5-b); in both layouts the gate electrode was placed at the structure periphery.

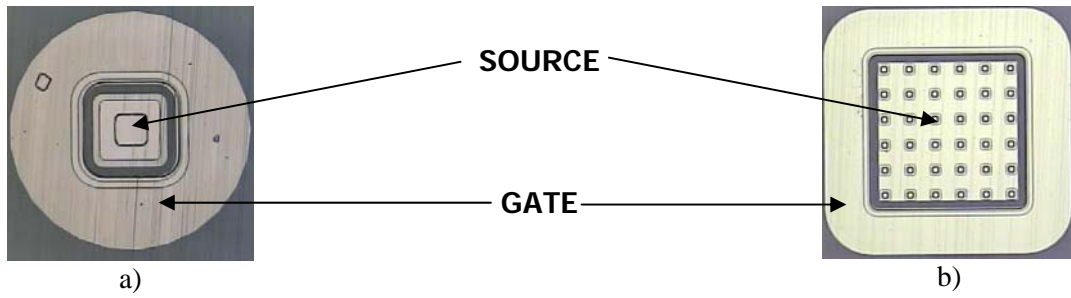


Fig. 5.- Fabricated layouts: a) square cell, b) matrix array

Due to self-heating effect the limiting current decreases as the voltage increases due to the electron mobility dependence on temperature. This effect is amplified when increasing the current density (with the appropriate layout; i.e.; with a high effective channel width per unit area layout) as show in Fig. 6.

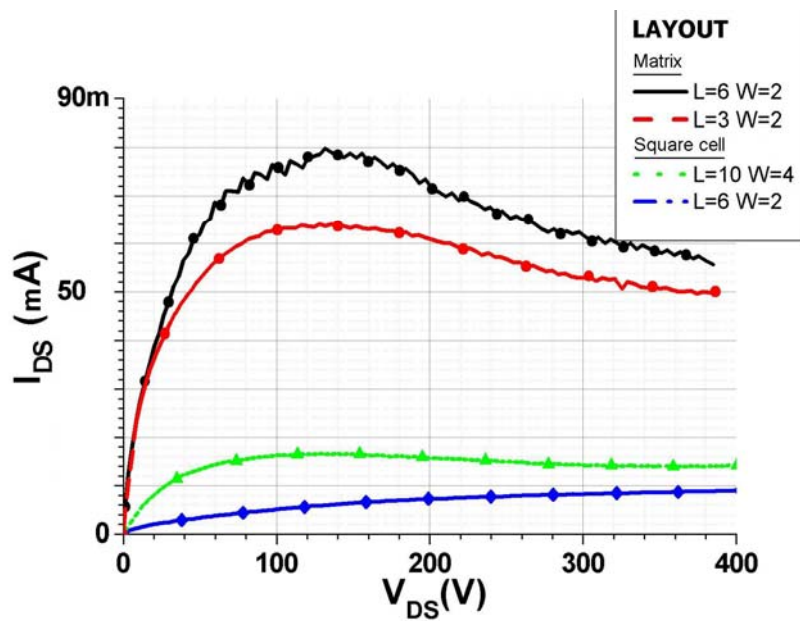


Fig. 6.- Current limiter I - V characteristics for different layouts.

To illustrate the gate control on the output current, switching simulations was performed with a two-step gate bias. The first gate bias step ($V_{GS} = -10$ V @ $t=10\mu s$) underlines the current reduction capability, from 55 A/cm² to 48 A/cm². Then, the second gate bias step, $V_{GS} = -40$ V @ $t=15\mu s$, allows to shut down the drain current in the circuit as shown in Fig. 7.

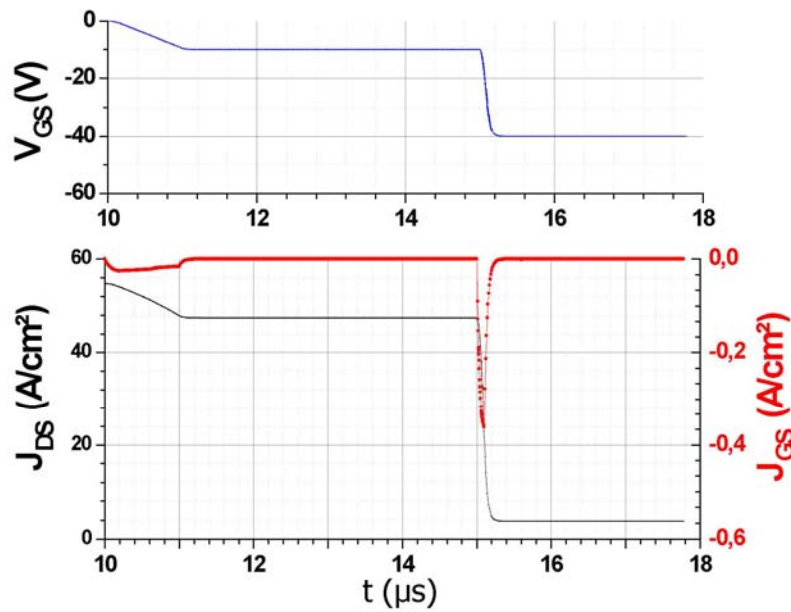


Fig. 7.- Simulated switching characteristics showing current reduction and shunt down capabilities.

The switch-off gate current depends on the gate resistance and on the voltage rise time. The gate switch-off power losses can be fixed with the gate resistance, without varying the drain current and the switch-off time, as shown in Fig. 8. In this way, the gate power losses and peak current can be reduced a 10% increasing the gate resistance from 20 Ω to 30 Ω (Fig. 8).

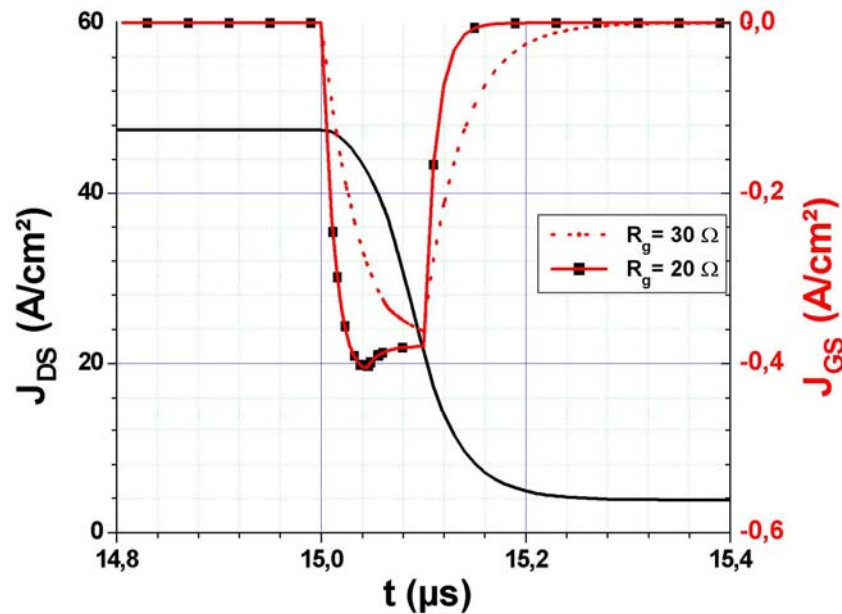


Fig.8.- Simulated switching-off characteristics for two R_G values showing gate current reduction (i.e. gate power losses reduction) without varying the drain current switching time.

Experimental switching measurements

The set-up shown in Fig. 9 was used to illustrate the device current limiting capability. The current limiter is plugged in series with the power supply and the load (L_S and R_S). The utilised loads for the experiment were 230V/5W bulbs. A short-circuit was performed across the load with either a

mechanical switch or a commercial high voltage Si MOSFET. The measured current and voltage waveforms are presented hereafter for each kind of current limiter utilised. In the case of the SiC ACCUMOSFET limiting device, no gate control system was needed; and with the modified SiC JFET device, no gate bias was applied.

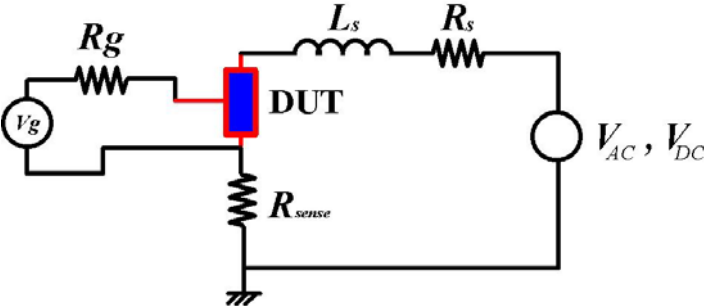


Fig. 9.- Electrical circuit to perform short-circuit test.

The ACCUMOSFET

In order to perform dynamics measurements and to evaluate the short-circuit behaviour, the SiC ACCUMOSFET limiter were packaged and bonded (Fig.10).



Fig. 10.- Packaged SiC ACCUMOS limiting device.

Fig. 11 shows the experimental voltage rising across the current limiter in case of short-circuit. The current rise time was $t_r = 1.4 \mu s$ and the over-voltage across the load was limited to 20 V, approximately.

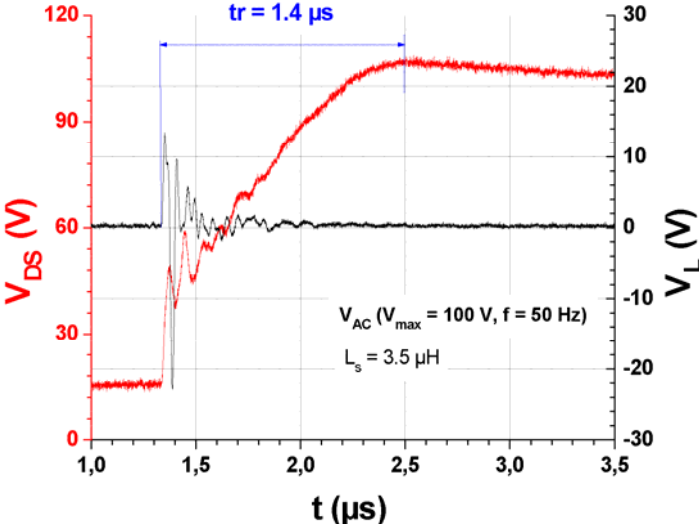


Fig. 11.- Experimental SiC ACCUMOSFET response time to a short-circuit.

In order to check the protection efficiency, an additional inductor was plugged in series with the load and the current limiter in the circuit to increase its value from $3.5 \mu H$ to $35 \mu H$. A DC power supply was used to get real working conditions. As inferred from Fig. 12, the SiC ACCUMOSFET is

able to limit the over-voltage appearing in the circuit. A x10 higher inductor implies only a x3.6 over-voltage peak. Concerning the current through the load, almost the same experimental output current was measured for $L_S = 3.5 \mu\text{H}$ and $L_S = 35 \mu\text{H}$. These measurements showing that both over-current and over-voltage are limited by the SiC limiting device. Furthermore, no significant t_r shift has been experimented (Fig. 13) rising L_S .

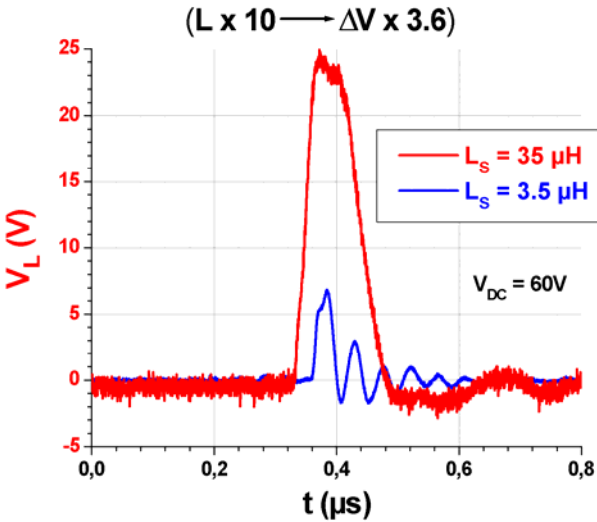


Fig. 12.- Over-voltage measurements with the SiC ACCUMOSFET.

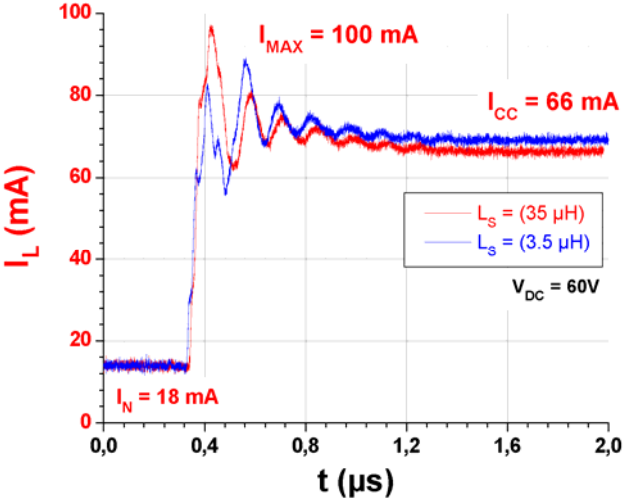


Fig. 13.- Experimental output current through the ACCUMOSFET.

The JFET structure

Similar measurements on the same test circuit have been performed using the SiC VJFET. As shown in Fig. 14, fabricated current limiters were encapsulated either on Alumina substrate (on the left, showing also the test set-up) or in a metallic TO220 package (right).



Fig. 14.- Short-circuit test set-up and encapsulated VJFET, on alumina (left) and metallic TO220 (right).

The measured response time of the SiC JFET, in case of short-circuit, is lower than $1 \mu\text{s}$ (Fig.15).

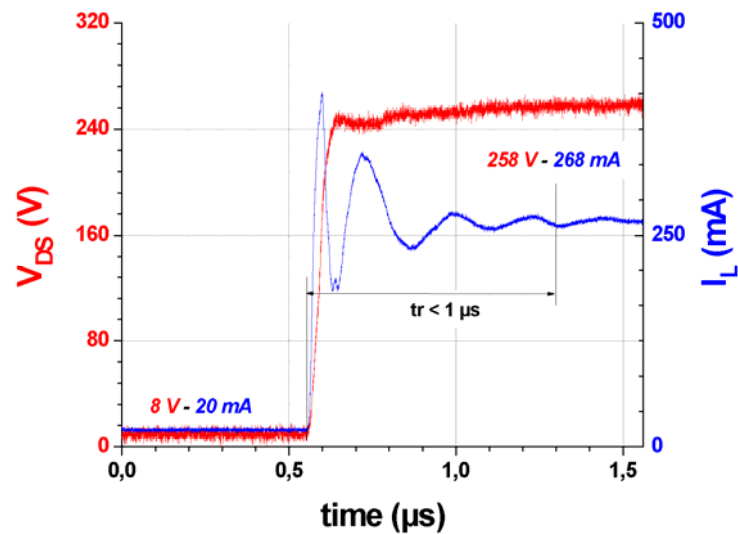


Fig. 15.- SiC VJFET experimental response to a short-circuit.

Without any electronic control system (i.e., with no gate bias), the SiC VJFET current limiter is able to respond in very short time. The short-circuit was maintained during several minutes without degradation of the electrical behaviour, the power dissipated being 78W. Due to the high dissipated power in limiting operation mode, it was necessary to modulate the saturation current of the SiC VJFET. To illustrate this behaviour, dynamic gate switching measurements were performed (Fig. 16).

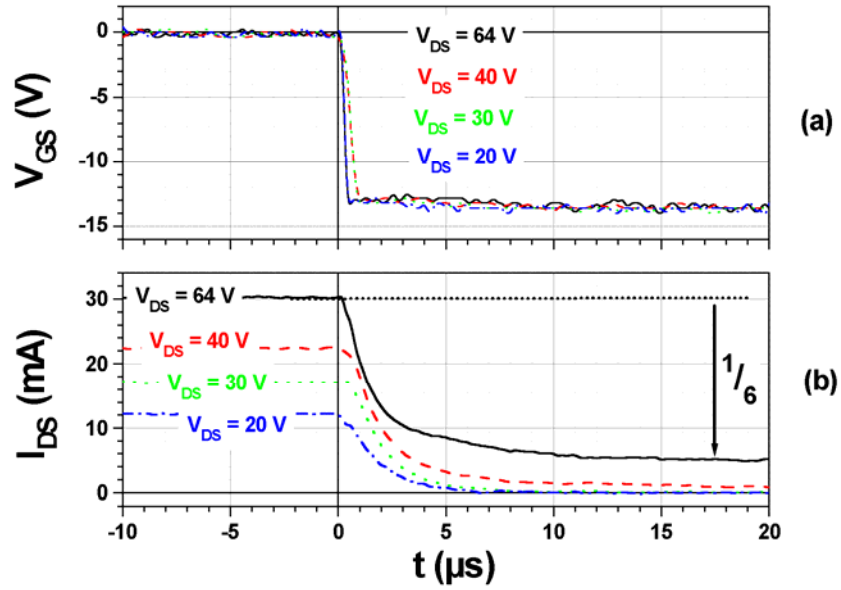


Fig. 16.- Measured switching characteristics. a) Applied V_{GS} versus time for different V_{DS} values. b) Output current versus time for various V_{DS} values.

From Fig. 16 we can experimentally conclude that the gate bias control by its own allows the output current modulation. Switching times of 5 μs were measured, which corresponds to the time constant (L/R) of the electrical circuit. A current reduction factor of $1/6$ was measured, implying a power loss reduction, by the same factor, in the limiting operation mode.

Conclusions

Two different solutions have been studied to integrate SiC current limiters to benefit from Silicon Carbide properties. Two types of structures (with two and three terminals) have been optimised using numerical simulations and then fabricated, characterized and checked in a real working circuit. The two terminal SiC ACCUMOSFET shows good characteristics in terms of response time to a short-circuit (less than 1.5 μ s) and high voltage capabilities (600V rated device). Such a SiC device permits a significant reduction of over-voltage that normally appears across the load in case of sudden current shifts. Similar characteristics were measured with the three terminal device, the SiC VJFET. In this last case, the highest breakdown voltage measured in the limiting state was 800V. Rising times lower than 1 μ s have been measured. Gate switching measurements have shown output current modulation capability and, therefore, power loss reduction in the limiting operation mode.

The current limiting capability has been demonstrated and the superior potential of SiC has been also shown experimentally. Next challenge will consist in the design of a fully integrated SiC current limiting device, based on a VJFET and MESFET association.

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