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Deep traps localization in AlGaIn/GaN MIS-HEMTs by a comparative study using capacitance and current deep level transient spectroscopies

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Abstract. In this study, deep traps in multiple-finger normally-off AlGaIn/GaN metal-insulator-semiconductor high-electron mobility transistors (MIS-HEMTs) were identified. The localization of these traps has been established by a comparative study using capacitance and current deep level transient spectroscopies (DLTS). The C_{gd} -DLTS measurements cover the GaN buffer region between the gate and drain contacts. On the other hand, the I_{DS} -DLTS measurements cover the channel region in GaN including the zone under the gate. Two electron traps, E2 (0.31eV) and E4 (0.5eV) have been detected. They are respectively attributed to reactive ion etching (RIE) induced surface damage. These two traps are more likely located in the GaN channel close to the gate. Two other deep electron traps E5 (0.64eV) and E6 (0.79eV) have also been detected and are localized in the GaN buffer layer.

1. Introduction

GaN material holds an advantageous position in the fabrication of power devices [1]. This advantage is manifested by the possibility to perform GaN based devices working in high voltage, high current, high frequency and high temperature conditions. However, despite these theoretical forecasts, trapping mechanisms limit the performances of the GaN devices [2]. In this context, the deep level transient spectroscopy (DLTS) is one of the most well-adapted techniques for deep-level characterization. The DLTS developed by Lang [3] was originally applied to depleted layers of semiconductors in Schottky or p-n junctions and measured capacitance transients, though it was mentioned that DLTS is equally applicable to current transients [4]. The DLTS technique can be applied to depletion regions of MIS structures (depletion mode) [5]. In this paper, the deep levels in the MIS-HEMTs were examined and localized by comparing capacitance deep level transient spectroscopy (C-DLTS) and drain-source current DLTS (I-DLTS) applied directly on MIS-HEMT transistors.

2. Experiments and discussions

2.1. Experimental methods



The DLTS study was carried out with MIS transistors grown by metalorganic chemical vapor deposition on a 200mm diameter Si substrates, oriented (111). The epitaxy consists of an AlN nucleation layer, followed by AlGaN buffer layers, then a 1.8 μm thick semi-insulating carbon doped GaN buffer layer, 100nm of back barrier layer, a 200nm unintentionally doped GaN layer acting as the channel material, a 1nm unintentionally doped AlN layer and a 21.4nm unintentionally doped Al_{0.20}Ga_{0.80}N barrier layer. Si₃N₄ was used for the passivation of the stack. Interdigitated comb-like transistors with one hundred 1 \times 1000 μm^2 gate fingers were then formed using TiN/W as gate metal and Ti/Al annealed for 30s at 875 $^\circ\text{C}$ as ohmic contact. Recessed gate electrodes were achieved by etching Si₃N₄ passivation and 35nm of the AlGaN/GaN bilayer using a dry etching process. The gate-to-drain distance L_{GD} is 15 μm . 30nm of Al₂O₃ was used to form the gate oxide. Electrical characteristics and deep level transient spectroscopy data were acquired with a Fourier transform deep level transient spectroscopy (FT-DLTS) system from PhysTech (FT 1030) using a Boonton 72B capacitance meter with a 100mV test signal at 1MHz. Capacitance and current transients were recorded between 80K and 450K in the warm up mode.

2.2 Experiments and results

2.2.1 Capacitance DLTS

The concept of Capacitance DLTS (C-DLTS) technique is based on using a depletion region. In such region, the population of holes and electrons is low as a result of the repulsion and drift of these carriers in the depletion field. In case of MIS-HEMTs with recessed gate, the extension of this depletion region around the gate is given in a first approximation by the usual parallel-plate capacitor approximation $C=S\cdot\epsilon/d$, where «S» is the recessed gate area in GaN, « ϵ » is the insulator or the GaN dielectric constant and «d» is the insulator or the depletion region thickness.

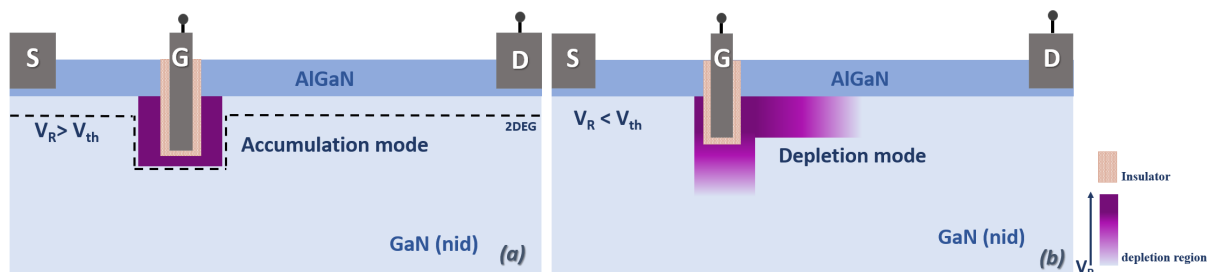


Fig.1 The distribution of the depletion region in the structure according to the applied reverse bias V_R in (a) accumulation and (b) depletion mode.

Two conditions of reverse bias polarization were chosen for the DLTS experiments: i) $V_R=0\text{V}\approx V_{\text{th}}$. In this case, the studied region is primarily confined between the 2DEG channel and the insulator of the recessed gate as shown by the schematic in Fig. 1a; ii) When the gate bias is much smaller than V_{th} ($V_R=-10\text{V}$), the 2DEG is pinched-off. In this case, the depletion depth is much larger than the gate insulator thickness, so «d» is primarily constituted by the GaN buffer layers vertically under the gate and laterally between the gate and the drain as shown in Fig. 1b.

The Fig. 2 presents the DLTS spectrum carried out with a MIS-HEMT transistor structure described in section 2.1. This spectrum is recorded with a reverse bias $V_R=0\text{V}$, a filling pulse height $V_p=2\text{V}$, a filling pulse width $t_p=1\text{ms}$ and a period width $T_w=200\text{ms}$. We determined that, by taking into account a pinch-off voltage of 0V at 300K found by $C_{\text{gd}}(V)$ measurements, the probed zone under these C_{gd} -DLTS measurement conditions is located in the channel. The three main detected electron traps were found in a previous work [6]. Traps E2 (0.31eV) and E4 (0.50eV) can be related to RIE-induced surface damage near the gate [7]-[8] and trap E5 to gallium vacancy related defect [9]-[10]. By keeping a filling pulse height $V_p=2\text{V}$, we applied a reverse bias $V_R=-10\text{V}$ to increase the depletion

region of the transistor and probe a deeper region in the GaN buffer layer between the gate and the drain (Fig. 1b).

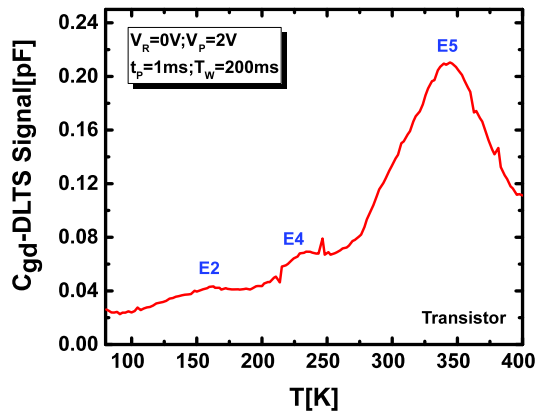


Fig. 2: Gate-Drain DLTS measurement of an AlGaIn/GaN MIS-HEMT transistor recorded with $V_R=0V$, $V_P=2V$, $t_p=1ms$ and $T_W=200ms$.

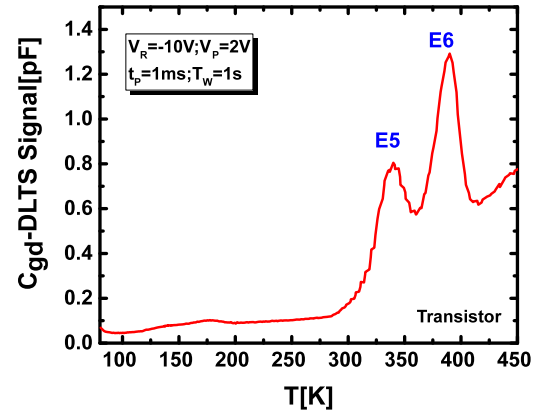


Fig. 3: Gate-Drain DLTS measurement of an AlGaIn/GaN MIS-HEMT transistor recorded with $V_R=-10V$, $V_P=2V$, $t_p=1ms$ and $T_W=1s$.

The C_{gd} -DLTS spectrum in Fig. 3 depicts two traps E5(0.64eV) and E6(0.79eV) related to native defects [6], [8]-[10]. At $V_R=-10V$, the amplitude of E5 is higher than for the case of $V_R=0V$. This could reveal that the concentration of E5 defect in depth of GaN is higher than the one at the interface. The absence of trap E6 in $V_R=0V$ polarization or at least its presence in low density, and contrariwise, its clear appearance for $V_R=-10V$ indicates its deeper position in the GaN buffer layer. This C_{gd} -DLTS measurement covers the GaN buffer region between the gate and drain contacts, which can explain the dominance of the defects E5 and E6 related to the native defects in GaN.

2.2.2 Current DLTS

In I_{DS} -DLTS, deep levels are detected by monitoring the drain-current (I_{DS}) changes induced by gate-source-voltage (V_{GS}) pulses. Positive V_{GS} pulses superimposed on negative V_{GS} bias voltage induce electron capture (as $V_{GS}=V_P$ is stepped up) and subsequent thermal reemission (after $V_{GS}=V_R$ is stepped down to its steady bias value) by deep-level traps located in the 2DEG channel [11].

However, unlike C-DLTS, I_{DS} -DLTS does not provide inherent spatial sensitivity because I_{DS} is constant throughout the device. Nonetheless, the physical location of defects can be ascertained. By rising V_{DS} voltage, the electrical field lines cover a larger region (Fig. 4b) which causes hot electrons to scatter out of the channel. These latter hot electrons become trapped in the GaN buffer layers.

Fig. 5 shows an I_{DS} -DLTS signal for several drain voltages V_{DS} . Three electron trap signals were observed, that matches the defect levels E2, E4 and E5 obtained by capacitance DLTS (gate-to-drain configuration) in Fig. 2. This I_{DS} -DLTS measurement covers the channel region in GaN including the zone under the gate, which can explain the dominance of the two defects E2 and E4 related to the gate etching process. In case of $V_{DS}=1V$, the probed region is too close to the gate and does not cover the entire region affected by traps E2 and E4 (Fig. 4a). When V_{DS} increases, the probed zone covers the whole region affected by E2 and E4 but also extends into the unintentionally doped GaN (Fig. 4b). That is why the amplitude of the three traps increases but not in the same proportion. By increasing the V_{DS} polarization (up to 5V), the amplitude of E5 defect increases, which confirms that E5 related to gallium vacancy defect is located in the buffer layers.

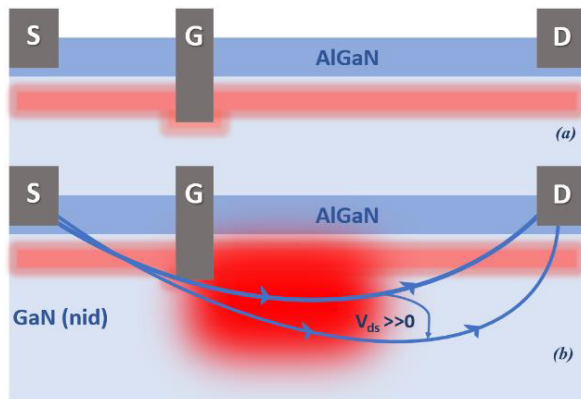


Fig. 4: The probed region for current DLTS measurements according to (a) $V_{DS}=1V$ and (b) when V_{DS} increases.

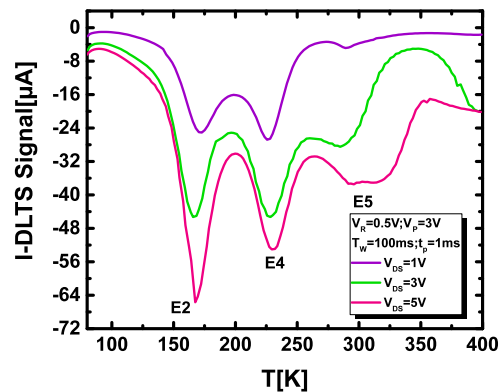


Fig. 5: Current DLTS measurement of an AlGaN/GaN MIS-HEMT transistor recorded with $V_R = 0.5V$, $V_P = 3V$, $t_P = 1ms$ and $T_W = 1s$ for several V_{DS} bias.

3. Conclusion

Four deep traps were found in multiple-finger normally-off AlGaN/GaN MIS-HEMTs using FT-DLTS. Among these traps, E2 and E4 seems to be formed by the etching process. Traps E5 and E6 are commonly observed in epitaxial GaN and are related to native defects. The localization of these traps has been established by means of capacitance and current deep level transient spectroscopy (DLTS). The C_{gd} -DLTS measurements show a dominance of E5 and E6 related to native defects in GaN. On the other hand, the I_{DS} -DLTS measurements reveal a dominance of E2 and E4 related to the gate etching process. Traps E2 and E4 have been localized in the channel close to the gate. E5 and E6 were localized in the GaN buffer layer.

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