Highly textured Pt thin film grown at very low temperature using Ca 2 Nb 3 O 10 nanosheets as seed layer

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Highly textured Pt thin film grown at very low temperature using $Ca_2Nb_3O_{10}$ nanosheets as seed layer.

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Abstract: The decrease of the growth temperature of platinum (Pt) thin film on silicon substrate was studied using $Ca_2Nb_3O_{10}$ nanosheets (CNOns) as seed layer. These nanosheets were obtained by the delamination of the layered perovskite $KCa_2Nb_3O_{10}$ and they were deposited on silicon substrates by the Langmuir-Blodgett method. Pt thin films were sputtered on silicon coated by CNOns (CNOns/SiO_2/Si), and on TiO_2/SiO_2/Si substrates for comparison, at temperatures ranging from room temperature up to 625°C. X-ray diffraction, scanning electron microscopy, and atomic force microscopy were used to characterize the crystalline quality, thickness, surface morphology and roughness of the Pt thin films. Highly (111) textured Pt thin films were obtained on CNOns/SiO_2/Si at substrate temperature as low as 200°C. The full width at half maximum of the rocking curve of the (111) X-ray peak was about one degree, indicating a high crystalline orientation. The resistivity was measured at room temperature by the four point probes method to confirm the quality of Pt thin films elaborated at low temperatures. These results pave the way for easier integration of highly textured platinum thin film in low temperature microelectronic processes.

Keywords: Platinum thin film, nanosheets, electrode, low temperature, silicon substrate.

1. Introduction

Electrode processing technology is the subject of many studies because electrodes play an important role in electronic devices. This is particularly the case for the development of capacitors and memories where the quality of the film-electrode interfaces is crucial for the electrical properties. Noble metals are often employed when an oxidation-resistant electrode is required. This is the case, for example, with the integration of thin films of dielectric and ferroelectric perovskite on silicon in oxidizing atmosphere. Oxide electrodes such as $SrRuO_3$ or $LaNiO_3$ (LNO) can also be used, but they usually require high crystallization temperatures. In the case of LNO, Zhang *et al.* [1] showed that crystallization was possible even at low temperatures (around 300°C), but the resistivity of these films was high, more than 1 mΩ.cm. Indeed, such oxide electrodes have a resistivity at least twenty times higher than that of platinum (Pt) which has a bulk resistivity of 10.6 μΩ.cm. Oxide electrodes also have a lower Schottky barrier height, resulting in higher leakage currents. Therefore, Pt is still widely used to provide metal electrodes in devices such as Metal/Ferroelectric/Metal (MFM) capacitors.

Reports on the elaboration of Pt thin films by sputtering have shown that the argon pressure during the deposition process is a key parameter for porosity and roughness. For example, Chang *et al.* have reported that dense films are obtained at sputtering pressure lower than 5 Pa [2]. Sakaliuniene *et al.* have also shown that film porosity is reduced and therefore that the resistivity decreases from 85 to 25 μΩ.cm when the argon pressure is reduced from 5 to 0.6 Pa [3]. In addition, it has been shown that the deposition temperature of these electrodes has a strong influence on the crystalline quality of the Pt film and thus on the electrical properties of the MFM stack [4-8]. Indeed, the well-ordered structure of the Pt electrode promotes crystal growth of the oxide ferroelectric film. Deposition temperatures or annealing above 600°C are required to obtain well-crystallized Pt films on $TiO_2/SiO_2/Si$ substrates [4, 6-9]. The thin TiO_2 layer improves adhesion and crystallization of platinum on the SiO_2/Si substrate [10-13]. Buffer layers like Ta, Zr or ZrO_2 [14-15] have also been tried, but TiO_2 is still widely used for the adhesion of the Pt bottom electrode. However, regardless of this buffer layer, the growth temperature of the Pt bottom electrode is very high, in the range of 600 to 700°C. This temperature is higher than the temperature required for the elaboration of conventional Si-based circuits, which is generally lower than 500°C. This leads to a limitation in the use of platinum electrodes which should therefore only be deposited at the early step of any process.

On the other hand, over the past 12 years, numerous authors have shown that two dimensional materials such as oxide nanosheets promote the growth of functional oxide materials on silicon or glass [16-21]. Since the pioneering work of Kikuta *et al* [16], followed by Shibata *et al* [17-18], a wide variety of oxides such as $SrTiO_3$, TiO_2, ZnO, $LaNiO_3$, $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) and $La_{0.7}Sr_{0.3}MnO_3$ have been grown using nanosheets such as $Ca_2Nb_3O_{10}$, $Ti_{0.87}O_2$ or MoO_2 [19-23]. The preparation of nanosheets covered substrates (Ns-substrates) mainly comprises two basic steps: the exfoliation of the nanosheets from layered compounds, followed by their deposition on the substrates by Langmuir-Blodgett (LB) method. These Ns-substrates have demonstrated their interest in obtaining well-crystallized oxide films at temperatures lower than those usually used. For example, in the case of PZT, Nguyen *et al*. [22] have shown that PZT can be grown at only 450°C while retaining interesting ferroelectric and piezoelectric properties.

The objective of the present study was to reduce the deposition temperature required to obtain high quality Pt electrodes on silicon substrate by using nanosheets. $Ca_2Nb_3O_{10}$ nanosheets (CNOns) have been first prepared by exfoliation and deposited on silicon by LB method. Subsequently, thin films of dense Pt have been sputtered at low pressure (0.6 Pa) and several temperatures, and characterized by X-ray diffraction (XRD), scanning electron microscopy (SEM), atomic force microscopy (AFM), and resistivity measurements.

2. Experimental

2.1. Materials

Boron-doped monocrystalline (100) silicon samples of 7x15 mm^2 were used as substrates. They were coated with a 650 nm amorphous SiO_2 layer obtained by thermal growth. Pt and Ti targets with a diameter of 4 inches and a purity of 99.99% were used for sputtering thin films of Pt and TiO_2. The nanosheets were synthetized from the precursors K_2CO_3 (Acros Organics, 99 %), Ca_2CO_3 (R.P. Normapur, 99.5 %) and Nb_2O_5 (Alfa Aesar, 99.5 %).

2.2. Nanosheets synthesis

$Ca_2Nb_3O_{10}$ nanosheets were obtained from $KCa_2Nb_3O_{10}$ which was synthesized by solid state reaction under the conditions of Ebina *et al*. [24]. An ionic exchange between potassium ions and protons was carried out using 6M HNO_3 acid during 72 hours. The acid was changed every 24 hours to obtain a powder of $HCa_2Nb_3O_{10}$ that was then diluted in a solution of distilled water and tetrabutylammonium hydroxide (TBAOH) in a 1:1 molar ratio, leading to the formation of a colloidal solution containing $Ca_2Nb_3O_{10}$ nanosheets. This solution was then dilut-

ed and placed in a Langmuir-Blodgett trough. The SiO_2/Si substrate was first washed with distilled water and then with ethanol, before being immersed in the solution. After LB deposition of the nanosheets, the substrates were first dried at 110°C and placed under UV light to photochemically destroy TBA residues. The substrates were then air-heated at 300°C for 1 hour to remove water and organic residues from the elaboration process. Finally, the stacking of the layers forming the substrate was $Ca_2Nb_3O_{10}$/SiO_2/Si (CNOns/Si).

2.3. Film Deposition

Platinum thin films were deposited *in situ* on CNOns/Si and on TiO_2/SiO_2/Si (TiO_2/Si) substrates by radio frequency (RF) magnetron sputtering. A pressure of 0.6 Pa of pure argon gas was used. The sputtering targets (Ti and Pt) were mounted horizontally, facing the rotating substrate holder at a distance of 4 cm. Each deposition was preceded by 15 minutes of preliminary sputtering. The power density applied to the Pt target was 1 W/cm², resulting in a film deposition rate of approximately 20 nm/min. For all samples, the film thickness was maintained close to 100 nm. Substrate temperature was varied from 30°C (room temperature) to 625°C. The heating and cooling ramps were 15°C/min and 30°C/min, respectively, with a dwell of 30 min at the selected temperature before deposition. For the preparation of TiO_2/Si substrate, TiO_2 was RF sputtered from a metallic Ti target at 500°C. The power density was 1 W/cm², and a gaseous mixture of argon (85 %) and oxygen (15 %) was introduced into the chamber at a pressure of 1.5 Pa. The same target-to-substrate distance and temperature ramps were used as for Pt deposition. The deposition rate of TiO_2 was determined by measuring with a SEM the thickness of several cross sections of a TiO_2 thin film deposited for 2 hours. The deposition time of the TiO_2 seed layer was then monitored to obtain a thickness of about 1 nm.

2.4. Characterizations

The crystalline structure of the films was analyzed by XRD with a D8 Discover Brucker diffractometer configured in θ-2θ reflection mode (Cu(Kα) wavelength, λ = 0.154056 nm)). Rocking curves were performed on the Pt (111) and the Pt (222) peaks to obtain their full width at half maximum (FWHM) and so to evaluate the grain misalignment.

The cross-sections were prepared in a DualBeam (DB) system (FEI-HELIOS 600, Elstar Field Emission Scanning Electron Microscope (SEM) column and Tomahawk Focused Ga Ion Beam column) allowing both SEM characterization and the preparation of site-specific cross sections using Ga^+ Focused Ion Beam. Before milling the cross-section, a Pt-protective

layer (named Pt-DB in the following) was deposited on the area of interest using the electron beam (5 kV, 800 pA current) for the first hundred nanometers, and then the Ga^+ ion beam (30 kV, 230 pA) for the remaining 1.4 µm. SEM observations were performed at 5 kV, with electron beam current of 400 pA and the In-Column Detector (ICD). The ICD detected Back-Scattered Electrons which were scattered very close to the electron beam axis and provided high Z-contrast signal but also a channeling effect.

The AFM Pico SPM-LE of Molecular Imaging was used in tapping mode to study the surface morphology of the samples before and after Pt deposition. In order to determine the substrate coverage by nanosheets, AFM images (obtained before Pt deposition) were analyzed using the open-source software ImageJ. Brightness and threshold function were adjusted to separate the areas of the substrate covered by nanosheets from the uncoated areas in two colors. AFM was also used to determine grain size and average roughness of Pt thin films using Gwyddion software.

The resistivity measurements were carried out at room temperature using the four probes method. First, the Pt thin films were etched by Ar atoms, with an etching rate of about 35 nm/min. The shape of the patterned Pt thin film was bars of 2 mm long and 150 µm, 100 µm or 50 µm width (supporting information, figure SI-1). Then, six Pt plots were sputtered at room temperature on these bars, using a photoresist and lift-off. The distance between voltage contacts was 300 µm. The measuring current was varied in the range of 1 to 20 µA to check for correct linearity of the recorded voltage. With the 150 µm wide microbridge and a typical Pt film thickness of 100 nm, a current of 1.5 µA corresponded to a current density of 10 A/cm^2. The uncertainty of the resistivity was between 1 µΩ.cm and 1.5 µΩ.cm and rounded up to 2 µΩ.cm for simplicity (supporting information).

3. Results and discussion

3.1. Influence of deposition temperature on Pt crystallization and morphology

The surface of the CNOns/Si substrates was systematically characterized by AFM before the Pt thin film deposition. After LB deposition of the nanosheets, the substrates were first annealed at 110°C for 1h30 and exposed to UV light for 45 min during the dwell. A second annealing was carried out at 300°C in air for 1 hour, just before Pt deposition, to remove the remaining water and organic residues from the elaboration process. No difference in AFM images was observed before and after this second annealing. Figure 1.a) shows a schematic drawing of the sample preparation, and figure 1.b) a typical AFM image after annealing at 300°C. The lateral sizes of the nanosheets extracted from the AFM image are in the range 0.5

to 1 µm and their thickness is 1.5 to 4 nm (figure 1.c)). These results are representative of the entire surface area of all samples and consistent with other works [21-22].

Coverage is between 40% and 85 % (supporting information, figure SI-2). AFM images also show that some overlap of the nanosheets occurs from place to place (figure 1.b)). Previous work has shown that a coverage higher than 95% can be achieved by optimizing nanosheet processing, such as surface pressure during LB deposition or by varying the exfoliating agents [21, 25].

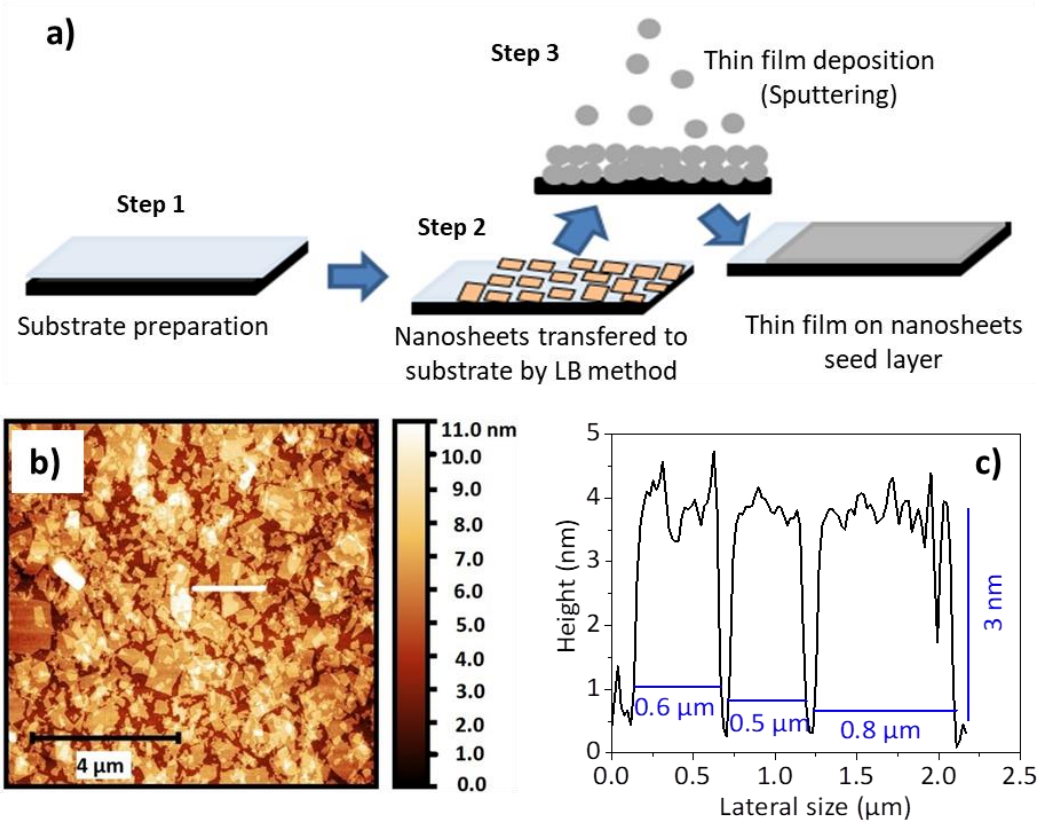

Figure 1: a) Diagram explaining the deposition of nanosheets and Pt thin films, b) AFM image of nanosheets on silicon after annealing at 300°C, and c) height profile measured on the white line in b).

100 nm Pt thin films were deposited on these CNOns/Si and on TiO_2/Si substrates at different temperatures ranging from room temperature to 625°C. The thickness of the bottom electrode is an important factor which modifies the ferroelectric properties for MFM structures. A thickness of 100 nm was chosen in order to promote good ferroelectric properties [26-27].

X-ray diffraction carried out on the Pt thin films showed that only the (111) Bragg peak is obtained on XRD patterns regardless of the growth temperature (see Figure 2). (200) and

(220) peaks did not appear at all. The patterns show that weak Pt (111) peaks were obtained for the Pt films deposited on TiO_2/Si substrates between 200°C and 475°C, then the intensity increases beyond 550°C, while intense peaks were already obtained from 200°C for platinum deposited on the CNOns/Si substrates.

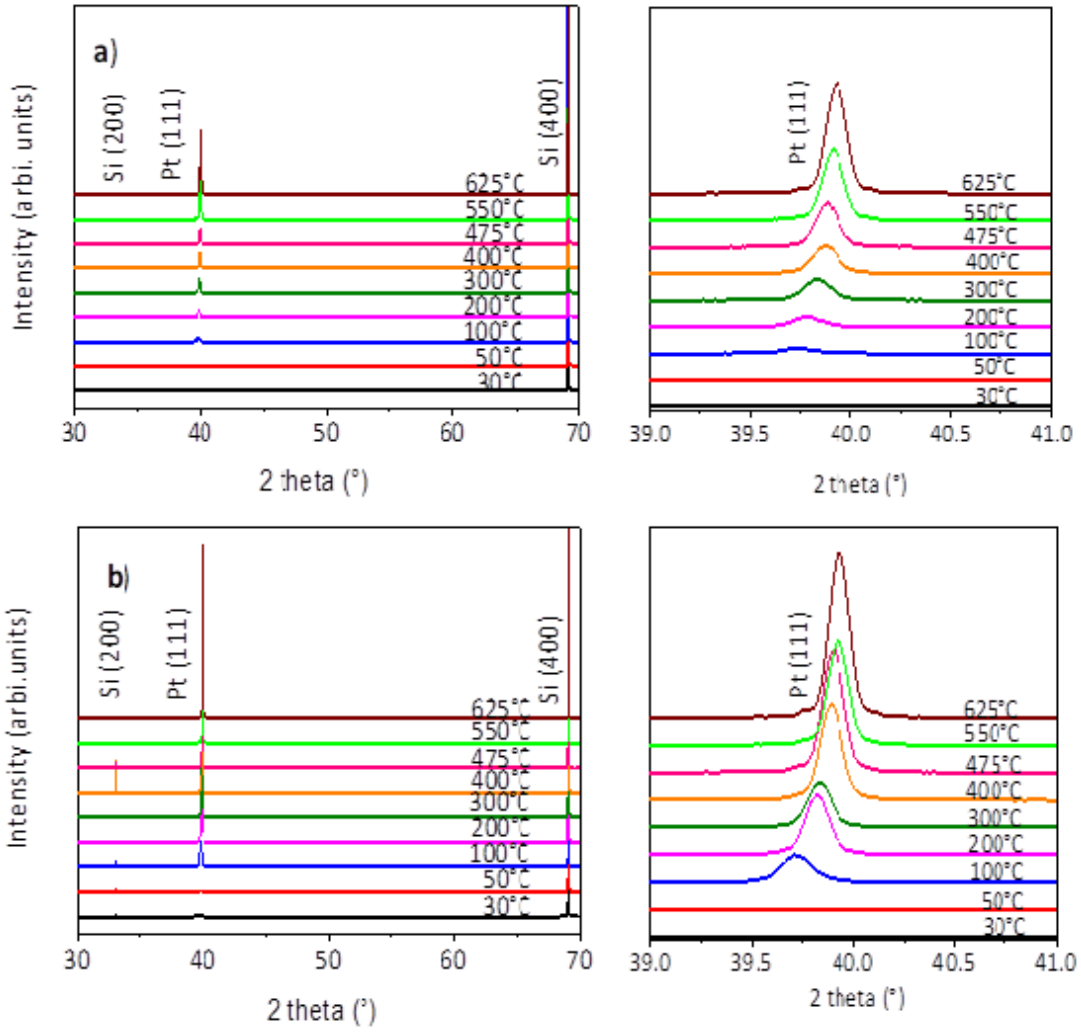

Figure 2: XRD θ-2θ scans of Pt thin films grown at different deposition temperatures on: a) TiO_2/Si substrates and b) CNOns/Si substrates. Enlargement of the 39-41° 2θ range highlighting the shift of the Pt (111) peak.

The peak intensity is also dependent on the size of the diffracting area of the sample, and to compare the results obtained on one sample to the other, the ratios of the intensity of the Pt (111) peak to the intensity of the Si (400) peak were calculated. This ratio is always higher in the case of CNOns, for a given deposition temperature (figure 3). It clearly demonstrates that better crystallization is obtained using CNOns/Si substrates.

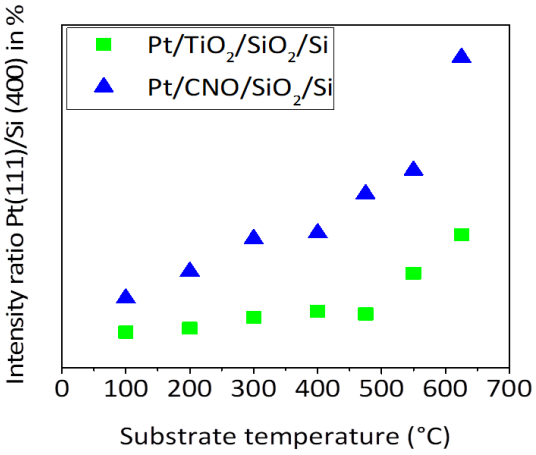

Figure 3: Intensity ratio Pt (111)/Si (400) on CNOns and TiO_2/Si substrates.

A regular shift of the Pt (111) peak towards higher angles (from 39.60° to 39.93°) is observed when the substrate temperature was increased from room temperature to 625°C. A similar trend has been reported for 40 nm thick Pt thin films [28] and for 150 nm and 360 nm Pt thin films grown by DC sputtering on silicon substrate [15]. These films were deposited at room temperature and then annealed in argon at temperatures varying from 400°C to 850°C, and a shift of the (111) X-ray peak from 39.76° to 39.91° was obtained.

X-ray diffraction was also performed at high diffraction angles to observe the Pt (222) reflection. The same shift as for Pt (111) peak was obtained (supporting information, figure SI-3), leading to a good agreement between the values of the Pt lattice parameter deduced from the positions of the (111) and (222) peaks. The intensity of the (222) peak was significantly lower than that of the (111) peak, as expected at high diffraction angles, and the (222) peak was no longer observable for Pt films deposited at 30°C and 50°C. Except for these two lower temperatures, the average Pt lattice parameter is considered (figure 4). It varies quite independently of the nature of the seed layer, thus the stress imposed by the silicon substrate during cooling controls the position of the Pt (*hhh*) X-ray peak.

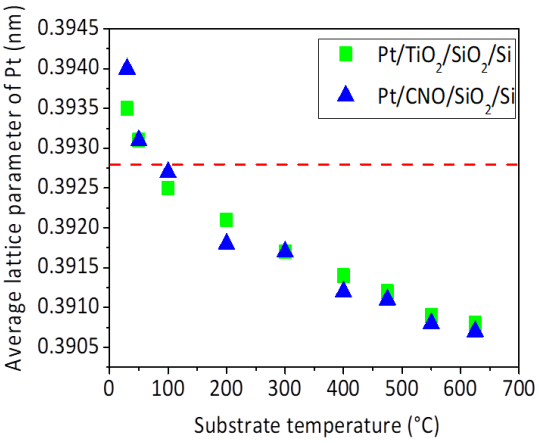

Figure 4: Influence of the deposition temperature on the Pt lattice parameter. Each point corresponds to the average value of the lattice parameter determined from the position of (111) and (222) peaks, except for films deposited at 30°C and 50°C ((111) peak only). The dashed line gives the value of the Pt bulk lattice parameter.

Figure 4 also shows that the Pt films have a lattice parameter close to that of bulk (0.3928 nm) for a deposition temperature of around 80°C. For a deposition at room temperature, the lattice parameter is larger than that of bulk, indicating that the film is subjected to a compressive stress in the plane. On the contrary, by increasing the growth temperature, the lattice parameter tends to decrease and becomes lower than the bulk one, which indicates an increase in the tensile stress in the plane. This is in agreement with the different thermal expansion coefficients of silicon ($\approx 2.6\ 10^{-6}\ K^{-1}$) and platinum ($\approx 8.8\ 10^{-6}\ K^{-1}$) [15].

The influence of the deposition temperature on the FWHM of the Pt rocking-curve is reported on figure 5.a). Each point corresponds to the average value of (111) and (222) FWHMs, except for films deposited at 30°C and 50°C ((111) peak only). The FWHM indicates the degree of misalignment of the crystallites relative to the normal of the film plane. At temperatures higher than 600°C, the Pt thin films are well crystallized on both seed layers and the FWHM is lower than 1.5°. When the substrate temperature decreases, the FWHM of Pt thin films deposited on TiO_2/Si increases regularly from 1.5° at 625°C to 5.5° at 200°C, while the FWHM remains very low, even at low temperatures, on the CNOns substrates (0.75° and 1.05° at 625°C and 200°C, respectively). Thus, the CNOns strongly reduce the deposition temperature required to obtain highly textured Pt films. Even at 100°C the FWHM is still around 2° on the CNOns, however the intensity of the (111) peak is reduced compared to 200°C, showing that the crystallization is less achieved.

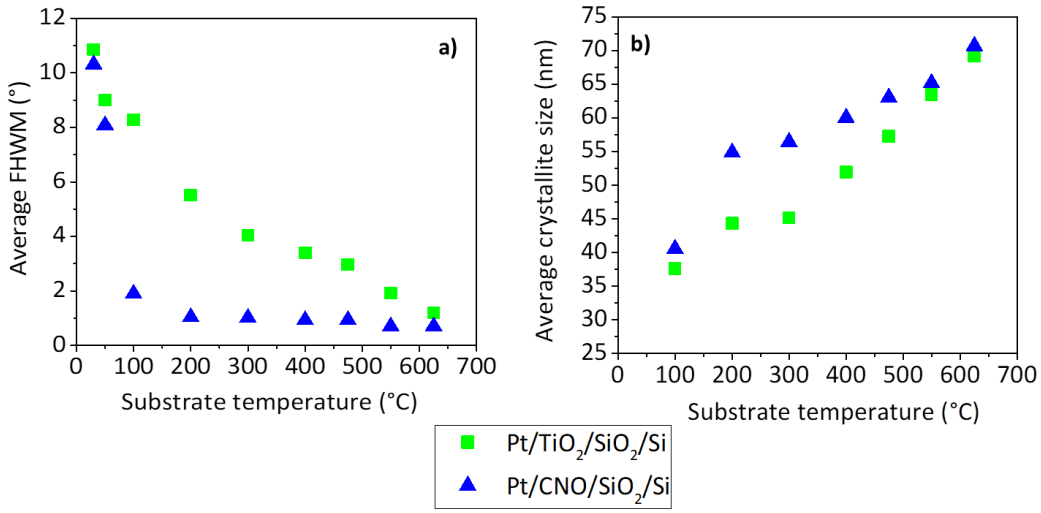

Figure 5: a) Influence of the deposition temperature on the average FWHM of the rocking curve of (111) and (222) peaks, except for films deposited at 30°C and 50°C ((111) peak only); b) variation of the average size of the crystallites determined using the Scherrer formula (on (111) and (222) peaks) as a function of the deposition temperature.

These results are confirmed in figure 5.b) which shows the evolution of the average size of the crystallites as a function of the substrate temperature. The size of the crystallites decreases when the temperature of the substrate decreases, varying from 71 nm at 625°C to 41 nm at 100°C for CNOns, and respectively from 69 nm to 38 nm with TiO_2. For a given temperature, the size of the crystallites of the Pt films deposited on the CNOns is always larger than that deposited on TiO_2. In addition, the difference in the size of the crystallites is more pronounced around 200°C which corresponds well to the large difference in FWHM (figure 5.a)).

Table I: Crystallites size (X-ray determined), grain size and roughness of Pt films (AFM determined) on both kinds of substrates. The accuracy of these values is about 5 %.

Deposition temperature (°C)	**Average crystallite size (nm)**		**Grain size (nm)**		**RMS roughness (nm)**	
	CNOns/Si	**TiO_2/Si**	**CNOns/Si**	**TiO_2/Si**	**CNOns/Si**	**TiO_2/Si**
625	71	69	306	271	1.9	2.5
550	65	63	288	245	1.1	2.3
475	63	57	241	156	1.2	1.6
400	60	52	120	117	2.1	1.8
300	56	45	76	61	1.6	1.6
200	55	44	70	59	2.0	1.3
100	41	38	50	51	1.9	1.1

Figures 6 and 7 show the surface of the Pt thin films deposited on TiO_2/Si and CNOns/Si, respectively, as observed by AFM. In both cases, the grain size decreases from 271 nm at 625°C to 51 nm at 100°C for the TiO_2 seed layer, and from 306 nm to 50 nm for the CNOns respectively (Table I). For high deposition temperatures (Ts > 500°C), the grain sizes determined from AFM were four times the ones determined by the Scherrer formula from XRD, but they tend to become similar at room temperature. The difference in grain and crystallite size is mainly because AFM is a surface measurement of the in-plane diameter of the grain, while XRD is sensitive to the volume. However, AFM measurements again show that the grains are larger on CNOns than on TiO_2. This increase in grain size and, to a lesser extent, in crystallite size are strong confirmation that crystal quality is improved using the CNOns. All these characterizations demonstrate that Pt thin films of high crystalline quality are obtained at very low temperatures on CNOns.

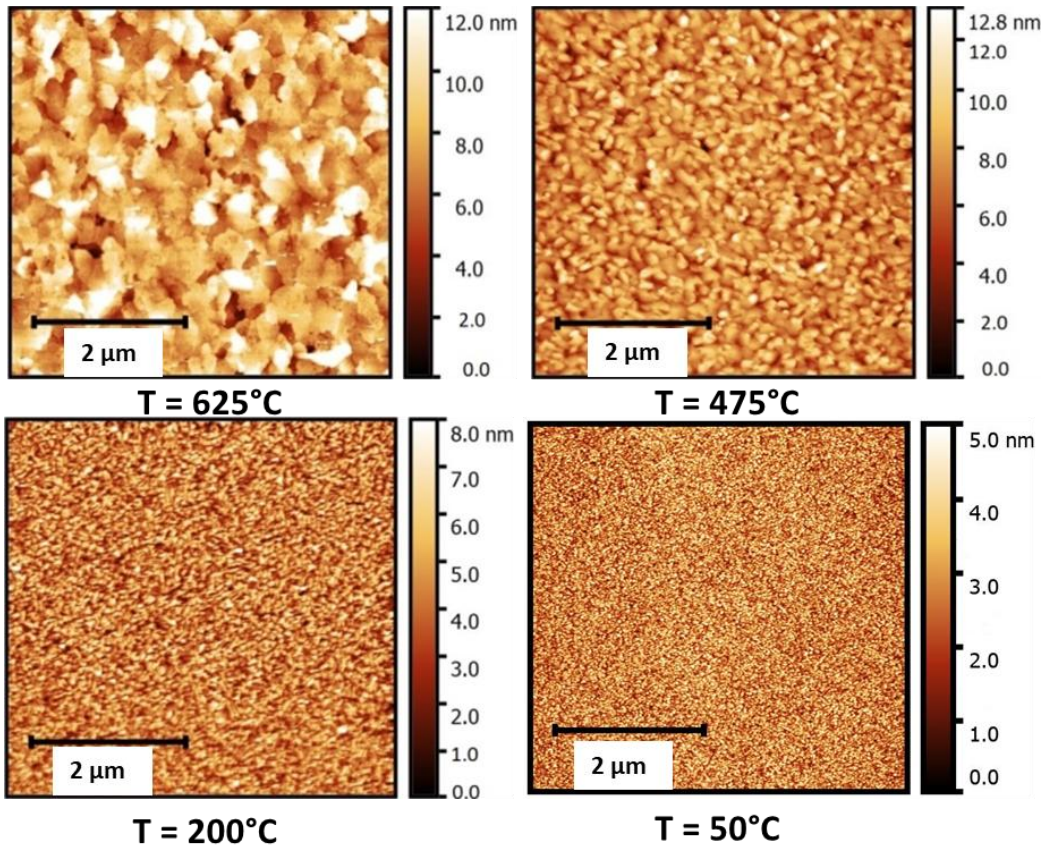

Figure 6: AFM images of Pt films deposited on TiO_2/SiO_2/Si at different temperatures.

In accordance with the variation in grain size, the RMS roughness of the Pt films increases almost continuously from 1.1 nm at 100°C to 2.5 nm at 625°C in the case of TiO_2 (Table I). The roughness of the SiO_2 layer covering the Si substrate is close to 0.2 nm. On the other hand, the roughness of the Pt thin films deposited on CNOns/Si varies between 1.1 and 2.1 nm regardless of the temperature of the substrate. This is probably due to the roughness of the surface of the CNOns before the deposition of Pt which has been found between 2 and 4 nm.

An important point is the influence of the coverage of the nanosheets on the crystallinity of the Pt films. For example, for Pt films deposited on CNOns/Si with a coverage as low as 20 % (temperature range 200°C-500°C), the FWHM increases to a maximum of 1.5°. This FWHM is again narrower than that of platinum deposited on TiO_2/Si, in the same temperature range. Consequently, the coverage of CNOns on SiO_2/Si is not a critical parameter for the deposition of high quality Pt thin films at low temperature. This also indicates that the crystallization of Pt on areas not covered with nanosheets is probably influenced laterally by areas coated with nanosheets.

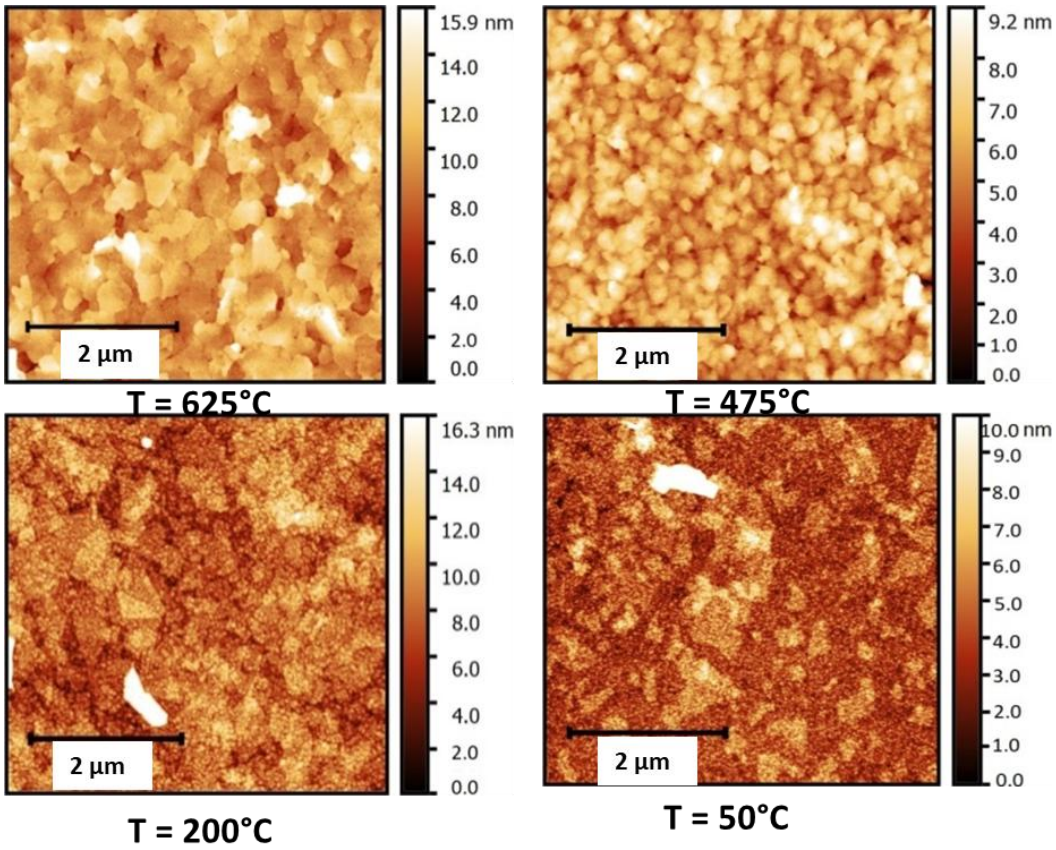

Figure 7: AFM images of Pt films deposited on CNOns/SiO_2/Si at different temperatures.

Figure 8 shows SEM images of cross-sections prepared in Pt films grown on CNOns/Si at room temperature and 625°C. The film deposited at room temperature, with a thickness of 90 nm, has well crystallized small grains (only several tens of nanometers-wide). These grains do not occupy the entire thickness of the film. The film deposited at 625°C has large grains of 50 to 200 nm in width, which have grown along the entire thickness (100 nm). These observations agree with AFM results: the grains present a nanometric size for films deposited at room temperature and large grains occupy all the thickness for films deposited at high temperature. The nanosheets are too thin to be seen on these cross-sections.

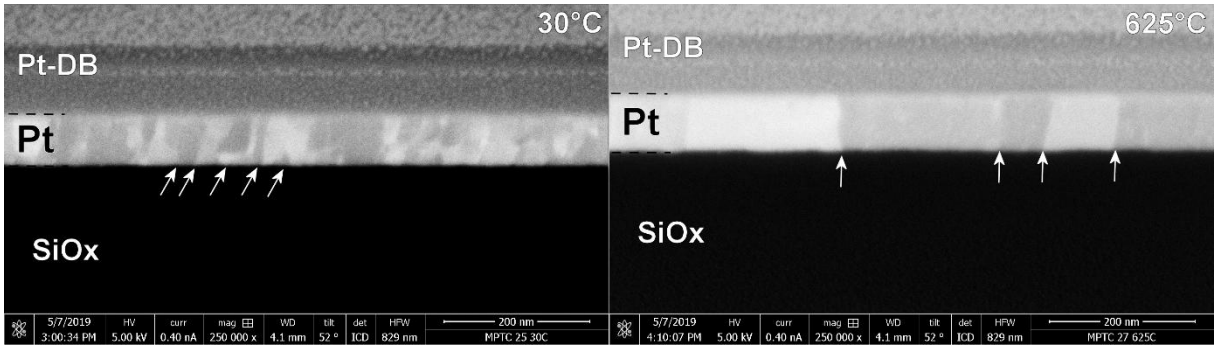

Figure 8: SEM images of Pt films grown on CNOns/Si substrates at room temperature and 625°C. Arrows highlight differences in grain size. Pt-DB stays for protective Pt-based film deposited in the DualBeam system.

3.2. Influence of deposition temperature on Pt resistivity

The resistivity of bulk platinum is 10.6 μΩ.cm and the resistivity of thin films is generally greater than that of bulk. Table II shows the resistivity values of the Pt thin films deposited on the two kinds of substrates at different deposition temperatures. The resistivity of the Pt films deposited at 625°C is 18 μΩ.cm on CNOns and 20 μΩ.cm on TiO_2 whereas the resistivity of the films deposited at room temperature is 22 μΩ.cm on TiO_2 and 24 μΩ.cm on the CNOns. Thus, there is no significant difference in resistivity for the two types of seed layers.

Table II: Resistivity of Pt films deposited at 625°C and at room temperature on the two kinds of substrates.

Substrate	**Substrate temperature (°C)**	**Pt film thickness (nm)**	**Resistivity (μΩ.cm)**
CNOns/Si	625 ± 10	100 ± 3	18 ± 2
	30 ± 5	90 ± 3	24 ± 2
TiO_2/Si	625 ± 10	110 ± 3	20 ± 2
	30 ± 5	95 ± 3	22 ± 2

The slight increase in resistivity at low deposition temperature can be related to the smaller grain size and therefore to the presence of more grain boundaries in the thin films. The decrease in the resistivity of Pt film as the deposition temperature increases had already been observed [3, 28-29]. Depending on the growth conditions, Sakaliuniene *et al.* obtained resistivities of the order of 25 to 85 μΩ.cm for Pt thin films deposited at low temperature on TiO_2/Si, and of 25 to 65 μΩ.cm after annealing [3]. Sreemany *et al.* [28] reported a variation of resistivity from 100 μΩ.cm at room temperature to 20 μΩ.cm above 500°C for Pt thin films deposited on glass. For Pt films deposited directly on SiO_2/Si, Lee *et al.* [29] measured a resistivity of 45 to 13 μΩ.cm for room temperature and 700°C, respectively. After a further annealing at 650°C, they obtained a resistivity of the order of 25 to 16 μΩ.cm, very close to our results.

Finally, the different seed layers used in this study do not significantly influence the resistivity of the films which are among the best compared to previous works, although the crystalline quality is clearly better with the use of CNOns. This higher quality of Pt thin films, that can be used as bottom electrodes, should promote the growth of oxide thin films and facilitate their integration on silicon substrates.

4. Conclusions

This study focused on the influence of $Ca_2Nb_3O_{10}$ nanosheets and TiO_2 seed layers on the crystallization and the electrical properties of 100 nm-thick Pt thin films deposited on silicon. The influence of the deposition temperatures ranging from room temperature to 625°C was investigated by XRD, AFM and SEM imaging. These characterizations have shown that the CNOns allow to reduce the Pt growth temperature down to 200°C, while retaining an excellent crystalline quality. The resistivity values are in line with the state of art (20 μΩ.cm) for the two seed layers. The possibility of growing high (111) textured Pt films of excellent crystalline quality on silicon substrates at low temperature (200°C) should facilitate the integration of complex oxides such as PZT with interesting dielectric and ferroelectric properties. These results confirm the advantage of using oxide nanosheets to produce seed layers which facilitate the growth of a wide variety of thin films on silicon.

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Authors declare no conflict of interest.

Supplementary information on a separate file.

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