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# **Study of suitable dielectric material properties for high electric field and high temperature power semiconductor environment.**

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« Device Characterisation », « Packaging », « Reliability »

## **Abstract**

Due to more severe operating condition (higher electric field, higher temperature,...), power electronics trends require to consider more accurately the dielectric environment of the semiconductor. The use of possible alternative semiconductors adds reason for such studies. Maximum electric field stress, relative dielectric permittivity and energy band gap properties, theoretically required for the SiC device passivation, are discussed. Advantages and drawbacks of high dielectric permittivity materials for passivation are emphasized. Then, a new 50 kV / 500°C experimental set-up allowing their precise characterization once the test-vehicles chosen, is presented in the paper.

## **1. Introduction**

A current trend in power electronics is to increase the integration level. The first main motivation lies in the reduction of these systems' sizes (volume and weight). Such a reduction represents energy saving for their transportation and also space saving, exploitable for new capabilities. This increase in volumic power requires components presenting both lower power losses and a smaller system complexity (for example a lower number of discrete components per function). An increase in both system efficiency and reliability is expected, which constitutes the second significant source of interest. Indeed, the research for power system integration includes (but is not limited to) other trends of the power electronics : higher operation frequency (leading to the size reduction of filters, capacitors, self and inductive machines), higher junction temperature (for both a decrease of the cooling system size and an increase of the switched power density), and power devices able to withstand a higher voltage (to avoid component series association, or for a direct power conversion from the distribution networks).

Therefore, power devices are expected to endure more severe operating conditions. These new stresses on the device constitutive materials impose to reconsider at the same time the system concept, the component architecture, the manufacturing technology processes, or even the material nature when physical limitations are reached. We can mention works on novel silicon structures (ex: CoolMOS [1], ...), and on new semiconductors (silicon carbide, gallium nitride, diamond [2], ...). These latter are

motivated by the silicon power devices limitations at high frequency (some kHz in railways applications) at high voltage (9 kV for rectifier diodes, 150 V for Schottky diodes) and at high temperature (ex:  $T_{Jmax}$  usually equals to 125°C (sometimes 140°C) for 3 kV to 6 kV fast switch diodes). A wide band gap energy, together with a high critical electric field, a good electron mobility and a high thermal conductivity, are suited semiconductor properties for significantly rising up the power device limits, as already demonstrated by numerous SiC demonstrators (19 kV bipolar diode in SF<sub>6</sub> gas [3], 2.6 kV-300°C on-wafer GTO [4]) and few commercial products (600 V-12 A-175°C Schottky diode in TO 220-2 case [5]).

In the semiconductor die environment, the dielectric materials, and more generally speaking, the whole packaging elements, have to follow these changes. These materials endure stresses which are induced either by external causes (the system (f, V, T) operating conditions) or internal causes (related to the semiconductor part). Among them we focus on the SiC-component passivation layer. This paper presents simulation results performed to quantify the theoretical electrical stress that this passivation layer has to withstand. On the other hand, this approach leads us to deduce the main physical properties that this layer has to present. A 4H-SiC P<sup>+</sup>NN<sup>+</sup> diode with Junction Termination Extension (JTE) periphery protection is considered in this study. Indeed, the planar JTE technique is often used, being efficient against premature breakdown of SiC devices ([3], [4], [6]).

Besides, since the interest in these new components is also their ability to operate in a higher temperature region than current ones, specific characterization means have to be built. The goal is to demonstrate the effective material abilities when high electric field and high temperature are applied at the same time. For this reason, an experimental set-up has been built allowing the measurements of material dielectric strength, or device breakdown voltage and leakage current, under voltage magnitudes and ambient temperatures up to respectively 50 kV and 500°C. This novel equipment principle, is presented in the second part.

## 2. Suitable material properties for the passivation layer of a SiC-component

### 2.1 Properties to be considered and method used for this study

#### Electric field distribution evaluation using two-dimensional finite element simulation

The first point to be considered is the increase in the **electric field value (E)** applied to the **semiconductor dielectric environment**. When a wide band gap semiconductor is considered due to its higher breakdown field ( $E_c$ ), the die surrounding materials have to endure higher electrical stresses. Indeed, to receive the highest system performance benefit for a targeted blocking voltage rating, the active device is designed to approach the maximum electric field value that the bulk of the semiconductor is able to withstand using the maximal doping level. Last, PN junction curvatures or interruptions, within the component or at its periphery, may create localized electric field reinforcement.

Maximum operating electric fields have therefore to be quantified in order to determine the lowest breakdown fields required for both SiC passivation and coating materials. The aim is to allow the maximal operating voltage of the whole structure to be as close as possible to the breakdown voltage of the semiconductor part (dimensioning concern), and to be stable versus time (reliability concern). For the present study, we focus our interest on the SiC device passivation layer, using the example of the 4H-SiC bipolar JTE-diode. The electric field stress impact on carrier injection at the interface between the passivation layer and the semiconductor die, has to be considered too, especially with an eye to increasing temperature operations. This second concern will determine the minimal band gap energy of the passivation layer material directly in contact with the semiconductor surface. The influence of  $\epsilon_{rp}$ , the dielectric relative permittivity, for a given thickness of the passivation layer  $t_p$ , has been mainly investigated as an important factor for the E field repartition both inside and outside the semiconductor, and for the reliability concern.

In order to evaluate this electric field distribution within and outside the semiconductor, **finite element simulation method** is applied, using MEDICI software [7]. It allows the description of the whole structure geometry under study, (including the semiconductor, the metallic electrode, the passivation

layer(s) and the insulating environment domains). The particular case of the  $P^+NN^+$  diode considered is presented in Fig. 1. After its geometrical description, the structure was meshed into finite elements to allow the calculation of electrical and physical quantities (like potential, electric field, charge carrier concentrations, current density, impact ionization rate, ...) at each grid node. Due to the necessity to fix appropriate boundary conditions and to include the semiconductor environment, the structure to be simulated becomes quite large (even when taking into account the device symmetry). The difficulty resides in setting a fine enough meshing, providing correct results while keeping the total number of calculation points below the software limit (around  $2 \times 10^4$  points at maximum). In the studied case, the chosen values for the extension of the epitaxy lateral margin ( $M=200 \mu\text{m}$ ) and for the insulating environment thickness ( $t=100 \mu\text{m}$ ) allowed an acceptable evaluation of the electric field distribution at the device sensitive areas.

The silicon carbide parameters were then provided for the physical models of the semiconductor region. The dielectric materials were declared as "insulator" regions, allowing to fix the dielectric permittivity parameter value (the other parameters, like electronic affinity, energy band gap, were kept equal to those of  $\text{SiO}_2$ ). Only the Poisson's equation was solved in these insulating regions. The electrical resistivity of these insulating regions is considered infinite. No effective semiconductor surface charge was taken into account in this work.

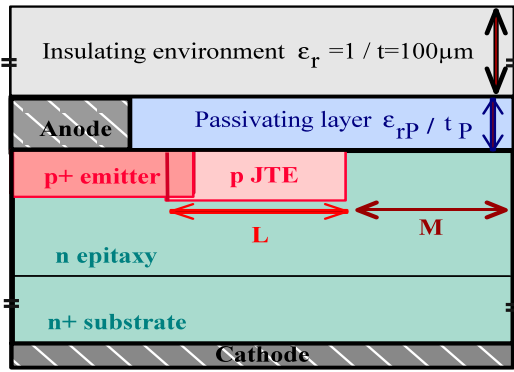


Fig. 1: Simulated high voltage  $P^+NN^+$  4H-SiC JTE diode with  $40 \mu\text{m} / 1.2 \times 10^{15} \text{ cm}^{-3}$  n-epilayer,  $0.5 \mu\text{m} / 4 \times 10^{19} \text{ cm}^{-3}$  p<sup>+</sup>-implanted emitter,  $0.4 \mu\text{m} / 1 \times 10^{13} \text{ cm}^{-2}$  p-implanted JTE, anode metal radius =  $92 \mu\text{m}$ , emitter radius =  $125 \mu\text{m}$ , JTE length  $L = 250 \mu\text{m}$ , epitaxy lateral margin  $M = 200 \mu\text{m}$ , simulated structure width =  $565 \mu\text{m}$ .

The geometry and doping levels specified in Fig. 1 correspond to the "optimal" design of the [SiC, insulating environment] system, in absence of any passivation layer, leading to a maximal breakdown voltage of 5.75 kV. This breakdown results from the carrier generation by impact ionization into the semiconductor at the emitter junction curvature). This particular structure is used as a reference point, for studying the effect of inserting different kinds of passivation layers on the E field distribution, and for evaluating theoretical requirements on their main properties.

#### Passivation capacitance evaluation using analytical calculation

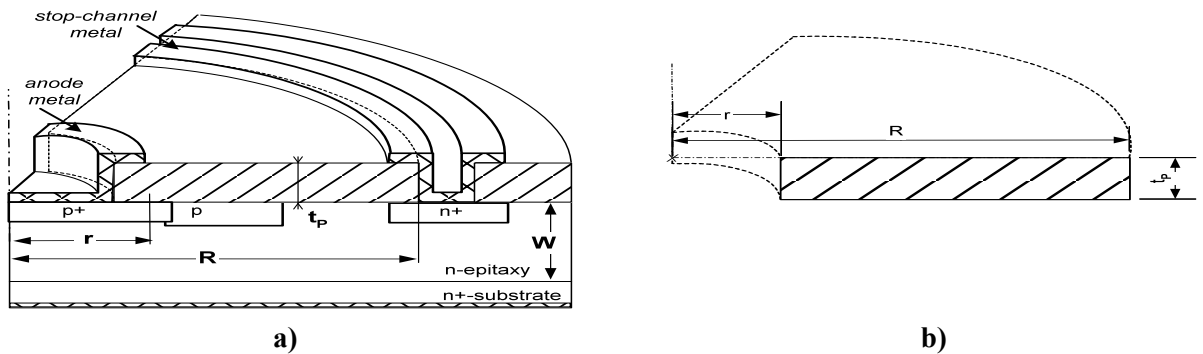


Fig. 2: **a)** Example of device (a circular  $P^+NN^+$  diode with stop-channel ring), and **b)** the equivalent cylindrical capacitor used for the capacitance analytic calculation.

Fig. 2a) presents an example of structure where the passivation layer may act as a parasitic capacitance  $C_p$  in parallel with the semiconductor blocking junction. This case corresponds to

a  $P^+NN^+$  diode with the passivation layer connected between the  $P^+$ -anode metal and the  $N^+$ -stop-channel ring metal.

In order to evaluate the impact of this  $C_P$  capacitance on the dynamic operating performance of the device, we considered that the passivation layer was equivalent to a cylindrical capacitor (Fig. 2b), and the following equation was used for  $C_P$  calculation :

$$C = \frac{2\pi\epsilon t_p}{\ln \frac{R}{r}} \text{ with } \epsilon = \epsilon_0\epsilon_r$$

## 2.2 Results and discussion

### Dielectric strength ( $E_{BrP}$ ) and relative permittivity ( $\epsilon_{rP}$ ) requirements for SiC device passivation

Fig. 3 presents an example of electric field lateral distributions at different altitudes near the semiconductor surface for the diode shown in Fig. 1, covered only with a  $t=100\text{ }\mu\text{m}$  /  $\epsilon_r=1$ -insulating environment, for the 5750 V reverse bias, which corresponds, in this case, to the SiC avalanche breakdown voltage.

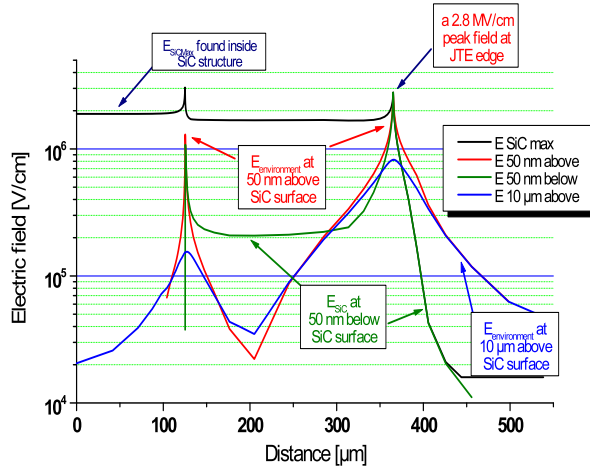


Fig. 3: Total electric field lateral distributions at different altitudes near and outside the SiC surface of the structure presented in Fig. 1 (50 nm below, 50 nm above, 10  $\mu\text{m}$  above), for  $V_{br}=5750\text{ V}$ . The black curve indicates the maximum electric field within the semiconductor part for each lateral X coordinate. This curve highest value is situated at the  $p^+$ -emitter junction curvature ( $X=+125\text{ }\mu\text{m}$  from the left,  $Y=+0.5\text{ }\mu\text{m}$  below the SiC surface).

As is shown in Fig. 3, one can observe first that the electric field distributions around the JTE-diode are strongly non uniform along an horizontal line.

The second observation arising from Fig. 3 is that the electric stress induced in this SiC diode environment can locally reach values close to 3 MV/cm. The E field maximum magnitudes outside the semiconductor are located close to the surface at the edge of the JTE. These values are about 10 times higher than the usual ones for Si devices, due to the fact that  $E_{cSiC}$  critical electric field is approximately 10 times higher than the Si one. It has to be noted that this enhanced stress occurs whatever the device voltage rating, so it is a common feature of all SiC structures. Moreover, using a higher  $E_{Br}$  semiconductor (like diamond) would lead to a further increase of the above stresses, reinforcing the interest of the study of the die environment. It should be added that the field peak at the JTE-edge can not be decreased by modifying the JTE-protection parameters, like increasing the JTE-length or depth (as checked by other simulations not shown here). Moreover, this peak magnitude being very close to the SiC critical avalanche field, the breakdown voltage of this kind of structure is very sensitive to the JTE doping process (a lightly higher doping level than the optimal value dramatically affects the breakdown voltage) [8].

From another hand, the table I gathers the critical electric fields given for different inorganic dielectrics already used or investigated as high relative permittivity ( $\epsilon_r$ ) gate dielectrics or secondary passivant in Si technology. This table also presents the so called operating electric fields for few of these materials. Before trying to compare these data with the maximum E field values around the SiC JTE-diode, several remarks have to be done. First, the  $E_c$  critical field values given in Table I generally correspond to the insulator dielectric strength measured using MIS (Metal Insulator Semiconductor) or MIM (Metal Insulator Metal) parallel plane configurations, and for a particular insulator thickness

(usually very thin for MIS applications). Also, the  $E_{op}$  operating field values (extracted from Lipkin et al. [9]) are derived from MIS structure characterizations as well. They generally correspond to the maximum field within the insulator above which excessive leakage currents were experimented, often related to charge carrier injection either from the semiconductor or the metal gate.

	$E_c$ (MV/cm)	$E_{op}$ (MV/cm)	$\epsilon_r$	$E_g$ (eV)
SiC-4H	2		9.7	3
SiO <sub>2</sub>	11	2	3.9	9
Si <sub>3</sub> N <sub>4</sub>	11	2	7.5	5.1
AlN	10-12	3	8.5	6.2
Al <sub>2</sub> O <sub>3</sub>	10		8.8-12	8.7
Ta <sub>2</sub> O <sub>5</sub>	9	0.3	24-26	4-4.5
HfO <sub>2</sub>	3-4		25	5.7
ZrO <sub>2</sub>	3-4		25	7.8
TiO <sub>2</sub>	6	0.2	40-80	3.5
BaTiO <sub>3</sub>			>150	3-4
polyimide	1.5-3	2.8-3.5		
parylene	2.1-2.8		2.65-2.8	

**Table I:** Critical electric fields, operating fields (extracted from [10]), relative permittivity and forbidden energy band gaps of commonly used or investigated materials for Si technology gate dielectrics or secondary passivation. Data come from [9], [10], [11].

So, the passivation dielectric stress is very different than the one of a MIS or MIM structure gate dielectric. In this last case, the electric field is uniform through the insulator, and normal to the interfaces with the semiconductor and the metal. Another important difference between these two dielectric configurations is the absence of the metal gate over the JTE-diode passivation zones where high  $E$  fields occur. Hence, no carrier injection from a metal can take place into the passivating dielectric. Moreover, the following results will point out the strong dependence of the electric field values in the JTE-diode environment on the relative permittivity ( $\epsilon_{rp}$ ) of the dielectric.

Fig. 4 presents the evolution of the distributions of the tangential ( $E_T$ ) and normal ( $E_N$ ) components of the electric field, at both sides of the semiconductor surface, for the same SiC structure as in Fig. 1. Four different cases are considered: with the [ $t_p=100 \mu m / \epsilon_r=1$ ] insulating medium alone (idem Fig. 3), with a [ $t_p=10 \mu m / \epsilon_{rp}=3.9$ ] passivation layer, with a [ $t_p=10 \mu m / \epsilon_{rp}=25$ ] passivation layer, and with a [ $t_p=10 \mu m / \epsilon_{rp}=100$ ] passivation layer. In all cases the passivant is covered by the same insulating ambient. The simulator solves the Poisson's equation alone in these cases, for the same 5750 V as in Fig. 3. N.B. : the theoretical continuity of the  $E_T$  component at the interface between two different materials can be checked in Fig. 4 ( by the superposition of the  $E_T$  curves 50 nm below and above the SiC surface).

Fig. 4 shows that the  $E$  maximum magnitude and position depend on  $\epsilon_{rp}$ . More precisely, an increase in  $\epsilon_{rp}$  leads to a decrease in the  $E$  magnitude at the edge of the JTE (reducing the normal component into the insulator but also the tangential one). It is related to a spreading of the equipotential lines at the JTE edge, further extending the space charge region at the device periphery surface. Simultaneously, however, an increase in  $\epsilon_{rp}$  value leads to an increase in the total  $E$  field magnitude at the edge of the emitter, due to a crowding of the equipotential lines in this area. The latter effect favors the carrier generation by impact ionization into the SiC crystal at the emitter corner. So a reduction or an augmentation of the diode SiC breakdown voltage  $V_{br}$  can result for a given  $\epsilon_{rp}$  value, depending on which effect is preponderant. The table II gathers the simulated  $V_{br}$  values, for which an infinite multiplication of the charge carriers is reached, due to the semiconductor impact ionization.

$\epsilon_{rp}$	1	3.9	25	100	200
$V_{br}$ (V)	5750	5450	5600	5750	> 5800

**Table II:** The JTE-diode SiC avalanche breakdown voltage  $V_{br}$  for different  $\epsilon_{rp}$  values of the passivating layer ( $t_p=10 \mu m$ ). (MEDICI simulator calculated the Impact Ionization Integrals).

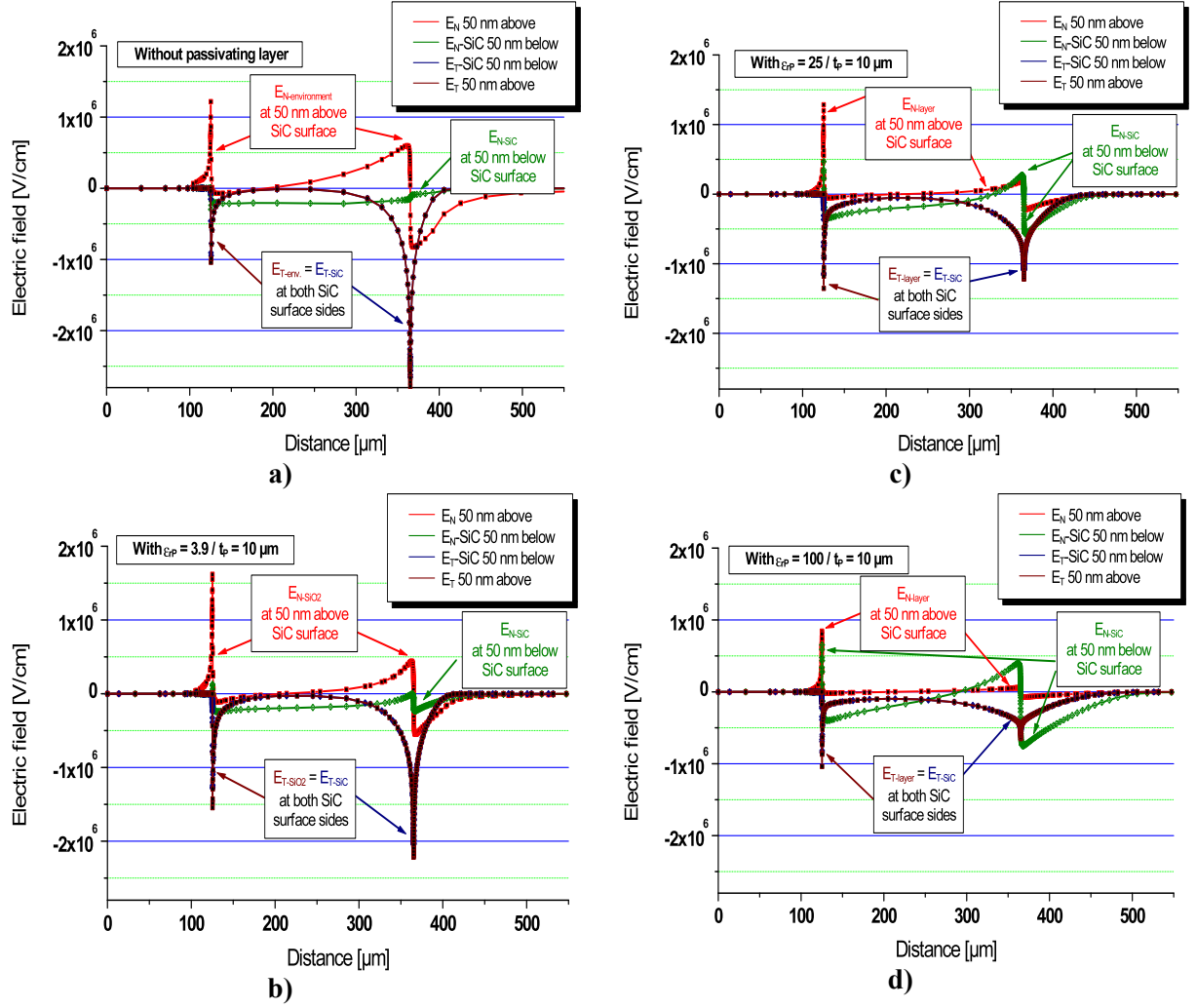


Fig. 4: Tangential ( $E_T$ ) and normal( $E_N$ ) electric field distributions, just below and above the semiconductor surface, for the same SiC structure as in Fig. 1 and bias as in Fig. 3. **a)** Without , **b)** With a [ $t_p=10 \mu\text{m}/ \epsilon_{rP}=3.9$ ], **c)** With a [ $t_p=10 \mu\text{m}/ \epsilon_{rP}=25$ ], **d)** With a [ $t_p=10 \mu\text{m}/ \epsilon_{rP}=100$ ], passivation layer. ( $E_T$  vector is positive when oriented towards the right,  $E_N$  vector is positive when oriented towards the bottom of the structure).

Thus, for the example of the JTE diode considered here, and assuming a zero effective surface charge density, the above observations show that a dielectric material exhibiting a  $\epsilon_{rP}$  permittivity superior to 100 would be required to reduce the high field stress at the JTE-edge, while keeping an elevated breakdown voltage of the SiC structure. Among the dielectrics studied in practice, only the perovskites like  $\text{BaTiO}_3$  are exhibiting an  $\epsilon_r$  property above 100. The local electric strength of this material should also be relatively large, the maximum magnitude of the  $E$  stress remaining quite high ( $6 \times 10^5 \text{ V/cm}$  near the SiC surface for a  $\epsilon_{rP}$  of 100, see Fig.4d). If such a material could be found, the  $E$  peak reduction at the JTE edge would also represent a weak sensitivity of the JTE protection technique towards the JTE doping dose increase. (N.B. : Though it can be noticed in Fig. 4 that an increase in  $\epsilon_{rP}$  induces at the same time an increase in the minimal  $E_T$  values along the SiC surface (located near the middle of the JTE), the related risk of surface flashover at high reverse biases can easily be corrected by properly designing the structure with a long enough JTE protection, as shown by other simulations).

For  $\epsilon_{rP} < 100$ , the materials listed in table I seem to exhibit enough large  $E_c$  critical field values, except for polymers (with  $E_c$  values  $< 3 \text{ MV/cm}$ ), to withstand the maximum electric field peaks in the



SiC JTE-diode passivation (assuming feasible such a comparison, which should be checked given that the mechanisms of conduction, or of degradation within the insulator might be different from those arising in MIS or MIM configurations).

The following paragraph aims to discuss the comparison of our simulation results with  $E_{op}$  values in Table I.

### **Band gap energy ( $E_{gp}$ ) and dielectric permittivity ( $\epsilon_{rp}$ ) requirements for SiC device passivation**

The impact of a charge carrier injection from the semiconductor into the insulating layer, is important as regards both leakage current and blocking voltage stability. Comparing the JTE-diode to the MIS configuration, *for a reverse bias below the SiC avalanche breakdown*, they are very fewer carriers susceptible to be injected into the passivant. This is because the semiconductor is depleted, and there is no facing metallic gate, in the zone where a high electric field is existing (assuming no inversion layer at the n-type epilayer surface). Therefore, the JTE-diode passivation seems less compelling than for the MIS gate insulation purpose with regards to this aspect. In addition, when increasing the  $\epsilon_{rp}$  value, the electric field near the surface at the dielectric side decreases (especially the normal component decreases), which is also favorable for a lower carrier injection level by Fowler-Nordheim tunneling. However, the actual benefit of the field reduction into the passivation might be compensated by the generally lower energy band offsets of such high  $\epsilon_{rp}$  materials with SiC, than the  $SiO_2$  ones (due to their thinner band gaps, see Table I and [12]). Smaller barrier heights facilitate the injection at lower electric fields. The effective benefit has to be investigated more in details before to conclude, for a given high  $\epsilon_{rp}$  dielectric.

*For the reverse bias responsible of the diode breakdown by avalanche multiplication in the SiC*, electrons and holes generation by impact ionization arises at the emitter junction edge. The existence of numerous and energetic carriers of both types could contribute to a significant injection into the passivating layer, and lead to possible charge trapping or insulator induced degradation. It is the electric field magnitude near the surface at the SiC side which is critical in this case. The reinforced electric field observed at the emitter edge surface when increasing the  $\epsilon_{rp}$  value (especially the  $E_{N-SiC}$  augmentation, as can be seen comparing Fig. 4a) and 4d)), could enhance the carrier injection even more facilitated by the lower energy band offsets associated to these materials.

The comparison of the  $E_{SiC}$  field magnitude shown in Fig. 4c) at the emitter edge for  $\epsilon_{rp}$  of 25, with the  $E_{op}$  operating field reported in Table I, indicates that dielectrics like  $Ta_2O_5$  or  $TiO_2$  would not lead to stable breakdown voltage of the passivated SiC JTE-diode (the normal component  $E_{N-SiC}$  alone is superior to the operating field). On the contrary for  $SiO_2$ , the  $E_{SiC}$  field magnitude at the emitter edge surface, which can be deduced from Fig. 4b at 5750 V, remains inferior to the 2 MV/cm reported in Table I. So the present simulation results reinforce the idea that  $SiO_2$  remains at the moment the best candidate for SiC-device primary passivation, thanks to its widest band gap, its very high critical field, and its current best interface quality with SiC. Due to relatively high energy gap and critical fields,  $AlN$ ,  $Al_2O_3$ ,  $ZrO_2$ , theoretically remain potential candidates to be envisaged.

### **Dielectric permittivity ( $\epsilon_{rp}$ ) influence on parasitic capacitance**

In order to evaluate the impact on the device dynamic operating performance of the device, of the equivalent passivation layer  $C_p$  capacitance in parallel with the blocking junction, we considered the following situation as corresponding to a worst case example : the width  $W$  of the structure n-type epilayer presented in Fig. 2a) was taken equal to 40  $\mu m$ , and supposed to be the thickness the junction space charge region capacitance; the diameter of the blocking junction was 1 mm (giving  $r \approx 0.5$  mm); and a 0.5 mm-length (giving  $R=1$  mm),  $t_p=10$   $\mu m$ ,  $\epsilon_{rp} = 500$  dielectric layer was considered.

The analytic calculation of the capacitance  $C_p$  show that it remains negligible, even for the considered high  $\epsilon_{rp}$  material value, and the low reverse biased junction capacitance  $C_{junc}$  ( $C_{junc} = \epsilon_{rSiC} \epsilon_0 \pi r^2/W$ ). In fact a  $C_p/C_{junc}$  ratio lower than  $10^{-3}$  was found for this instance.



Of course, the presented results remain preliminary and ideal to allow an effective design of the SiC JTE-diode passivation. The existence of surface effective charge (fixed or mobile charge, interface traps, ...) or insulator carrier traps, should be taken into account as first order parameters for E field distributions and breakdown voltage values. Besides, combination of SiO<sub>2</sub> and high  $\epsilon_{rp}$  layers, to try to receive both related advantages, and combination of several periphery protection techniques (including passivation layer with finite sheet resistance), have to be investigated by simulation, under static and dynamic conditions. Over all, viable practical solutions, exhibiting the suitable characteristics, while allowing process compatibility, and thermal stability, have to be elaborated and characterized.

### 3. Presentation of a 50 kV and 500 °C characterization set-up

Up to now, the classical range of study for materials or devices is limited in terms of temperature particularly when high voltage is required. In order to bypass these limitations a characterization set-up has been designed and built. This equipment consists of a 25 l-volume, stainless steel chamber, resistively heated (up to a 500°C ambient temperature), and able to withstand a 30 bar-internal pressure allowing high voltage to be applied up to 50 kV. Due to the small size of the samples or devices under test, one of the key concerns when applying high voltage is surface flashover. When working at room temperature or up to 200°C, samples are classically immersed in a dielectric fluid (oil, fluoroinert liquid,...). In some cases (for examples in switchgear) when a very high voltage is present and for important temperature conditions pressurized gases such as SF<sub>6</sub> or N<sub>2</sub>-SF<sub>6</sub> mixture may be used. In our case, since a temperature up to 500°C has to be reached, the liquid solutions have to be rejected and only the gas or vacuum solutions may be retained. For the sake of simplicity, a pressurized N<sub>2</sub> chamber able to withstand the required pressure for the desired voltage rating has been built. The test-cell is placed in the chamber and is connected to the external devices via one high voltage ceramic bushing and four coaxial connectors allowing low current and capacitance measurements. Monitoring and control of the internal temperature and pressure are fully automated and computerised.

A schematic diagram of this set up and a picture are presented in the figure 5. This complex system is still in a calibration and qualification procedure. The very first results will be presented during the conference.

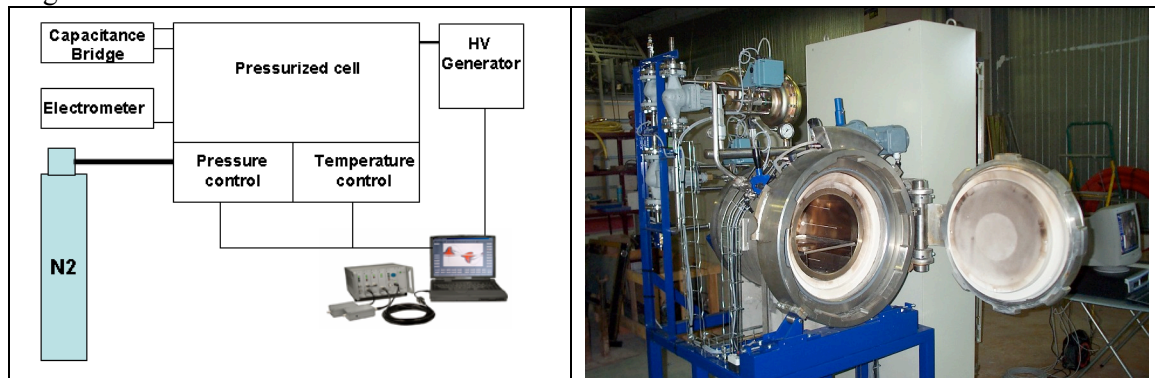


Fig. 5: High voltage (up to 50 kV) and high temperature (up to 500 °C) experimental set up.

### 4. Conclusion

Dielectric material properties, in terms of dielectric strength, dielectric permittivity and energy band gap, suitable for SiC device passivation have been analyzed using numerical simulation. Differences between passivation and MIS-structure requirements as regards insulating material characteristics are pointed out. Advantages and drawbacks of high dielectric permittivity materials for passivation are emphasized. The comparison between different dielectric materials is now possible but may also take into account all the trade off associated to a high voltage and a high temperature environment. Experimental characterizations under high electric field stress and high temperatures have to be performed in order to check the validity of the simulation and to achieve an appropriate dimensioning. The new characterization set-up allowing up to 50 kV voltage biases and 500°C temperatures, which will be a key tool for this type of study is presented as well.

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