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Fabrication and Characterisation of High Voltage SiC-Thyristors

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Abstract. Based on numerical simulations we fabricated thyristors on SiC with respect to different pulsed power applications. In order to achieve high breakover voltages we developed and investigated various types of terminations (MESA, EGR, JTE).
Thyristors, terminated by epitaxial guard rings (EGR), showed breakover voltage of up to about 1900 V. By dynamic electrical characterisations of the devices a reliable turn-on and turn-off could be demonstrated.

Introduction

The physical properties, above all its high electric field, good thermal conductivity and high temperature capability make SiC to be the top choice for high power semiconducting switches [1]. These properties could be used to design higher voltage devices with higher current densities in order to reduce the number of devices used in a switching system.
On the basis of numerical simulations published by N. Arssi et al [2] we designed a thyristor in reference to the studies for future pulsed power applications as reported by S. Scharnholz et al. [3] and E. Spahn et al. [4]. In order to define our devices, we looked about what is the state of the art for high power silicon thyristors.

Fabrication

Device Layout. Starting the simulation with a fixed point for the breakover voltage the structure for the thyristor was defined as in Fig. 1 to sustain a V_{BO} of 5 kV. The first simulations were done without including the periphery into the calculations. We only looked to the pn-junction which has to block the voltage. So, with an 35 µm thick low doped epitaxial blocking layer, different kinds of periphery protection were calculated like MESA, EGR and JTE.
The first device we realized had epitaxial guard rings (EGR's). In Fig. 2 shows a picture of the device displaying the layout of the structure with interdigitated gate and anode areas. The structures realized on the masks vary from 170 to 330 µm in length and 35 to 50 µm in width
Moreover, the number of fingers was varied and so the total anode area ranges from $0.7\text{x}10^{-3}$ to $5.7\text{x}10^{-3}$ cm^2. The sizes of the gate structures are varying in the same range as the anode.
The number of guard rings was set to five with a width of 12 µm and a distance of 2 µm. The guard rings are terminated by a trench with a width of 45 µm. These parameters were also defined by the simulation.
For the MESA protected devices we used the same variations for the size of the structures. The distance from the edge of the MESA to the anode structure was set to 13 µm as a minimum.

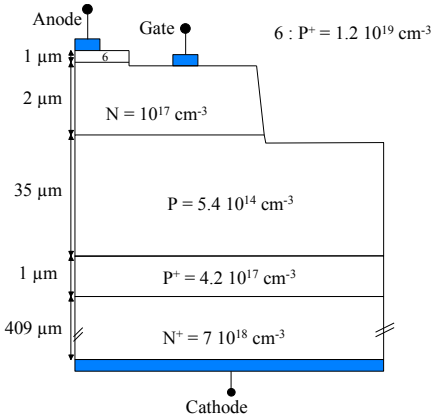

Fig.1: Half cell of the thyristor with the doping Level and thickness given by Cree™

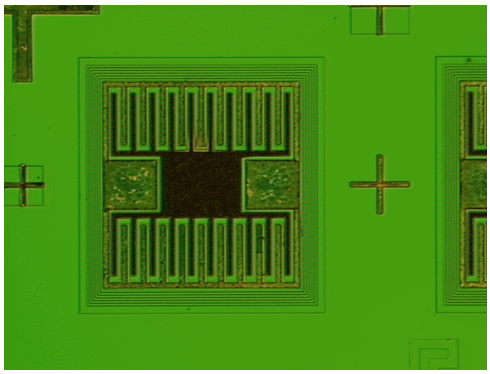

Fig. 2: Device with EGR termination (5 rings of 12µm width and a distance of 2 µm)

Process Flow. For the realization of the devices we used three different sets of masks, one for each kind of termination. In principle the process flow of all three terminations has the same sequence. The first step was to etch the trench for the gate contacts through the top epi-layer. The mask was a Ti mask or alternatively a Ti/Cr- mask for the ECR RIE etching. With this step the structure of the anode and also the alignment marks for the following steps were defined. The second step was to etch the termination area. We used the same etching parameters as before and the same mask metal. Fabricating the devices with EGRs we tried to stop etching accurately on the p drift layer. As contrast to this for the MESA and for the JTE devices we etched deep into the p layer. In the finished devices we obtained an over etching for the EGRs of 150 nm and a MESA of 1,3 µm into the p layer. The simulation shows that the breakover voltage is enhanced with increasing the MESA depth. Limited by the technical equipment we are not able to etch more than 1,3 µm deep in one step. Also as a result from the etching the sidewall angle of the structures vary from 93° to 98°.
The third step was to define the metal contacts for anode and gate after deposition of the passivation oxide. The oxide was deposited in two different ways. For the first samples we deposited 800 nm oxide by PECVD and for the second series a 1600 nm thick oxide was deposited by CVD at 900°C. The oxide was annealed in two steps with a final dry reoxidation as described from Scharnholz et al. [5]. The metal contacts for the anode consisted of a Al/Ti double layer. For the gate and the cathode we used a Ti/Ni double layer. The contacts where annealed at 1000°C for 180 s in an RTA furnace.
For the JTE there was an additional step for the implantation which required one more mask layer to define the implantation area in a deposited protection oxide.
Up to now we realised thyristors with an EGR and a MESA termination. The devices terminated by a JTE and a MESA with larger etching depth are still in process.

Characterisation

Blocking-state. The results shown in Fig. 3 are measured on a sample of the first series with devices having a MESA protection. In this particular case the etched MESA was 1,3 µm in depth. The maximum breakover voltage VBO measured on this sample was almost 1500 V. The measurement was done in oil to prevent a breakdown in air close to the surface of the devices. Because of the technological process flow, there was a small crack between the metal contacts and the passivation oxide. This was changed for the second series of samples.

In a second case we measured the breakover voltage VBO on samples with EGRs. This time the measurement was done with the samples put into perfluorinated fluid Galden™ HT270. As to be seen in Fig. 4 the breakover voltage amounts up to about 1900 V for these devices. The measurement was stopped when the leakage current reached 1 µA to prevent from a premature destruction.

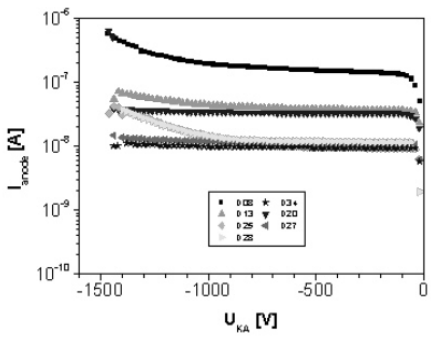

Fig. 3: Simulation of the dependence of the breakover voltage from MESA depth

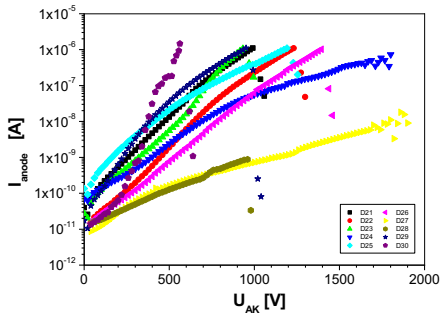

Fig. 4: Measurement of the breakover voltage with I_G = 0mA on different devices at room temperature

Switching. Applying a gate current pulse with a length of 1 µs an amplitude of at least 27 mA was necessary to switch on the devices. In Fig. 5 we show the gate pulse and the corresponding signals of anode-cathode voltage and the cathode current. Using the same pulse we could switch on the devices with anode-cathode voltages ranging from 45 V to 300 V. In all these cases the cathode current was limited to 100mA with series resistances ranging from 0,4 to 3 kΩ.

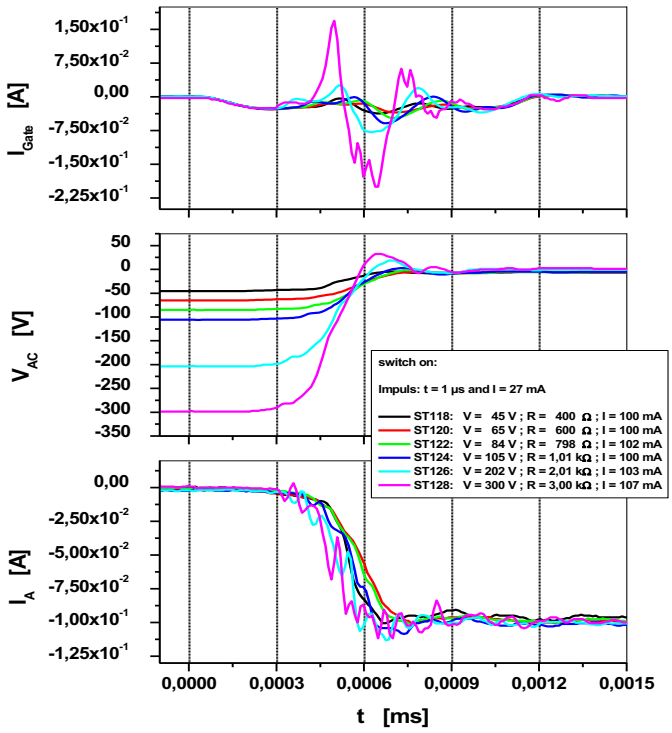

Fig. 5: Switching on by different anode cathode voltage and constant current

The switch-off of the devices was investigated by using a gate pulse of 1µs and a variable amplitude. With an anode cathode voltage of 100 V we switched off cathode currents of more than 60 mA. We also investigated the influence of the duration of the gate pulse on the switch-off behaviour. Therefore we vary the pulse length from 1µs up to 1 ms. To switch off a device with a

anode cathode voltage of 100 V and a cathode current of 100 mA we need a gate pulse amplitude of 61,5 mA for the short pulse and 43,5 mA for the long pulse.

Conclusion

Based on simulation results thyristors on SiC with different terminations were fabricated. We characterised the devices according to the breakover voltage as well as the switch-on and –off behaviour. The breakover voltage attains values up to 1900 V for devices terminated by epitaxial guard rings. Investigations concerning the switching behaviour showed that the devices could be turned on and off by short gate pulses.
Besides this the experimental results show a good correlation to the simulations. Based on this further simulations were performed showing that high power thyristors are feasible with the chosen design and process flow. Therefore future work will focus on the realisation of such high power devices on SiC.

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