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A 4H-SiC High Power Density VJFET as Controlled Current Limiter

D.Tournier, Ph. Godignon J. Montserrat
Centro Nacional de Microelectronica (CNM)
Campus UAB - Bellaterra, Spain
tournier@cnm.es

D. Planson, C. Raynaud, J.P. Chante
Centre de Génie Electrique de Lyon (CEGELY)
Villeurbanne, France

F.Sarrus, C. Bonhomme, J.F. de Palma
Ferraz Shawmut
Newburyport – MA, USA

Abstract — Considering fault current limiters for serial protection, a lot of structures exist, from regulation to other complex systems such as circuit breakers, mechanical switches or more conventional fuses. Up to now, only few semiconductor current limiter structures have been described in the literature [1]. Although Current Regulative Diode components already exist [2, 3], the voltage and current capabilities ($V_{BR}=100\text{ V}$, $I_{max}=10\text{ mA}$), do not allow to use them in power systems. This paper presents both simulation study and experimental results of a bi-directional current limiter structure based on a vertical SiC VJFET. This device was designed for serial protection in order to limit I^2t value. Finite-element simulations were performed with ISE-TCAD [4] to design the device and evaluate static electrical characteristics of the VJFET. Then, dynamic simulations were performed to underline current reduction ability and power losses adjustment by gate resistance value optimization. Finally, electrical characterization for an unidirectional and a bi-directional devices have been done up to 400 V. The measured specific resistance is in the range of $176\text{ m}\Omega\text{cm}^2$. Limiting capabilities have also been measured for a bi-directional device made of two unidirectional device connected head to tail. Highest breakdown voltage value in “current limiting state” were measured to be around to 811 V, corresponding to a high power density of 140 kW/cm^2 .

Keywords — Current limiter, JFET, serial protection device, high voltage, command integration.

I. INTRODUCTION

SiC semiconductor based devices are suitable for high current and high voltage applications [5,6]. A promising application of SiC-based devices is current limitation for power system protection [2,3], which benefits from its high thermal conductivity and wide band gap. Most of silicon components realized in SiC, Schottky diode, MOSFET, MESFET, show good electrical and thermal characteristics [6]. Few SiC-current limiter were presented [1,7]. This work is targeting the design, manufacturing and characterization of a new VJFET [9] (fig.1), which implement both gate and source

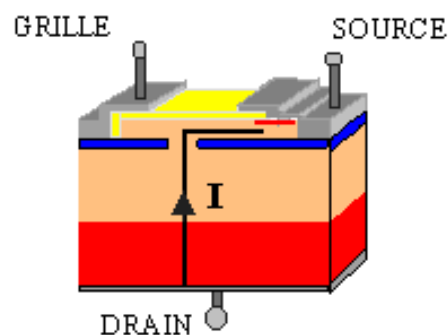


Fig.1. Cross section of the VJFET.

in buried layers. In the steady state, the voltage drop across the component must be as low as possible. In the active state, (limiting phase), the current limiter must sustain a high current, under high voltage bias. The resulting high power density must not cause component failure. We will describe the structure, the behavior of the component and the adjustable parameters. Then, dynamic simulations are discussed. Finally experimental electrical characteristics of both unidirectional and bi-directional are presented.

II. SiC VJFET CONTROLLED CURRENT LIMITER

A. Structure description

The novelty of this device consists in the design of the gate, which is formed by a buried layer. Fig. 1 shows the cross section of the α -SiC VJFET. This device has a channel divided in two parts: a vertical one and a lateral one. The source is grounded and current flows from drain to source. P-buried layers are designed so that the VJFET is a normally-on and presents a low specific resistance. When the drain voltage rises, the current saturates at a voltage corresponding to the pinch-off of both vertical and horizontal channels. In the saturation mode, the device presents an important on resistance (R_{ON}), resulting from the serial resistance of both

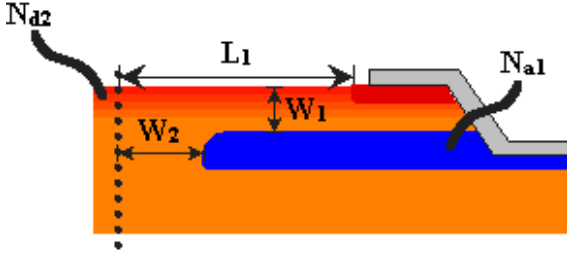


Fig.2. VJFET parameters to be optimized.

parts of the channel and the drift resistance of the epitaxial layer. Due to self heating, current decreases as the voltage increases (since electron mobility decreases and induces a current reduction). This effect is amplified while increasing limiting current density. When a negative bias is applied between gate and source, the PN junction formed by the Pwell and the epitaxial layer is reverse biased leading to current modulation. A trade off between specific resistance and blocking capabilities was investigated by simulations.

B. Static simulations

A global optimal parameter (eq.1) taking into account both doping concentration and geometrical dimensions (detailed in eq. 2) allow to get a range of parameters to be investigate by fine simulations.

$$Opt(W, Nd, L) = \max \left(\frac{g_0 \cdot g_{ms}}{V_p \cdot I_p} \right) (W, Nd, L) \quad (1)$$

$$g_{ms} = \frac{Z \cdot \mu}{L} (2 \cdot \epsilon \cdot q \cdot Nd)^{1/2} [V_p^{1/2} - (V_{di} - V_g)^{1/2}], \quad g_o = \frac{Z \cdot \mu \cdot q \cdot Nd \cdot a}{L}$$

$$V_p = \frac{q \cdot Nd \cdot a^2}{2 \cdot \epsilon}, \quad I_p = \frac{Z \cdot \mu \cdot q^2 \cdot Nd^2 \cdot a^3}{6 \cdot \epsilon \cdot L} \quad (2)$$

As an example, considering a channel doping concentration of $3 \cdot 10^{16}$ Atoms/ cm^3 , the optimal channel thickness is assumed to be around $0.4 \mu\text{m}$ (Fig. 3). To estimate peripheral effect on the electrical characteristics, finite element simulations are useful. In that case, different models are used, taking into account physical properties of silicon carbide. As the dissipated power can reach high values, the mobility temperature dependence is taken into account Tab.1. Most of parameters were given by Ruff [8] or are extracted from experimental results [9].

Main parameters to be adjusted are presented in Fig. 2. As an example, channel parameter N_{d2} has been investigated. Current density dependence and self heating effect are presented on Fig. 4 (both increasing while rising doping concentration). The simulated specific resistance R_d in the linear mode is in the range of $150 \text{ m}\Omega \cdot \text{cm}^2$ @ $V_{DS} = 1\text{V}$.

Finite simulations allows to stand a current dependence versus channel implanted doses. This let us choose a set of fabrication parameters considering for example the desired current saturation value (Fig. 5). Additional parameters such

as device breakdown voltage have been taken into account for the design of the final demonstrator.

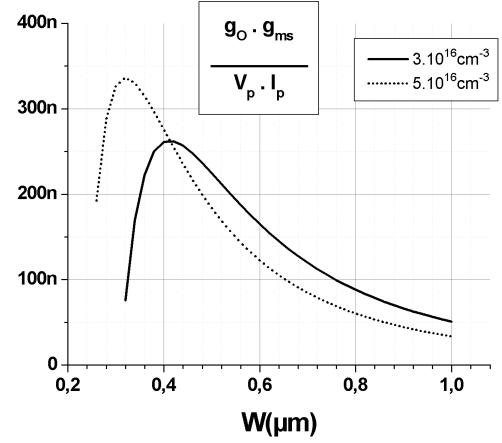


Fig.3. Optimal channel thickness estimation.

TABLE I. MOBILITY MODEL AND PARAMETERS USED FOR SIMULATION (CAUGEY THOMAS MODEL)

$$\mu_{n,p} = \mu_{\min 1} + \frac{\mu_{\max} \left(\frac{T}{300} \right)^\xi - \mu_{\min 2}}{1 + \left(\frac{N_i}{C_r} \right)^\eta}, \quad N_i = N_A$$

Paramètres	4H-SiC	
	μ_n	μ_p
$\mu_{\max} (\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{cm}^{-1})$	870	120
$\mu_{\min 1} (\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{cm}^{-1})$	0	0
$\mu_{\min 2} (\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{cm}^{-1})$	0	0
$C_r (\text{cm}^{-3})$	$2 \cdot 10^{17}$	$5 \cdot 10^{19}$
α	0,55	0,3
ξ	2	2

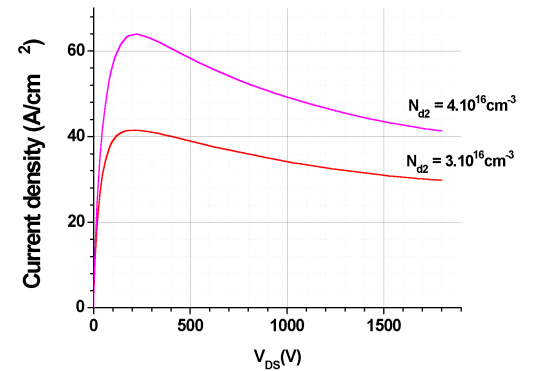


Fig.4. Influence of the surface channel doping on the current density and self heating effect.

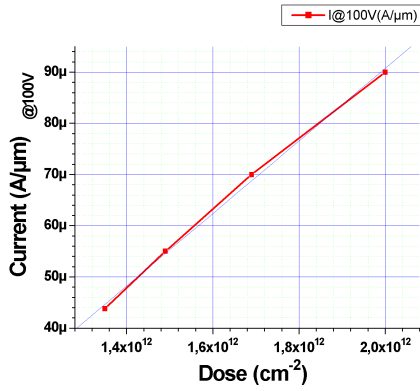


Fig.5. Saturation current dependence versus channel dosis.

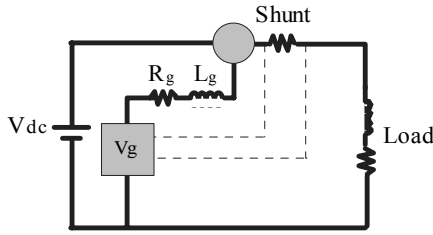


Fig.6. Electrical circuit for switching.

C. Dynamic simulations

Mixed-mode simulations using a spice circuit and finite element for the VJFET were done to evaluate switching performances of the circuit described on Fig. 6. Parasitic wiring inductance has been taken into account. Using a shunt for current sensing and an appropriate electronic command block allows to modulate the VJFET gate voltage to thereby reduce the current in the circuit. The simulated electrical circuit is presented in Fig. 7. Switching simulations were performed with a two step gate bias.

The first gate bias step underlines the current reduction ability ($V_{GS} = -10 \text{ V} @ t = 10 \mu\text{s}$). Then, applying a gate bias $V_{GS} = -40 \text{ V} @ t = 15 \mu\text{s}$ allows to shut down the current in the circuit as presented in Fig. 7. The switch off gate current is function of the gate resistance value and voltage rise time. Adjusting resistance value allow to control the gate switch off power losses, without effect on drain current value and switch off time, as shown in Fig. 8. Consequently, gate power losses and peak current are reduced of around 10% as resumed in table I.

TABLE II. COMMUTATION LOSSES AS FUNCTION OF R_G

R_G	$I_{Gmax} \text{ (A/cm}^2\text{)}$	$P_{off} \text{ (W/cm}^2\text{)}$
20	-0.41	0.146
30	-0.36	0.133

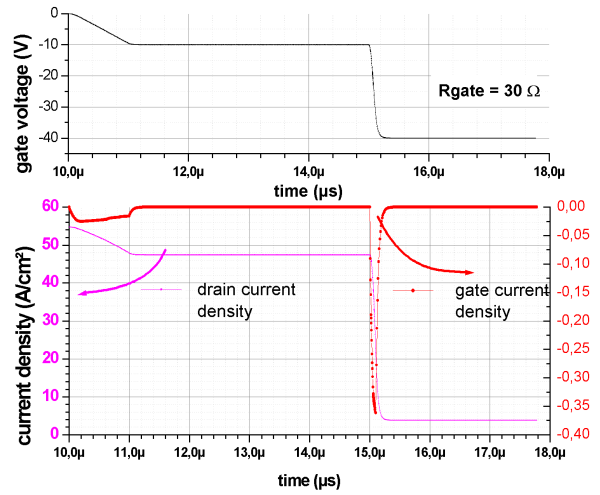


Fig.7. Current reduction and switch off waveform.

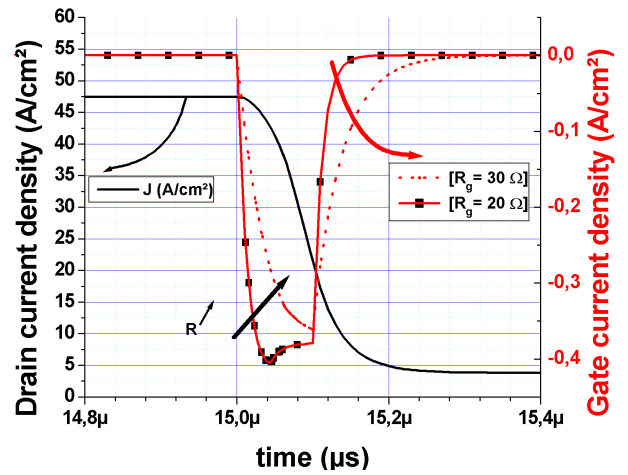


Fig.8. Switching off characteristics details for 2 R_{gate} values.

III. DEVICE FABRICATION AND CHARACTERIZATION

Various device layouts have been implemented (such as an interdigitated device presented in Fig. 9), to validate both the process technology, parameters adjustments and the device performances.

Key points of the device fabrication are high energy implantation, annealing activation and ohmic contact formation. State of arts values [6] of ohmic contact were measured on the first batch of VJFET fabricated ($\approx 10 \mu\Omega \cdot \text{cm}^2$).

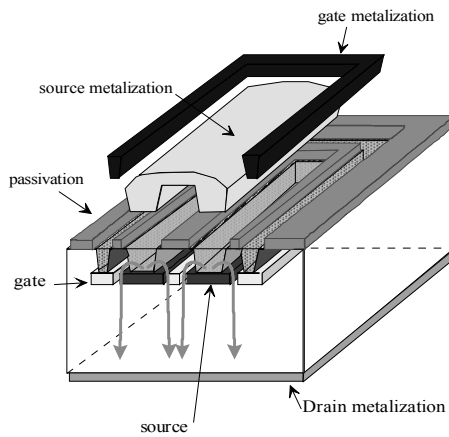


Fig.9a. Interdigitated structure cross-section.



Fig.9b. Fabricated interdigitated VJFET.

Fig. 10 presents the measured electrical characteristics for an unidirectional VJFET. Unidirectional measurements were done with 0,5 s pulse ($f = 2\text{Hz}$), with drain bias up to 400 V. The specific resistance varies from $176 \text{ m}\Omega\text{-cm}^2$ up to $237 \text{ m}\Omega\text{-cm}^2$ for the matrix structures. The maximum pulsed power density dissipated in the limiting mode is 160 kW/cm^2 . Limiting capabilities have also been measured for a bi-directional device made of two unidirectional devices connected head to tail (i.e. drain connected). This one exhibits a specific resistance of $700 \text{ m}\Omega\text{-cm}^2$. Highest breakdown in "current limiting state" were measured to be around to 811 V (Fig. 11), corresponding to a high pulsed power density of 140 kW/cm^2 .

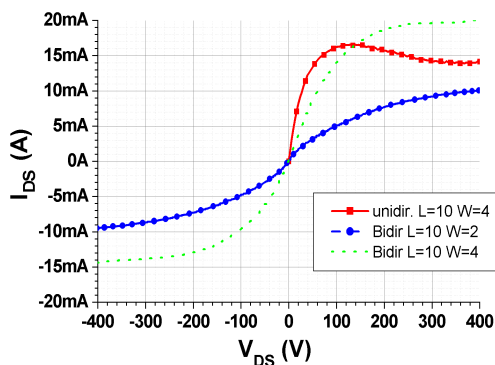


Fig.10. Electrical measured characteristics for unidirectional and bi-directional limiter.

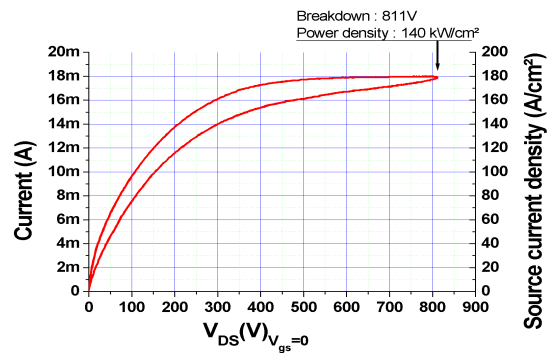


Fig.11 Unidirectional current limiter characteristics

IV. CONCLUSION

This work has demonstrated the feasibility of a SiC current limiter with high power density. The design was made using the ISE software with respect to the technological limitations. The first demonstrator measurements exhibit optimistic results. Bi-directional components were measured by associating two devices head to tail. SiC VJFET manufacturing process is compatible with SiC MESFET manufacturing process [10]. This allows to foresee the integration of a self controlled current limiter by an appropriated association of FET transistors. This device could be used in application such as current limitation in case of a short circuit of an electrical system. It could permit an elevation of the current ratings of classical mechanical device. Switching measurements will be made to validate both current sensing and gate bias voltage generation using the electronic control card.

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