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A Comparative Study of High Temperature Aluminum Post-Implantation Annealing in 6H and 4H-SiC, non-Uniformity Temperature Effects

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Abstract. 4H- and 6H-SiC small samples were implanted by keV Al⁺ ions at room temperature and annealed in an induction heating furnace, at the center of the susceptor, for different temperatures and times in the range 1600-1800°C and 5-60 min, respectively. The implanted layers were amorphous but the SiC crystalline structures were recovered after annealing, as measured by Rutherford Back-Scattering analyses in Channeling geometry.

Al⁺ electrical activation determined by sheet resistance and Hall effect measurements increases with the annealing temperature or time, on both polytypes. When whole SiC wafers were annealed in the same induction heating furnace, sheet resistance mapping systematically presented a radial gradient from the center to the periphery of the wafer. The measured linear dependence between sheet resistance and temperature allowed us to rebuild the radial temperature gradient at the crucible-susceptor furnace during the annealing process.

Introduction

Silicon carbide (SiC) is envisaged as a promising semiconductor material for a wide variety of high-temperature, high-power and high-frequency electronic applications. Ion implantation, an indispensable technique to locally dope silicon carbide still presents many problems in particular for p-type zone creation. High ionization energy of dopants imposes to raise the implanted dose above the amorphization threshold for room temperature implantations.

Structure recrystallization and electrical activation of dopants, i.e. their incorporation in active SiC atomic sites, require high temperature annealing, about 1700°C in special configuration, with an overpressure of silicon and carbide.

In this work p-type 6H and 4H-SiC layers created by Aluminum (Al) ion implantations followed by high temperature annealings are studied in order to realize efficient p⁺-n junctions for bipolar power diodes. Dopant electrical activation dependence on the post-implantation annealing conditions is discussed considering the non-uniform temperature at the SiC sample surface during this process.

Experiment

Al keV implantations were carried out at room temperature on the whole surface (5×5 mm²) of n-type 6H and 4H-SiC epilayers (doping level 10¹⁵~10¹⁶ cm⁻³), cut out from CREETM commercial wafers. A total dose of 1.75×10¹⁵ cm⁻² was implanted in misoriented samples to avoid channeling effects along SiC crystal axes.

Post-implantation anneals were realized in a SiC dedicated J.I.P.ELECTM induction heating furnace [1] at the center of the susceptor (Fig. 1). High heating ramp was used, 40°C/s, before to reach a constant temperature plateau in the 1600-1800°C interval, ranging from 5 min to 1 hour.

Physico-chemical analyses were made to observe the crystal recrystallization and doping profiles using Rutherford Backscattering Spectrometry in the Channeling geometry (RBS/C) and Secondary Ion Mass Spectroscopy (SIMS). The surface roughness (arithmetical) was evaluated by Veeco Dektak 3030 stylus profilometer.

Electrical activation was measured by a classical four-point probe technique directly on the implanted layers. For a more accurate approach of the electrical behavior of Al-implanted layers, Van der Pauw (VdP) geometries and Transmission Line Method (TLM) structures were realized on SiC wafers (1.375'' diameter) by a photolithographic process. P-type layers were thus investigated by sheet resistance (R_{sh}) and Hall effect measurements. The same ion implantation parameters were utilized, and a 1700°C during 30 min thermal annealing was carried out on these wafers.

Results and Discussion

RBS/C measurements performed on as-implanted samples illustrate spectral superposition for the 6H and 4H-SiC polytypes (Fig. 2). To convert energy to depth in RBS/C spectra a constant density value of SiC (3.21 g cm^{-3}) was assumed.

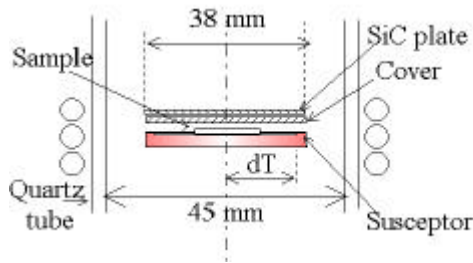


Fig. 1: Details of the chamber of the SiC rf-induction heating furnace

It is shown that a $0.3 \mu\text{m}$ layer (just under the surface) has been amorphized, the implant dose being superior to the threshold of an amorphous layer formation [2]. The amorphous layer is found larger if the density of amorphous SiC (2.9 g cm^{-3}) is considered.

After annealing, a weakly better recrystallization is observed for 6H-SiC samples. After 1700°C annealing during 30 min the backscattering yield is 5.8% for the 6H-SiC sample and 6.3% for 4H-SiC sample, that proves nevertheless good crystallinity after annealing in both cases.

As verified by SIMS analyses (Fig. 3) on as-implanted and annealed samples compared to Monte-Carlo simulations, no dopant losing occurs after high temperature annealing.

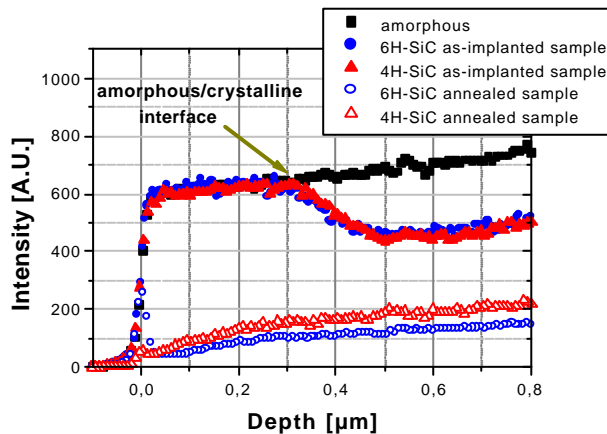


Fig. 2: RBS/C spectra on Al as-implanted and 1700°C during 30 min annealed 6H and 4H-SiC samples (the density of SiC has been assumed to be 3.21 g cm^{-3} (value for crystalline SiC)).

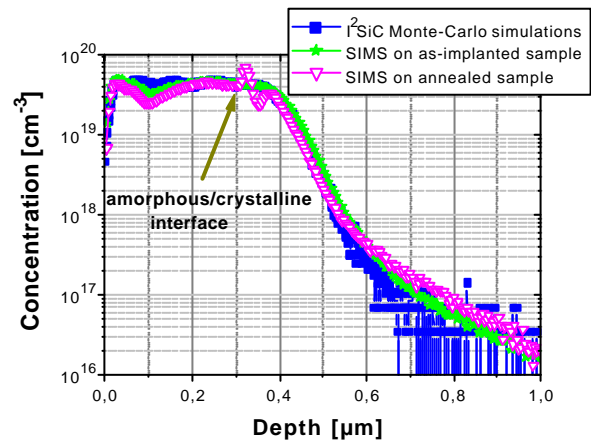


Fig. 3: SIMS analyses in as-implanted and 1700°C during 30 min annealed 6H-SiC samples, compared to $i^2\text{SiC}$ Monte-Carlo simulation [3]

Al dopant accumulation peaks are formed after annealing (Fig.3) just below the amorphous-crystalline interface. When an amorphous layer is created by ion implantation, defects named as end-of-range defects are formed just below the amorphous-crystalline interface, in the crystalline material. An interstitial over-

concentration formed after ion implantation generates into extrinsic dislocation loops during the annealing process. These defects associated with strain fields may act as gettering sites for Al implanted dopants during the same annealing process [4].

It is also important to note that the roughness of the sample surfaces after annealing increases with the temperature and the annealing time, this process becomes excessive for temperatures and times superior to 1700°C and 30 min.

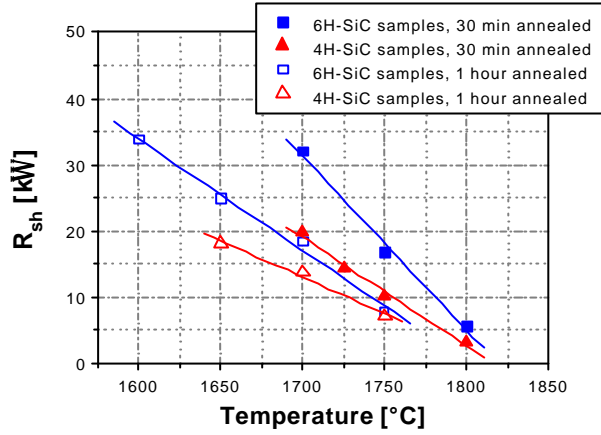


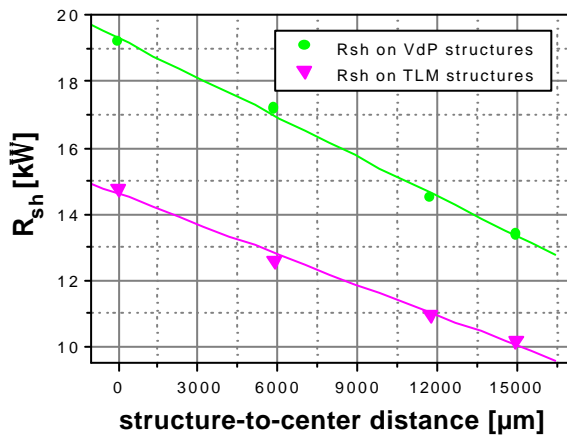
Fig. 4: Sheet resistance variations with annealing temperature for 30 min and 1 h annealing duration, measured at RT by four-point probe technique.

Electrical activation of dopants on implanted and annealed samples was investigated by R_{sh} measurements with a four-point probe technique. R_{sh} decreases when the annealing temperature or the annealing time increases. In Fig. 4 R_{sh} variations with the annealing temperature are represented, for 30 min and 1 hour annealing times. The weaker values for the sheet resistance on the 4H-SiC are mainly the consequence of weaker ionization energy of the Al dopants in 4H-SiC rather than a better electrical activation after high temperature annealing [5].

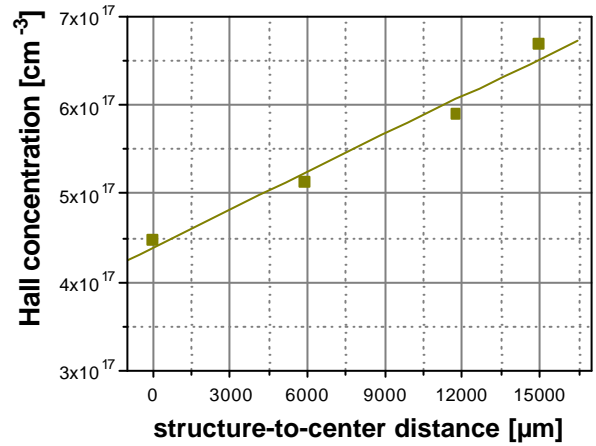
The linearity of the R_{sh} variations proves a non saturation of electrical dopant activation, nevertheless regression lines intersect temperature axe between 1800°C and 1820°C for the 4H-SiC and 6H-SiC samples, which

illustrates that these annealing conditions lead to nearly complete Al dopant activation.

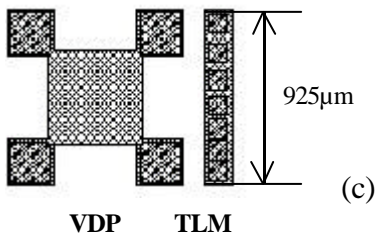
R_{sh} measurements made on VdP or TLM structures of SiC wafers show a linear dependence with the distance between the tested structure and the center of the wafer. Figure 5 presents results obtained on the 4H-SiC wafer. Similar results were found on the 6H-SiC samples. Sheet resistance found by TLM measurements must be corrected by a geometrical factor.



(a)



(b)



(c)

Fig. 5: Sheet resistance measured on VdP and TLM structures (a) and hall concentration variation (b) on a 4H-SiC wafer annealed at 1700°C during 30 min. Top mask view of VdP and TLM structures (c)

A good agreement is found between the sheet resistance measured on the VdP structure placed at the wafer center (19.2 k Ω in Fig. 5a) and the values obtained by four point probe technique on 5 \times 5 mm² whole surface implanted samples, annealed in the susceptor center (19.7 k Ω in Fig. 4). The linear variations of R_{sh} on VdP wafer structures compared with the results presented in Fig. 4, i.e. the linear relationship between R_{sh} and the annealing temperature, involve an almost linear temperature variation at the surface of the susceptor, due to the induction heating system. The temperature increases from the center of the susceptor to its periphery. The difference of 30°C between the center and the wafer periphery, evaluated by fitting R_{sh} linear variation with the temperature (Fig. 4) and the R_{sh} measured on VdP structures (Fig. 5a), is in agreement with thermodynamic calculations of the susceptor induction heating process (Fig. 1).

As a consequence and confirmation of this temperature distribution, we observed that the roughness of the wafer increases from the center to the periphery.

SIMS measurements realized locally in p-type implanted regions (VdP structures) show that the dopant profile does not depend on the structure-to-center distance. Therefore the decrease of the sheet resistance from the center to the periphery is attributed to the electrical activation of implanted dopants, which increases following the susceptor temperature variation during the post-implantation annealing process.

A linear variation of the carrier concentration is also determined by Hall effect measurements (Fig. 5b) at room temperature, the mobility values preserving a rather constant value (18 cm²V⁻¹s⁻¹). High values of hall concentration involve a good electrical Al dopant activation.

Conclusion

Aluminum implantation at RT was analyzed in 6H and 4H-SiC using high temperature annealings in an induction heating furnace. Amorphous layers are well recrystallized and no dopant loosing occurs after annealing. Electrical activation of aluminum increases when the annealing temperature or the annealing time increases, complete activation has been found both for 6H and 4H-SiC for annealing at about 1800°C during 30 min. Based on these results and the electrical activation distribution maps on SiC wafers, measured on VdP structures, we have determined the radial temperature gradient to be ~30°C, the periphery being hotter. Radial temperature gradient at the surface of the susceptor induces a better electrical activation of Al-implanted zones annealed at the periphery of the susceptor. To avoid non-uniform temperature effects susceptor has to be remodeled. Otherwise this effect has to be considered in device realization.

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