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Simulation study of a novel current limiting device : a vertical α-SiC JFET – Controlled Current Limiter

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Keyword : Current limiter, JFET, serial protection device, high voltage.

Abstract :

Considering fault current limiters for serial protection, a lot of structures exist, from regulation to other complex systems such as circuit breakers, mechanical switches or more conventional system : fuses. Up to now, only few semiconductor current limiter structures were described in papers [1]. Although Current Regulative Diode components exist [2, 3], the voltage and current capabilities (V_{BR}=100 V, I_{max}=10 mA), do not allow to use them in power systems. A comparison of a silicon Current Regulative Diode (CRD) and an equivalent SiC one demonstrates the thermal and electrical limitations of silicon. This paper deals with a novel bi-directional current limiter structure based on a vertical α-SiC VJFET, with both buried gate and source. This device was designed for short circuit protections. Simulations were performed with ISE-TCAD [4] to evaluate static and transient electrical characteristics of the VJFET, according to several specifications : voltage capability, current rating, time during which the device can sustain a short circuit. Simulations allow geometrical design and doping profile estimation as well as the technological process to realize such a component. Both 6H and 4H-SiC Controlled Current Limiter (CCL) have been realized. Electrical characterizations of fabricated devices underline the limiting effect and the command ability.

1. INTRODUCTION

Silicon carbide, thru its electrical properties allows to foresee the realization of new power components with higher capabilities than silicon. Its band-gap energy (E_g=3eV@300K) and its high critical electric field ($E_c = 2\cdot10^6$ V/cm) allow to make components such as diode with reverse voltage capability up to 6,2 kV [5].
Moreover its thermal conductivity (λ = 4,9 $W\cdot cm^{-1}\cdot K^{-1}$) allows components to work with high current density and under high temperature. Most of silicon components have been realized in SiC and show good electrical and thermal characteristics like Schottky diode [8], MOSFET [9], MESFET… As in steady state, the voltage drop across the component must be as low as possible, in the active state, (limiting phase), a current limiter must sustain a high current, under high voltage bias. The resulting high power density must not cause the failure of the component. Silicon carbide authorize to work at high temperature and high voltage and is a good candidate for the design of a new current limiter for high voltage and high current.

2. CURRENT LIMITATION : COMPARISON OF Si AND 6H-SiC CRD as DEVICES

2.1 Current Regulative Diode : Structure Description.

(CRD) [1] are currently used to limit current in low power applications. The current limitation is based on field effect. A cross section of the simulated device is presented in Fig.1 . When applying a positive voltage on the cathode, the extension of space charge in the preformed channel region (6) will cause the current saturation.

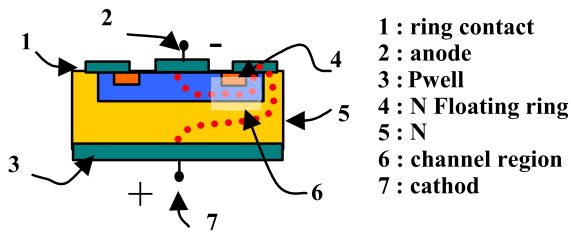

Fig. 1 Cross section of a silicon CRD.

2.2 CRD : Simulations and Comparison Between Si / SiC.

Simulation comparison of Si and 6H-SiC CRD like components were performed with ISE-tcad software to estimate the potentiality of this kind of device to realize a high voltage and high current CCL. The figure 2 shows the electrical characteristics comparison of the simulated silicon device and the equivalent silicon carbide one.

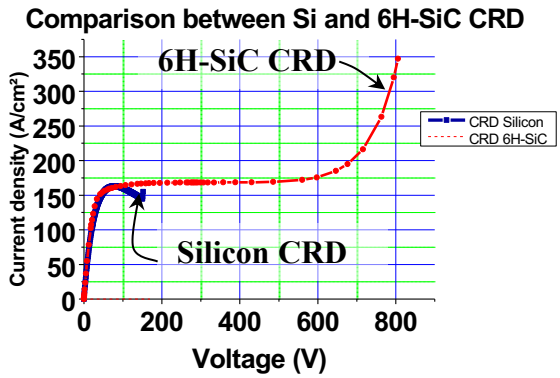

Fig 2. CRD simulated characteristics.

2.3 Conclusion :

Considering the self heating of the CRD silicon device, thermal limitation induces low voltage capabilities. For the same specific resistance, limitations appear : the avalanche breakdown voltage (V_{BR} = 120 V), and thermal limitation of silicon (T = 480 °K). For the SiC device, good electrical characteristics could be envisaged (with high breakdown voltage value) but require difficult technology steps such as the realization of a deep p-well difficult with SiC technology. For those reasons, vertical unipolar SiC structure were investigated in order to design a component with a low specific resistance, high voltage breakdown (>1kV) and high current capability.

3. α-SiC VJFET Controlled Current Limiter.

3. 1 Structure description.

Several current limiters have been recently presented, based on vertical MOSFET structure [9]. The novelty of this device consists in the design of the gate, which is formed by a buried layer. The figure 3 shows the cross section of the α-SiC VJFET. This device presents a channel divided in two parts : a vertical one and a surface one. When the drain voltage rises, the current saturates at a voltage corresponding to the pinch off of the vertical and horizontal channels. In saturation mode, the device presents an important on resistance (R_{ON}), resulting from the serial resistance of both parts of the channel and the drift resistance of the epitaxial layer. In saturation mode, as the voltage V_{DS} rises, the extension of the space charge in the epitaxial layer leads to a modification of the vertical

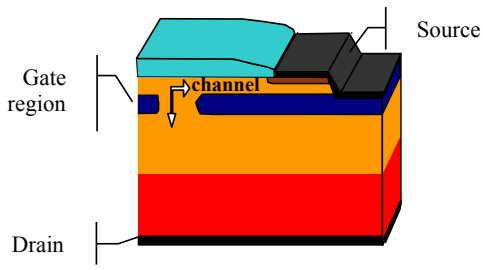

Fig.3 Cross section of the VJFET

channel length resulting in a slope on the electrical characteristics. Due to the self heating as the voltage increases (electron mobility decreases and induces the current reduction). This effect is enhanced while increasing current density. Simulated characteristics are presented below.

3. 2 α-SiC VJFET : Simulations

For the simulation of the upper structure, different models are used, such as the carrier mobility and ionization coefficient models. Most of parameters were given by Ruff [11]. The P buried layers are designed in such a way that the component presents a normally on electrical behavior. Main parameters to be adjusted are presented in figure 4.

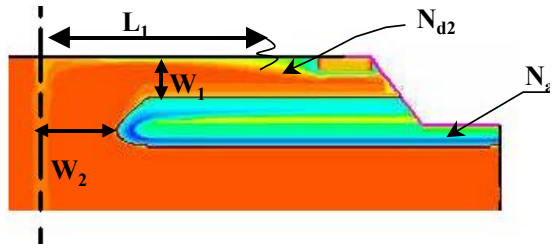

Fig. 4. VJFET parameters to be optimized.

Doping concentration of the epitaxial layer, were first adjusted to sustain required voltage. Then channel parameters have been investigated as presented on figure 5.

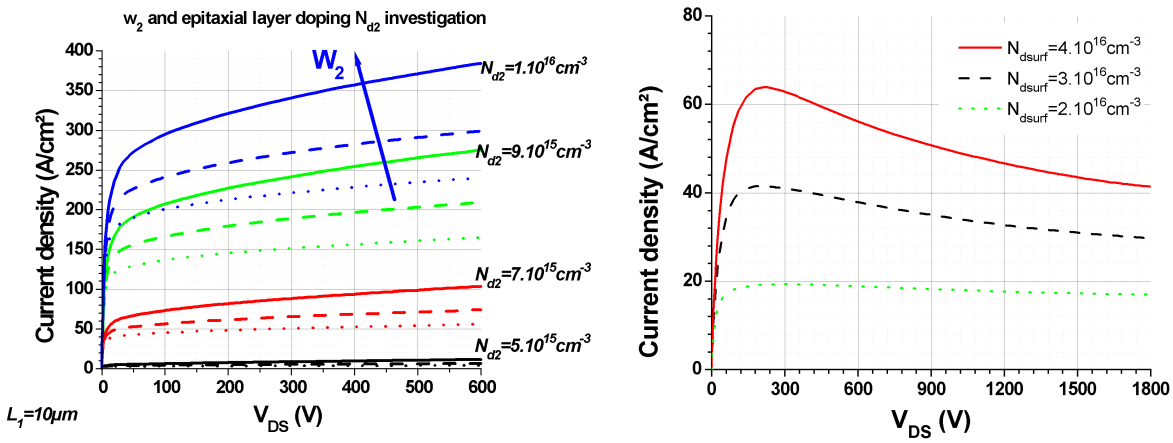

Fig.5-a Epitaxial layer investigation Fig.5-b Surface channel adjustment.

Fig. 5 Electrical simulated characteristics

Other parameters such as passivation layer effect have been investigated (fixed charge effect on the channel). The simulated specific resistance R_d in the linear mode is in the range of 150 mΩ·cm² @ $V_f = 3V$. The optimal solution for a current limiter is to find a trade off between R_d, V_{br}, V_{sat}, I_{sat}. The novel gate structure allows to control the current in the VJFET. When a negative bias is applied between gate and source, the PN junction formed by the Pwell and the epitaxial layer is reverse biased. Simulation results give : at a bias voltage of $V_{DS} = 40$ V, a current density of 50 A/cm², a bias voltage of $V_{GS} = -42$ V allows to stop the current.

3.3 Device fabrication and characterization

P wells are assumed to be realized by high energy ion implantation (2 MeV). The width of the vertical channel is determined by the implantation mask and the lateral dispersion of the implanted impurities. The implantation doses and energies are adjusted with Monte Carlo simulations [10] in order to define a surface channel of an average depth of 0.5µm. Source and gate contacts are assumed to be realized by RIE etching, stopped into P buried layers. The epitaxial layer is determined to sustain a V_{BR} reverse voltage of 1750V.

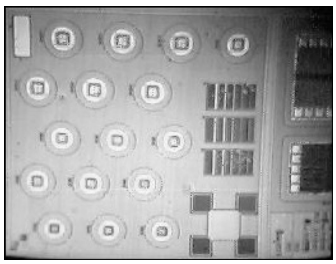
Fig.6 view of fabricated device and test structures.

The figure 7 presents the measured electrical characteristics for an unidirectional and a bi-directional device. Unidirectional measurements were done with 0,5s pulse (f = 2Hz), with drain bias up to 400 V. The specific resistance is in the range of 176 mΩ·cm² up to 237 mΩ·cm² for matrix structures. Figure 7 highlights the power sustaining ability up to 400V.The power density dissipated in the limiting state can reach a value of 160 kW/cm². Limiting capabilities have also been measured for a bi-directional device. This one exhibits a specific resistance of 700 mΩ·cm² and a limitation current up to ± 400V (with no gate bias applied).

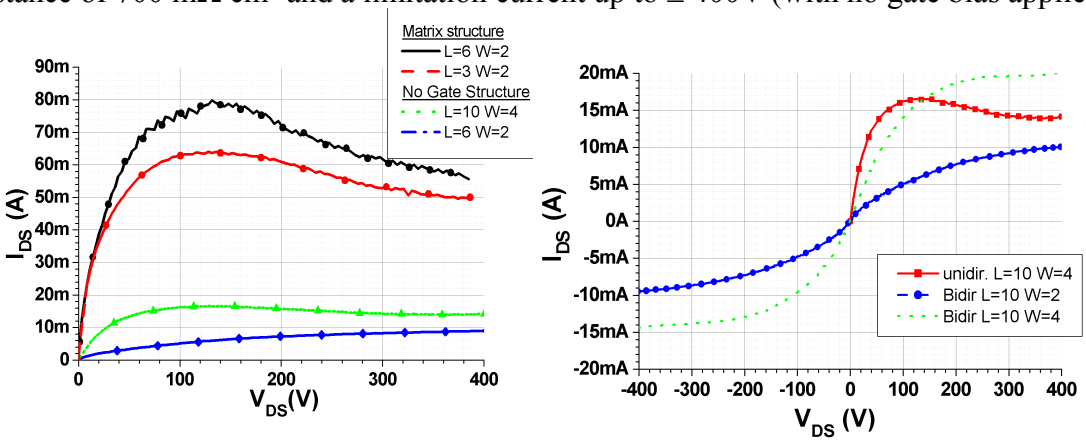

Fig.7. Electrical measured characteristics.

Conclusion :

This work has demonstrated the feasibility of a current limiter which could be used for serial protection in industrial applications. The design of the limiter was made using the ISE software with respect to the technological limitations. The first demonstrator measurements exhibit optimistic results, although few adaptations are necessary to reach the foreseen characteristics. Bi-directional components were measured by associating two devices head to tail. This device could be used in application such as current limitation in case of a short circuit of an electrical system. It could permit an elevation of the current ratings of classical mechanical switch with the serial addition of this device.

Acknowledgment.

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