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Autonomous CMOS Power Management Integrated Circuit for Electrostatic Kinetic Energy Harvesters e-KEH

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Abstract—In this paper we present an autonomous Power Management Integrated Circuit PMIC for an electret-biased electrostatic kinetic energy harvester with a Bennet's doubler conditioning circuit. The circuit is designed in high voltage 0.35 μm standard bulk CMOS technology. It supplies a low voltage load from the energy extracted from a high voltage transducer. The circuit is provided with a “cold start” mechanism and with a “safe mode” (Recovery) feature that permits to the system to stay active (awake) for a longer time after external vibrations stop temporarily. An ultra-low static power hysteresis comparator is designed for a specific control of the capacitive transducer's conditioning circuit. The autonomy of the system is ensured by a voltage regulator that supplies the internal blocks of the circuit with 1.1 V. The proposed design consumes less than 400 nW making it adequate for use with existing state-of-the-art capacitive harvesting MEMS devices.

Keywords—Energy harvesting, power management, Bennet's doubler, electrostatic transduction, MEMS, IoT.

I. INTRODUCTION

The emergence of the Internet of Things prioritized the power management in the connected devices, so to maximize their autonomy. Many efforts have been made for optimizing the consumed power: introduction of sleep mode, near sensor computing approaches, etc. The autonomy is even more important when access to these devices is difficult or even impossible (space instruments, *in-vivo* implanted biomedical devices...), and when the battery cannot be replaced easily. Device's autonomy can be ensured by harvesting energy from available ambient sources e.g. light, vibrations, RF waves.

This work proposes an electrical interface implemented in 350 nm CMOS technology for devices converting vibrational energy into electricity to supply small IoT nodes. The architecture is optimized for electrostatic (capacitive) transducers having a high voltage output interface.

Electrostatic transducers are particularly suitable for miniature electrostatic kinetic energy harvesters (e-KEH) which use MEMS technology. The full architecture of the implemented harvesting system is depicted in Figure 1(a).

Electrostatic transducer is a variable capacitor whose capacitance varies with displacement of its movable electrode. An electret layer is deposited on one of the transducer's electrodes, so providing an initial electrical biasing of transducer and allowing a start-up of the energy harvesting without needing an external energy source. Such transducers are able to provide between 1 and 100 μW of power, depending on the particular transducer implementation and on the parameters of external vibrations.

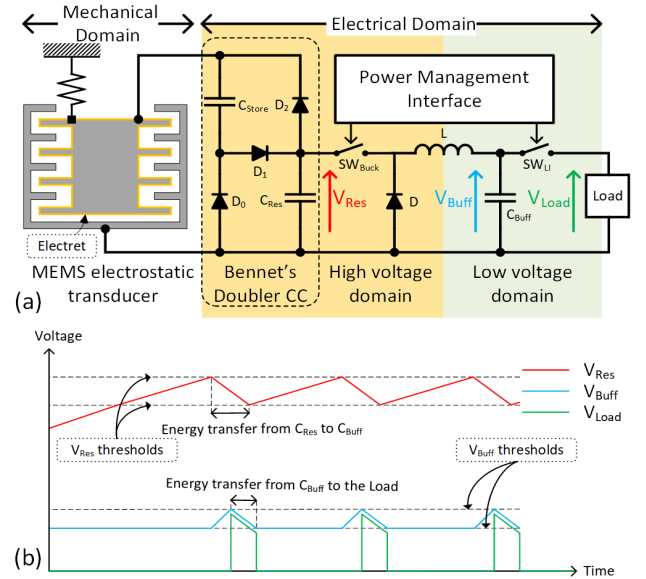


Figure 1 (a) Full e-KEH architecture with the proposed power management interface (b) working principle

A conditioning circuit, based on the Bennet's electricity doubler is used to convert the capacitance variation into electric energy which is available on a reservoir capacitor (C_{Res} in Figure 1(a)). An additional interface is required in order (i) to transfer the converted energy into a low voltage reservoir capacitor C_{Buff} (called buffer in this work), (ii) to manage the transfer rate so to ensure the voltage V_{Res} to be within the optimal interval. More on the Bennet's doubler operation in the energy harvesting mode can be found in [1]

This work reports on a practical implementation of such an interface called Power Management Integrated Circuit (PMIC). The main technical challenge is that the circuit must operate with an extremely low available power (few microwatts) while managing high voltages. The design was validated by a standard analog IC verification flow and the layout was sent to the foundry for the fabrication.

The proposed design is based on a two-step energy transfer process as shown in Figure 1(b). In the first step, energy is transferred from the conditioning circuit's C_{Res} to the buffer capacitor C_{Buff} through a DC-DC buck converter with an integrated high voltage PMOS switch SW_{Buck} . In the second, the energy is transferred from C_{Buff} to the load via a PMOS switch SW_{LI} . The first (second) transfer step begins when a pre-defined upper threshold is detected on V_{Res} (V_{Buff}) and it stops when a lower threshold is detected. Notice that the two steps are not synchronized and the control circuits are completely independent from each other. The thresholds of

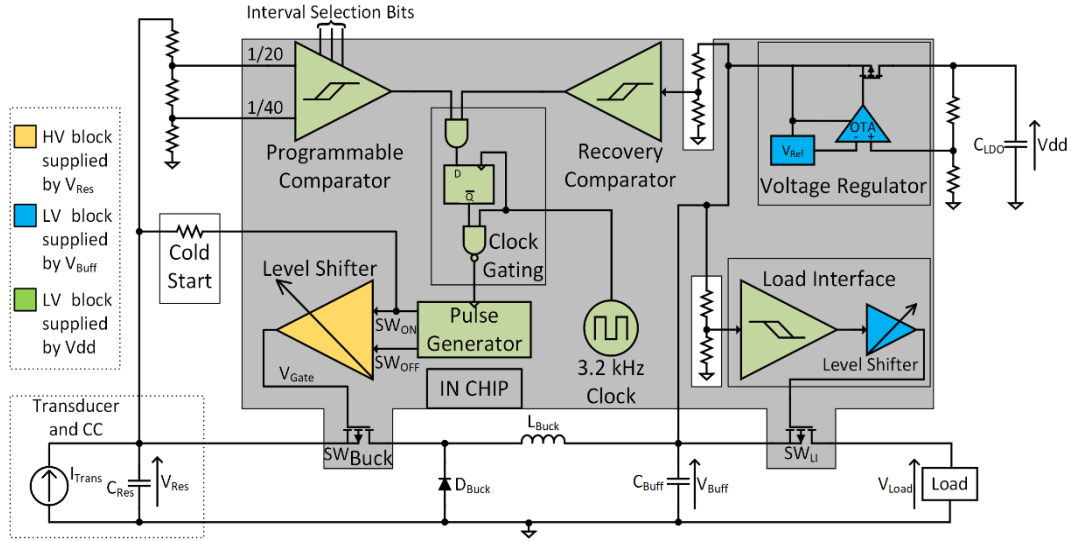


Figure 2 Full e-KEH system showing the detailed architecture of the designed PMIC

V_{Res} are supposed to be set-up by an external circuit achieving the MPPT (Maximum Power Point Tracking) function, which is not addressed in this work.

The proposed PMIC is designed to be fully autonomous and to be supplied by a part of the energy generated by the transducer with a reduced voltage of 1.1 V (compared to the nominal 3.3 V of the technology), so to ensure an ultra-low power consumption. An original technique is proposed for the e-KEH's cold start and for "Recovery mode" used to extend the circuit activity time when the external vibrations are temporarily absent or very weak. The proposed design borrows some blocks from the first implementation of the e-KEH PMIC published by our team [2]. In the following sections, we describe the main blocks of the PMIC and we present the three operating modes of the e-KEH. Then we present the obtained simulation results.

II. SYSTEM DESCRIPTION

The detailed architecture of the designed PMIC within the full e-KEH system is depicted in Figure 2, where the transducer and its conditioning circuit are represented with a DC-current source I_{Trans} in parallel with a capacitor $C_{Res}=1\mu F$. This is a generic model of any capacitive kinetic energy harvester, which always behaves as a charge pump. The main blocks can be split into 3 categories according to their function:

- Voltage regulator: ensures the autonomy of the e-KEH by supplying the internal blocks with 1.1 V;
- Load Interface: manages the transfer of energy from the buffer to the load;
- Rest of the blocks: manage the transfer of energy from C_{Res} to C_{Buff} .

A. Working modes

According to the external vibrations that the e-KEH undergoes, and to the stored energy in its capacitors, there are 3 possible operating modes:

Harvesting mode. In this mode, the e-KEH has enough stored energy in the capacitors and the external vibrations have a sufficient level for the supply power generation. The energy is transferred from C_{Res} to C_{Buff} via the buck converter according

to the multiple energy shot technique. When the programmable comparator detects the selected threshold V_H on V_{Res} , it activates the buck converter by allowing the clock signal to pass through the clock gating circuit to the pulse generator. This later, controls the level shifter's output thus turning ON and OFF the switch SW_{Buck} . Once the lower threshold V_L is detected on V_{Res} , the buck converter is deactivated so that energy re-accumulates in C_{Res} .

Simultaneously with the buck converter operation, the Load Interface block manages the transfer of energy from the buffer to the load. It is based on the same hysteresis behavior as the buck control circuit. However, in this case, the energy is transferred to the load in one shot through the switch SW_{LI} . The chosen thresholds are $V_{Buff-H} = 2.25$ V and $V_{Buff-L} = 2$ V.

Cold start. A cold start scenario is a start-up of the e-KEH while the initial stored energy in all of its capacitors is zero. As the used transducer is an eletret-biased combined with a Bennet's Doubler conditioning circuit, as soon as external vibrations start, the harvesting process begins and the voltage V_{Res} increases [3]. However, without a cold start circuit, the energy would only accumulate in C_{Res} and the control blocks would not be supplied. This would lead to the saturation of the V_{Res} voltage. The proposed cold start solution consists of a pull-up resistor that forces a positive voltage on the level shifter's SW_{ON} input. The e-KEH manages to transfer energy from C_{Res} to C_{Buff} thereby, supplying the voltage regulator. V_{Res} and V_{Buff} increase until V_{dd} reaches its nominal value and the e-KEH enters to the Harvesting mode.

Recovery. This mode corresponds to the situation where the e-KEH has enough energy stored in the capacitors. However, there are no vibrations. As the internal blocks of the PMIC consume energy, V_{Buff} decreases. If the vibrations stop for a long time V_{Buff} may reach low values that are insufficient to ensure the correct functioning of the LDO, thus the control blocks. To overcome this situation, we propose to add a hysteresis comparator whose lower threshold V_{Rec-L} corresponds to the minimum supply voltage required by the LDO. The Recovery Comparator activates the buck converter when the lower threshold $V_{Rec-L} = 1.8$ V is detected and it deactivates it when the upper threshold $V_{Rec-H} = 2$ V is detected. The behavior of the buck converter is the same as explained for the Harvesting mode. The Recovery mode can be seen as a "safe mode", where, the priority is to keep the

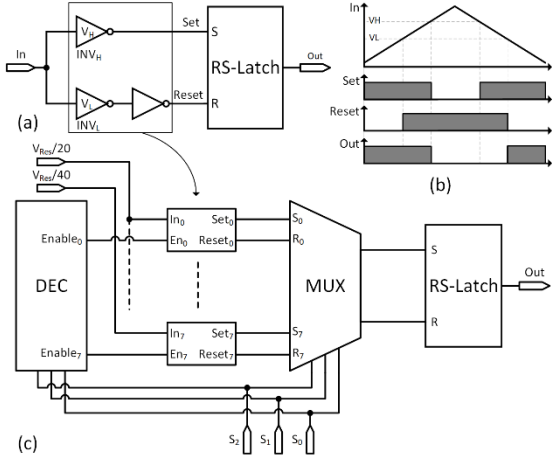


Figure 4 (a) RS-Trigger based hysteresis comparator (b) chronograms (c) programmable hysteresis comparator

system active (awake) as long as possible until the vibrations resume.

B. Circuit description

This section describes the operation of some key blocks of the PMIC.

Clock generator. This circuit is based on a relaxation oscillator architecture and is inspired by the work reported in [4]. This clock has an ultra-low power consumption of 25 nW and a frequency of 3.2 kHz. Implementation details of this circuit, and particularly its adaptation to 1.1 V supply voltage are described in [2].

Level shifter. It is a dynamic level shifter allowing the gate control of the high-side PMOS switch SW_{Buck} . Its state is controlled by short pulses on SW_{ON} and SW_{OFF} and it has a zero static power dissipation. When it receives a pulse on SW_{ON} its output switches from V_{Res} to $(V_{Res} - 2 V)$. And when it receives a pulse on SW_{OFF} , the output switches back to V_{Res} . More detail about the level shifter design may be found in [2], [4], [5].

RS-Trigger based hysteresis comparator. This circuit is used in both Recovery Comparator and in Load Interface circuits. It has been previously designed by [2] based on [6], [7]. It is composed of basic logic elements i.e. three inverters and an RS-Latch (see Figure 4(a)). The comparator's thresholds correspond to the inverters INV_H and INV_L thresholds V_H and V_L , respectively. These thresholds can be fixed by tuning the size ratio W/L of each inverter's transistors. The behavior of the hysteresis comparator is summarized in Figure 4(b) chronogram.

RS-Trigger programmable comparator. To make a programmable hysteresis comparator based on the RS-trigger hysteresis comparator described above, we propose the architecture presented in Figure 4(c). The principle is to duplicate the pair of inverters INV_H and INV_L as many times as the number of intervals. Each pair of inverters is then sized according to the required interval. To allow the programmability of the circuit, we use a decoder and a multiplexer. The decoder turns off all unused inverters (in order to reduce power consumption), while the multiplexer selects the outputs of the active pair of inverters and connects its outputs to the RS-Latch's inputs.

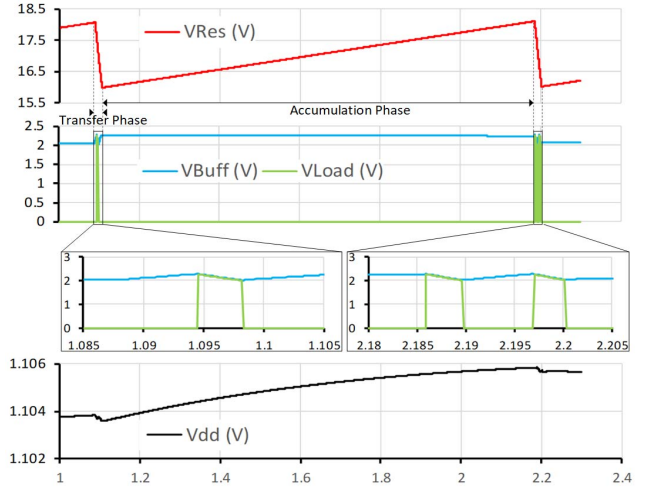


Figure 3 Harvesting mode simulation results

The designed programmable comparator has 3 bits input selection vector, allowing to choose one out of 8 possible intervals of equal length $V_H - V_L = 2 V$. The programmable comparator has two analog inputs, these inputs correspond to the divided (down-scaled) voltages of the output of the conditioning circuit: $V_{Res}/20$ and $V_{Res}/40$. This combination of inputs allows the comparator to cover a wide range of input voltages [8 V – 24 V].

Voltage regulator LDO. The designed voltage regulator is a Low Drop Out (LDO) voltage regulator that is supplied by V_{Buff} and generates a regulated output voltage of 1.1 V. An operational transconductance amplifier OTA is used as an error amplifier in the LDO. The designed reference voltage generator is based on a constant g_m CMOS quad with an integrated floating resistance of 22.5M Ω . The generated reference voltage is $V_{Ref} = 672 mV$. The average quiescent power of the LDO is 42 nW. The minimum supply voltage required for the designed voltage regulator is equal to 1.8 V. Thus, we decided to fix this value as the lower threshold of the Recovery Comparator V_{Rec-L} (see sub-sec.A above).

III. SIMULATION RESULTS

Several simulations, including MC simulations of individual blocks, have been done to study performance and power consumption of the PMIC. In the following, we present the obtained simulation results of the full e-KEH architecture in all operating modes.

A. Harvesting

In this simulation, the main performance characteristic to be measured is the efficiency η_{e-KEH} of the energy transfer from the transducer to the load. The transducer's equivalent current source is fixed to $I_{Trans} = 2 \mu A$, and the initial conditions are: $V_{Res0} = 16 V$, $V_{Buff0} = 2 V$ and $V_{dd0} = 1.1 V$. The chosen interval for V_{Res} is [16 V – 18 V]. The average power generated by the transducer model is 34 μW : this is within the power range generated by the state-of-the art capacitive kinetic harvesters, which is typically between 10 μW and 100 μW [8]. Figure 3 shows the obtained simulation results from 0 to 2.3 s. If we consider the two cycles of accumulation and transfer, we obtain the following results:

- The energy consumed by the load is $W_{Load} = 48.7 \mu J$;
- The PMIC consumed $W_{PMIC} = 7.3 \mu J$;

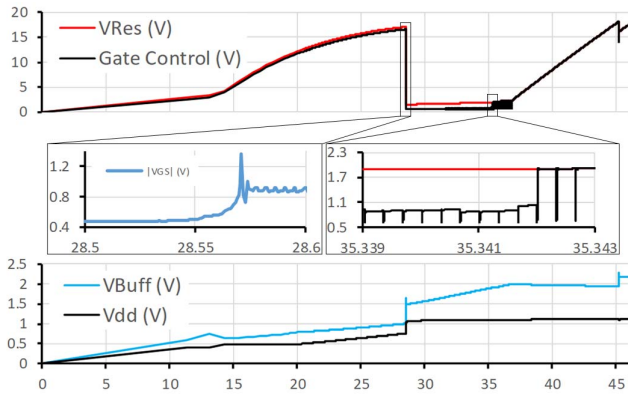


Figure 6 Cold start simulation results

- The energy dissipated by the discrete components is $W_{\text{other}} = 10.8 \mu\text{J}$ of which $W_{\text{D-Buck}} = 9.8 \mu\text{J}$ is consumed by the flyback diode.

The resulting end to end efficiency is then $\eta_{\text{e-KEH}} = 72.9 \%$.

B. Cold start

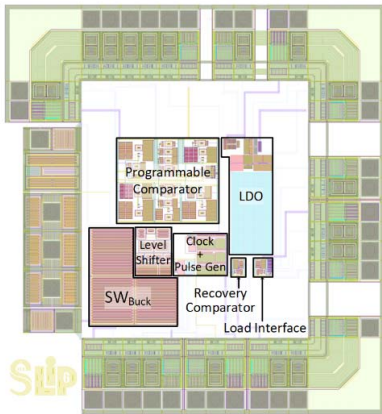


Figure 5 Designed PMIC layout

Initially, V_{Res} , V_{Buff} and V_{dd} are null. $I_{\text{Trans}} = 2 \mu\text{A}$ during the simulation. The obtained results of a transient analysis are presented in Figure 6.

As C_{Res} charges from I_{Trans} , a positive voltage is forced by the pull-up resistor at SW_{ON} . The Level shifter's output is then $V_{\text{Gate}} < V_{\text{Res}}$. C_{Res} and C_{Buff} charge in the same time and V_{dd} increases. It can be seen at $t = 13 \text{ s}$, that V_{Buff} increases slowly compared to V_{Res} . This is due to the effect of the pulse generator that tries to force SW_{ON} to 0 V.

At $t = 28.6 \text{ s}$, the pull-up resistor manages to force a positive voltage on SW_{ON} resulting in $V_{\text{Gate}} < V_{\text{Th}} = 0.63 \text{ V}$ (see zoom from 28.5 s to 28.6 s in Figure 6). Energy is then instantly transferred to C_{Buff} and V_{dd} approaches its nominal value. Here, the buck converter is activated by the Recovery Comparator. In the beginning, the level shifter doesn't manage to operate correctly due to V_{Res} low values. until this later reaches a sufficient level (see zoom from 35.339 s to 35.343 s). At $t = 36.8 \text{ s}$, $V_{\text{Buff}} = V_{\text{Rec-H}} = 2 \text{ V}$ and the buck converter is deactivated. The e-KEH enters to Harvesting mode.

C. Recovery

Figure 7 shows the obtained simulation results of the e-KEH operating in Recovery mode. The initial conditions are: $V_{\text{Res}0} = 8 \text{ V}$, $V_{\text{Buff}0} = 2.2 \text{ V}$, $V_{\text{dd}0} = 1.1 \text{ V}$. In the beginning $I_{\text{Trans}} = 0 \text{ A}$. Due to internal blocks consumption V_{Buff} decreases,

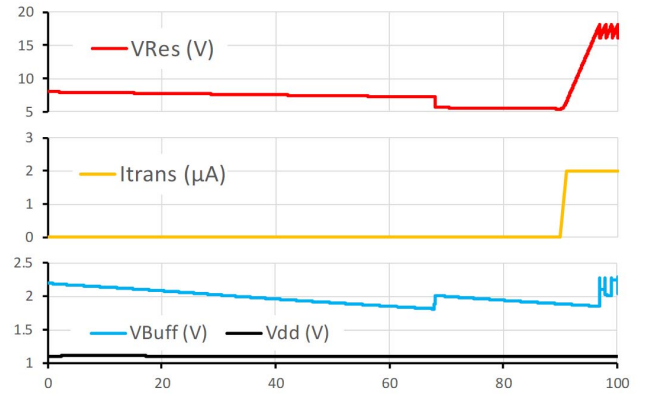


Figure 7 Recovery mode simulation results

until it reaches the Recovery Comparator's threshold $V_{\text{Rec-L}} = 1.8 \text{ V}$. The buck converter is then activated and C_{Buff} recharges until $V_{\text{Buff}} = V_{\text{Rec-H}} = 2 \text{ V}$. Note that V_{Res} decreases due to the voltage divider and Cold Start's pull-up resistor power dissipation. At $t = 90 \text{ s}$ the transducer's current $I_{\text{Trans}} = 2 \mu\text{A}$, thus V_{Res} increases and the e-KEH enters to Harvesting mode.

D. Implemented chip

In Figure 5, the full layout of the designed PMIC is depicted. The core occupies an area of 0.7 mm^2 from a total area of 4.1 mm^2 (pad limited chip). The circuit is primarily designed for input voltages from 8 to 24 V. Though, the technology's maximum rating voltage 50V can be reached by adjusting the external components values.

IV. CONCLUSION

A designed power management circuit is proposed for electrostatic kinetic energy harvesters in a high voltage CMOS technology. It has an ultra-low quiescent power consumption thus, being suitable for available capacitive transducers. The proposed e-KEH architecture is fully autonomous, where the voltage regulator ensures that the internal blocks are supplied from harvested energy. The cold start and the Recovery circuits allow the harvesting process to begin and to be maintained despite the randomness of the external vibrations.

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