CMOS voltage and current feedback opamps: a comparison between two similar topologies

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Hervé Barthélemy [(1)], Valentin Gies [(1)], Stéphane Meillère [(2)], Rémy Vauché [(2)], Edith Kussener [(3)], Manon Fourniol [(1)]

(1) Université de Toulon, Aix Marseille Univ, CNRS, IM2NP, Toulon, France

(2) Aix Marseille Univ, Univ Toulon, CNRS, IM2NP, Marseille, France

(3) ISEN Yncréa - CNRS, IM2NP, Maison des technologies, 83000 Toulon, France

Corresponding Author:
Prof. H. Barthélemy
herve.barthelemy@univ-tln.fr

Commenté [r1]: on est censé avoir la même affiliation quelque soit l'université :)

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Abstract— The *voltage feedback operational amplifier* (VFOA) and the *current feedback operational amplifier* (CFOA) are the main opamps with voltage output currently used in electronic. The VFOA is a combination of an *operational transconductance amplifier* (OTA) as input stage and an output voltage buffer (VB). In this paper, the CFOA is described as a combination of an *operational transconductance conveyor* (OTC) as input stage and an output voltage buffer. Two similar CMOS architectures are then defined, analyzed and simulated in order to provide some elements of comparison. Results, for a typical CMOS 0.35µm technology, show the role of compensation capacitances to boost the frequency performances of the non-inverting amplifier.

Keywords: voltage feedback amplifier, current feedback amplifier, Operational transconductance amplifier, operational transconductance conveyor.

1. Introduction

Because they offer the possibility to realize a quasi-linear amplification, operational feedback amplifiers [1] play an essential role in a huge number of electronic applications. Most of these applications concern analog signal processing based on amplifiers, filters and oscillators. An Operational Transconductance Amplifier (OTA) as input stage in series with a Voltage Buffer (VB) as output stage permit to describe the Voltage Feedback Operational Amplifier (VFOA); note that connection node between the OTA output and the VB input is a high impedance node (called here Z) which allows the opamp high open-loop gain to be created. In a similar way, the Operational Transconductance Conveyor (OTC) as input stage in series with a VB as output stage permits to describe the CFOA; the high impedance node Z is now the node between the OTC output and VB input. The OTC description **[2]** is also useful because it allows the description of each type of Current Feedback Operational Amplifier (CFOA) input stages [2].

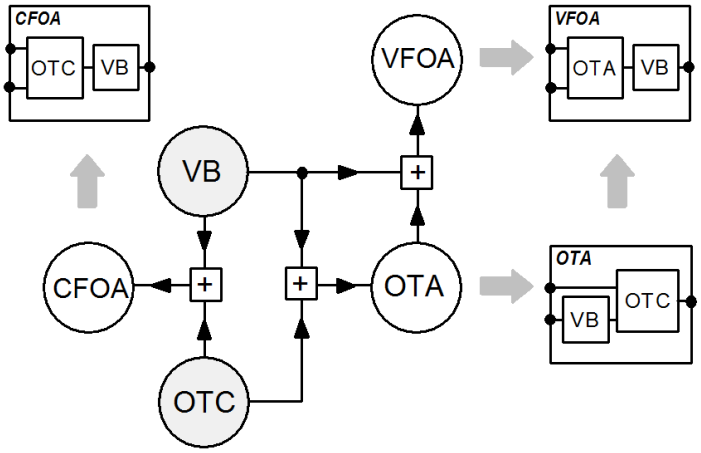


Figure 1. Design synthesis of the OTA, VFOA and CFOA using OTC-VB combinations.

The diagram in Fig.1 shows how the OTA, the VFOA and the CFOA are constructed using an OTC [2]. OTA, OTC, VFOA and CFOA are the four usual opamp topologies having current or voltage outputs: i) *current output: OTC and OTA* ii) *voltage output: CFOA and VFOA.*

Several names and acronyms are used to describe opamp topologies. For example, the VFOA is also called *voltage feedback amplifier* (VFA) or *voltage opamp*. The CFOA is also called *current feedback amplifier* (CFA) or *operational transimpedance amplifier;* note that *operational transimpedance amplifier* leads to the same acronym than one used for the *operational transconductance amplifier* (OTA), consequently the acronym OTA is not used to describe the CFOA. The ideal OTA is also equivalent to a *voltage controlled current source* **[10]** (VCCS). Fig.1 summarizes the topologies discussed above. The square boxes in Fig.1 show examples of implementations.

It is not always very easy to know which type of opamp topology is the most appropriated. **The main objective of this paper consists in the using and the simulation of two quasi-similar designs, in order to study the performances of these amplifiers for similar conditions, i.e. voltage supply, power, area.** In this paper, we also provide some comparisons between a CMOS VFOA and a CMOS CFOA considering theoretical and simulated results. Performances analysis was made for similar power consumption and level of design implementation. The CFOA and the VFOA, discussed in this paper, are also implemented with the same CMOS output *Voltage Buffer* (VB) topology. Moreover, the architecture of the high impedance node is identical for the two opamps.

These implementations are discussed in section 2. In section 2.1, an overview of the ideal operational transconductance conveyor (OTC) **[2]** and of the ideal operational transconductance amplifier (OTA) **[3,4]** are given. In section 2.2, the OTA and the OTC are used to describe the *voltage feedback operational amplifier* (VFOA) and the *current feedback operational amplifier* (CFOA) respectively **[5,6]**. In section 3, the two CMOS architectures with similar sizes are analyzed theoretically and simulated from LTSPICE **[10,11]** using the typical CMOS 0.35µm BSIM3V3 transistor models from AMS **[12]**. In most applications, opamps operate at frequencies below 1GHz and a 0.35µm provides also a high performance/power ratio to operate at these frequencies **[13]**. However, for higher frequency, it could be more advantageous to use 0.18µm or below, especially if the analog circuit should be in the same chip than a high density digital part **[13]**. For these conditions, due to the channel modulation effect, it is often necessary to size the transistors lengths higher than its minimal value because this permits to provide high

transistor output resistances, even if a cascode technique is used. Finally, a conclusion is given in section 4.

2. Opamp topologies

2.1. OTA and OTC

Using the VB description, Fig.2 and Fig.3 show electrical description and symbol of the OTC and the OTA respectively. This OTC [2] allows to describe all type II current conveyors (CCII) or current controlled conveyors (CCCII) [7,8], or the diamond transistor [5,9]. The OTA (Fig.3) allows all the differential transconductance amplifiers topologies having high input impedances to be described.

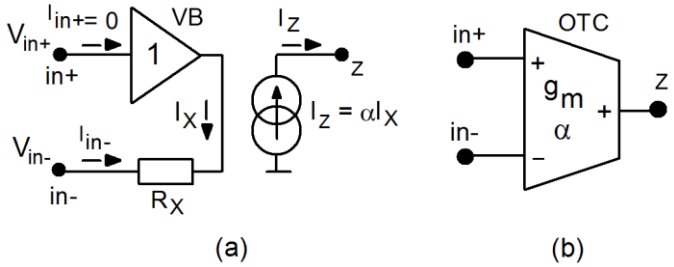


Figure 2. Single ended *operational transconductance conveyor* (OTC) **[1].**

It is important to notice that the ideal OTC (Fig.2) must not be called OTA [5,9] because its behavior differs from an ideal OTA (Fig.3). Effectively, the ideal OTA provides an ideal infinite impedance at their two input differentials nodes *in+* and *in-*, that is not the case of the node *in-* of the ideal OTC, for which a non-zero current I_X (or $I_{in-} = -I_X$) is flowing through the node *in-*. This is also the reason that the current gain α must be included in the OTC symbol. Note that the OTC simulates a traditional CCII when $R_X=0$ and $|\alpha|=1$ and it simulates a CCCII (or a diamond transistor [5,9]) for $R_X>0$ and $|\alpha|=1$. For both the ideal OTA and OTC, the amplifier and conveyor transconductance g_m is defined by:

$$g_m = \alpha / R_X = \alpha g_{mX} \quad (1)$$

with

$$I_Z = g_m(V_{in+} - V_{in-}) \tag{2a}$$

where $(V_{in+} - V_{in-})$ is the differential input voltage and I_Z the output current. In non-ideal case, if necessary, the common mode gain can be considered. In this case, the Iz current can be expressed as follows:

$$I_Z = g_{md}(V_{in+} - V_{in-}) + \frac{g_{mc}}{2}(V_{in+} - V_{in-}) \tag{2b}$$

where g_{md} (= g_m) is the differential transconductance gain and g_{mc} the common mode transconductance gain.

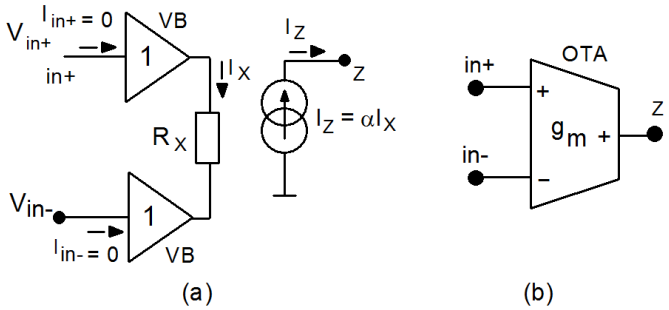


Figure 3. Single ended *operational transconductance amplifier* (OTA).

From Fig.2 and Fig.3, it is possible to see that the OTA is a construction using an OTC and an additional VB. This construction is showed in Fig.4.

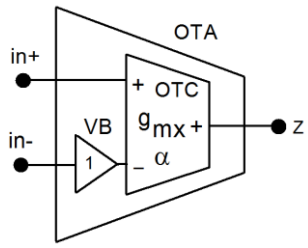


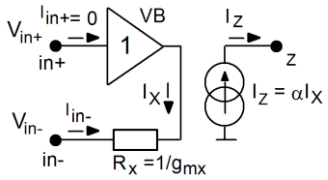
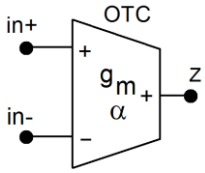
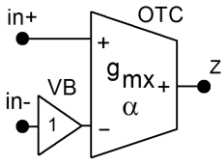
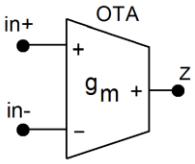
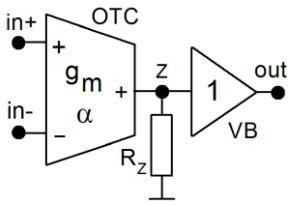
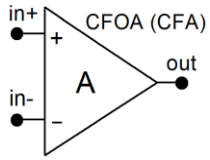
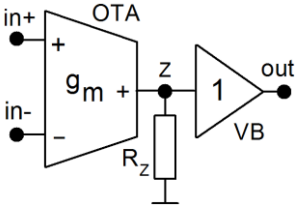
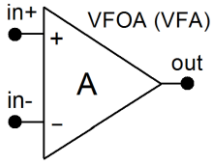
Figure 4. OTC and VB based single ended OTA.

In the next sub-section, the OTC and OTA will be used to introduce the CFOA and the VFOA.

2.2. Opamps classification

The 4 resulting opamp topologies discussed above are summarized in Table 1. Note that in case of two stages OTA or OTC, the transconductances are generally written G_M instead of g_m (and/or G_{MX} instead of g_{mx}).

Table 1. Electrical descriptions and symbols of the 4 main opamp topologies OTC, OTA, CFOA, VFOA.

	Electrical descriptions	Symbols
OTC		
OTA		
CFOA		
VFOA		

From Table 1, the DC open loop gain for the CFOA and the VFOA is:

$$A = g_m R_Z \tag{3}$$

When V_{in+}=0, the input impedance at node *in-* is infinite for the VFOA configuration and is equal to R_X for the CFOA configuration, with $R_X = g_{mX}^{-1}$.

3. CMOS CFOA and VFOA topologies

3.1 CMOS Topologies and analysis

Fig.5 and Fig.6 represent the equivalent CMOS topologies of the similar CFOA and VFOA used to operate the comparison.

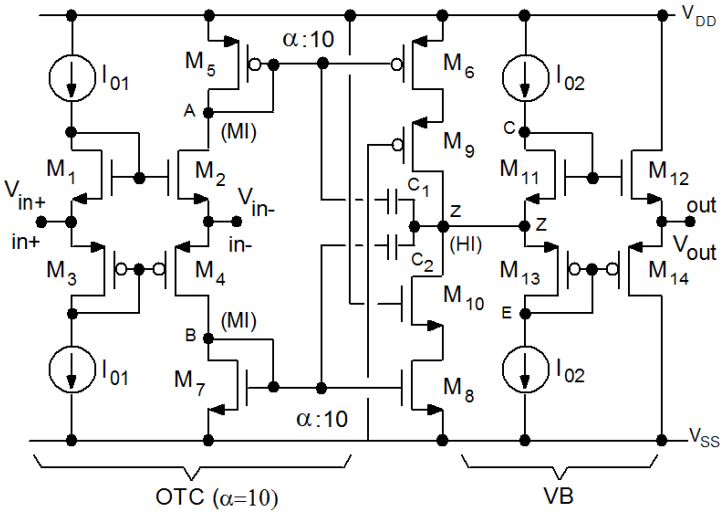


Figure 5. One stage current feedback opamp (CFOA or CFA).

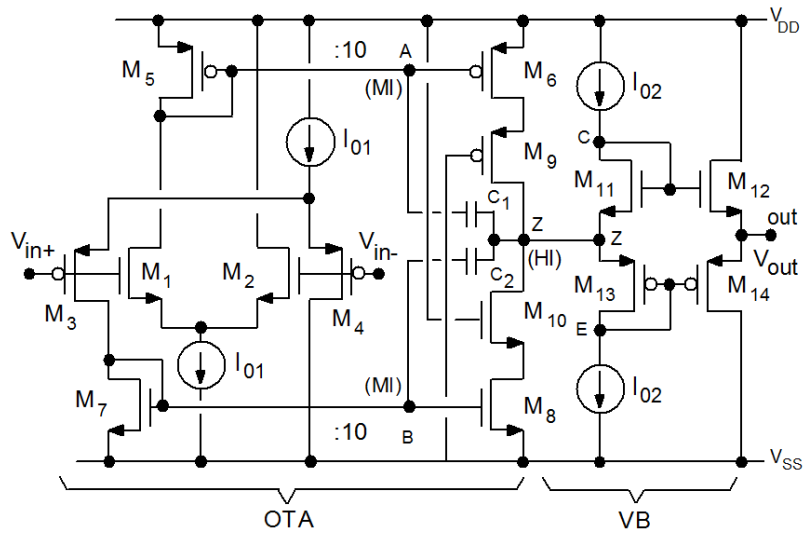


Figure 6. One stages voltage feedback opamp (VFOA or VFA).

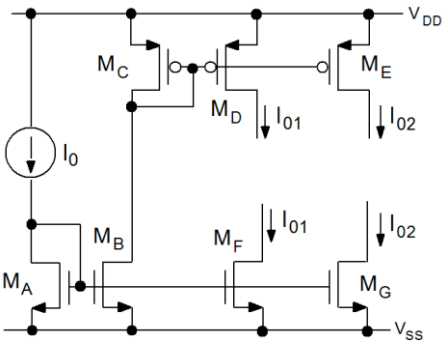


Figure 7. Biasing circuit of the CFOA in Fig. 5 and the VFOA in Fig. 6.

Fig.7 shows the biasing circuit of the CFOA and the VFOA. The both topologies in Fig.5 and Fig.6 have been chosen, i.e. designed, due to their similarities. The VFOA is designed using a traditional complementary *nmos* (M_1-M_2) and *pmos* (M_3-M_4) differential input pairs of two transistors. The OTA input stage (Fig.6) is also called rail-to-rail OTA **[14]**. However, for the CFOA and the VFOA, the maximum output voltage swing is limited by the two diode connected transistors M_{11} and M_{13}. In Fig.5 and in Fig.6, the cascode transistors M_9 and M_{10} allow a high impedance to be obtained at node Z (HI). Considering *mos* channel length Li of transistor Mi, L_1 to L_4 are equal and L_5 to L_{14} are equal too (see Table 2). The bias currents I_{01} and the channel-width ratio W_P/W_N of transistors M_1,M_2,M_3 and M_4 have been fixed in order to obtained the same gate-

source transconductance value, i.e. $g_{m1}=g_{m2}=g_{m3}=g_{m4}$; we also assume that all *nmos* and *pmos* transistors operate in saturate mode **[11]**. Neglecting the channel length modulation effect, the equivalent OTC and OTA (Fig.5, Fig.6) transconductance g_{mx} (see Table 1) can be approximated, i.e. SPICE level 1 **[11]**, by :

$$g_m = 2\alpha\sqrt{2\beta_1 I_{01}} \qquad \text{(OTC)} \qquad (4a)$$

$$g_m = \alpha\sqrt{\beta_1 I_{01}} \qquad \text{(OTA)} \qquad (4b)$$

where β_1 is the current gain of the transistor M_1 in saturate mode **[11]**, i.e. $\beta = \mu C_{OX} W/L$ with μ the mobility and C_{OX} the oxide capacitance per meter square **[11]**, W the *nmos* channel width, L the *nmos* channel length.

A two stage VFOA is currently designed from two high impedance nodes. Here the two topologies (Fig.5 and Fig.6) are based on a medium impedance (nodes A and B) and a high impedance (node Z). Consequently, they belong to the class of one stage opamps. As usual, C_1 and C_2 (with $C_1=C_2$) are the Miller capacitances used for increasing the phase margin. The *high impedance* (HI) at node Z (R_Z) is given by:

$$R_Z = R_{Z0} \,//\, R_{VB} \qquad (5)$$

where R_{Z0} is the VFOA or CFOA output resistance and R_{VB} the voltage buffer input impedance at Z node. Assuming that the channel-width ratio W_6/W_8 and W_9/W_{10} are set equal to μ_n/μ_p, where μ_n and μ_p are the mobility for *nmos* and *pmos* respectively, we have:

$$R_{Z0} = \frac{1}{\sqrt{2}} \frac{1}{\lambda_n^2 + \lambda_p^2} \frac{1}{\sqrt{\alpha^3}} \frac{\sqrt{\beta_{10}}}{\sqrt{I_{01}^3}} \qquad \text{(CFOA)} \qquad (6a)$$

$$R_{Z0} = \frac{2}{\lambda_n^2 + \lambda_p^2} \frac{1}{\sqrt{\alpha^3}} \frac{\sqrt{\beta_{10}}}{\sqrt{I_{01}^3}} \qquad \text{(VFOA)} \qquad (6b)$$

and the output voltage buffer impedance is, for the CFOA and the VFOA, about:

$$R_{VB} = \frac{1}{\lambda_n + \lambda_p} \frac{1}{I_{02}} \qquad \text{(CFOA, VFOA)} \qquad (7)$$

where β_{10} is the current gain of the transistor M_{10} and λ_n, λ_p the channel-length modulation parameters of the *nmos* and *pmos* transistors respectively. Note that using the same λ_n and λ_p for all transistors is an approximation. From equations (6a) and (6b), and for the same bias current, the VFOA has a higher impedance, while the transconductance is lower; see equations (4a,b). At the same DC bias current, considering infinite VB input impedance, the open loop voltage gain $A=g_m.R_Z$ should in the same order for both the CFOA and the VFOA, because, in this case $R_{Z(VFOA)}=2\sqrt{2}\,R_{Z(CFOA)}$ and $g_{m(CFOA)}=2\sqrt{2}\,g_{m(VFOA)}$. However, because R_{VB} is finite, the CFOA open loop gain voltage should be higher than the VFOA one. In the next section, to operate at the same power consumption (2.4mW), the ratio between the current $I_{01(VFOA)}$ and $I_{01(CFOA)}$ is 3/2 (*found by simulation*); from equation (4a,b), we have found $g_{m(CFOA)} \approx 2.31.g_{m(VFOA)}$; in the same way the CFOA open loop gain voltage should be higher than the VFOA one.

3.2 Simulations and Discussions

In this sub-section, it is proposed to provide a comparison between the CFOA and the VFOA presented in Fig.5, Fig.6, and Fig.7 with the help of simulation results. Table 2 summarizes the sizes of all transistors for the CFOA and the VFOA. Table 2 also includes our estimation (*post-layout*) of the drain and source area and perimeters of each transistor in order to take into account, during simulations, the reverse junction capacitance effects. All Simulations have been performed using LTSPICE **[10,11]** and the typical CMOS 0.35µm BSIM3V3 transistor models from AMS **[12]** for V_{DD}=3.3V and V_{SS}=0V. The DC common mode voltage is then equal to $V_{DD}/2$=1.65V. The DC bias current I_{01} is set to 50µA for the CFOA and 75µA for the VFOA while $I_{02}=I_{01}/2$. All simulations were performed with infinite loading impedance (*node out*) and the compensation capacitances C_1 and C_2 have been set from simulations. In this paper, the value of $C_1=C_2=C_C$ have been increased until there is no resonance.

Table 2. CFOA AND VFOA TRANSISTORS SIZES AND EQUIVALENT DRAIN AND SOURCE AREAS (AD, AS) AND THEIR PERIMETERS (PD, PS) [10].

	W (μm)	L (μm)	AD=AS (m^2)	PD=PS (m)
M_1,M_2	50	0.5	44E-12	52E-6
M_3,M_4	150	0.5	130E-12	152E-6
M_5,M_7,M_{10}	10	1	9E-12	12E-6
M_6,M_8	100	1	88E-12	102E-6
M_9,,M_{11}, M_{12}	30	1	27E-12	32E-6
M_{13}, M_{14}	90	1	81E-12	92E-6
M_A, M_B, M_C, M_D, M_F	10	2	9E-12	13E-6
M_E,M_G	5	2	5E-12	7E-6

3.2.1. DC and low-frequency simulations

Table 3 summarizes the main simulated performances of the two opamps at low frequencies and Fig.8 shows the simulated DC output current characteristic of the OTC and of the OTA; the slopes around $V_{DD}/2$ are equal to g_{mx} (see equation (1)). For $I_{01(OTC)}$=50μA and $I_{01(OTA)}$=75μA, Table 3 confirms an expected higher transconductance g_{mx} for the OTC (see equation 4a,b). In Table 3, from equations and simulations, we have reported the calculation of the OTC and OTA transconductance g_m, i.e. $g_m = \alpha g_{mX}$ as well as the theoretical estimation of R_Z from equation (3) by:

$$R_Z = \frac{AR_X}{\alpha} = \frac{A}{\alpha g_{mx}} \tag{8}$$

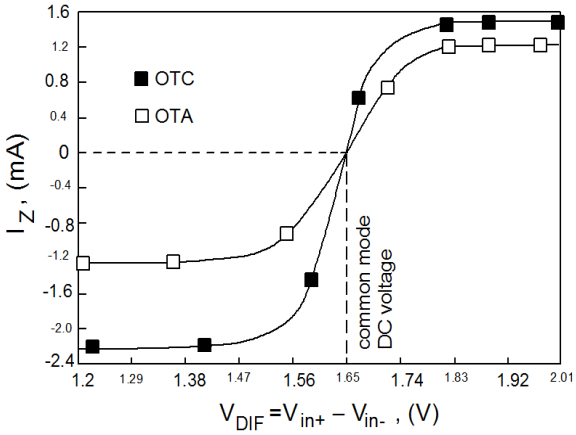


Figure 8. Simulated DC transconductance characteristic versus the input differential voltage around the DC common mode voltage of 1.65V.

Table. 3 MAIN SIMULATIONS RESULTS AT LOW FREQUENCIES

	CFOA	VFOA	
DC bias Current I_{01}	50	75	[µA]
Total power consumption	2.4	2.4	[mW]
Max output voltage swing	[0.6-2.75]	[0.6-2.74]	[V]
Total current consumption (I_{DD})	725	725	[µA]
R_X	535	1416	[Ω]
g_{mX}	1.87	0.71	[$m\Omega^{-1}$]
α	10.1	10	[I/I]
g_m	18.9	7.1	[$m\Omega^{-1}$]
g_{mc}	275	25	[$\mu\Omega^{-1}$]
CMRR	37	49	dBc
R_{Z0}	54.6	66 (93@I_{01}=50µA)	[kΩ]
R_{VB}	228	50 (228@I_{01}=50µA)	[kΩ]
R_Z	44	28.5 (66@I_{01}=50µA)	[kΩ]
A=g_mR_Z	832	202 (468@I_{01}=50µA)	[V/V]

(1) For the OTA R_X is created by the two input differential pairs

Due to the symmetry of the traditional input differential pair of two transistors (M_1-M_2, M_3, M_4 in Fig.6), the VFOA offers a higher *common mode rejection ration* of CMRR=-51dBc while the CMRR is equal to CMRR=-31dBc with the CFOA topology **[15-21]**. Simulated overview of the *open loop gain voltage* (DC characteristic) is shown in Fig. 9.

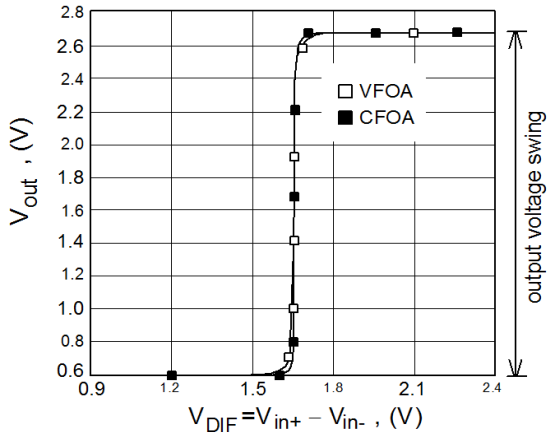


Figure 9. Simulated DC open-loop voltage characteristic versus the input differential voltage and around the DC common mode voltage of 1.65V (V_{DD}/2).

3.2.2. Frequency analysis

In this section, the frequency performances and the DC voltage gain precision of the two configurations (Fig.5 and Fig.6) are evaluated in the case of the non-inverting amplifier. Fig.10a shows the principle of the negative feedback and Fig.10b the corresponding opamp based non-inverting amplifier. In Fig.10b, using a VFOA, the current i_x is zero, because the negative input node *in-* is voltage buffered. Using the CFOA, the current $\boldsymbol{i_x}$ tends to 0 when A tends to infinity, then for an ideal CFOA we also have $\boldsymbol{i_x = 0}$. The open loop gain v_{in-}/v_{dif}, for both the CFOA and the VFOA is simplified to **[22, 23, 24]**:

$$\frac{v_{in-}}{v_{dif}} = A\beta = \frac{A}{G_0} \qquad \text{with} \qquad \beta = \frac{1}{G_0} = \frac{R_G}{R_G + R_F} \tag{9a,b}$$

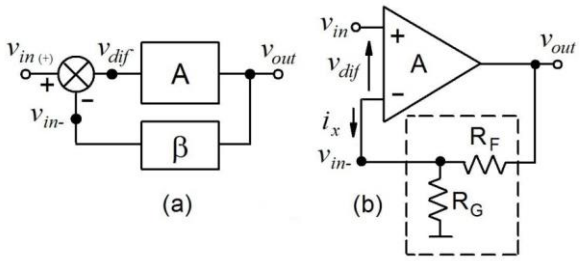


Figure 10. Negative Feedback configuration (*positive gain amplifier*):
-a- principle **-b-** opamp implementation

From (9a) it follows that:

$$\frac{v_{out}}{v_{in}}\underset{A\to\infty}{=}\frac{1}{\beta} = G_0 \tag{10}$$

where G_0 is the ideal gain of the non-inverting amplifier. Equation (9a) shows the impact of the gain in stability **[22, 23, 24]**: if R_F/R_G increases, the open-loop gain of the system decreases. Because the phase remains the same, the gain margin increases and stability is improved. Therefore, a voltage follower configuration (G_0=1) is the worst case for stability **[22, 23, 24]**; if the opamp is stabilized for G_0=1, the opamp will remain stable in all cases. Based on the Miller compensation used in this paper (C_1,C_2), two ways of compensation can be used to set the value of C_C. One way (comp. W1) consists to set definitively C_C in the worst case for stability (G_0=1). A second way (comp. W2), the compensations capacitances (C_C) are set in function of G_0 **[22]**. In this last case (comp. W2), for R_G=1kΩ, Fig.11 draws the values of C_C versus G_0. In Fig.11,

for G_0=1: $C_{C(CFOA)}$=325pF and $C_{C(VFOA)}$=430fF; these values become respectively $C_{C(CFOA)}$=400fF and $C_{C(VFOA)}$=1pF when R_G tends to infinity.

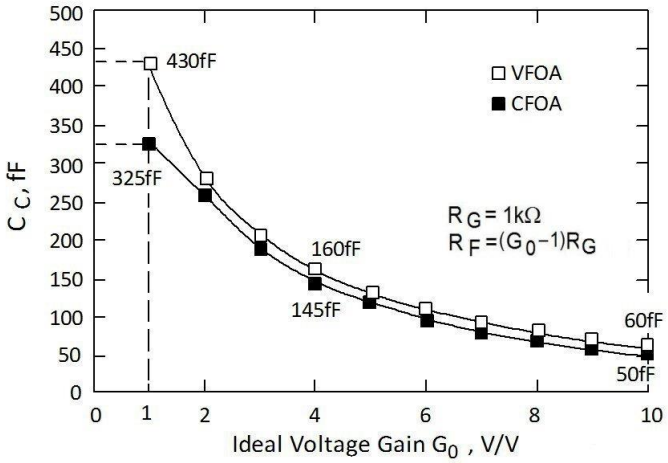


Figure 11. Values of the compensation capacitances C_C versus G_0 (comp. W2).

Voltage buffer configuration (G_0 =1): The unit gain voltage amplification, i.e. R_F/R_G=0, can be obtained in two particular ways: R_G finite (R_F=0) or R_G infinite ($R_F \geq 0$). Each cases lead to different values of the compensation capacitances. Table 4 summarizes the simulation performances considering these two cases: R_G finite and R_G infinite. In Table 4 "FPE" is the frequency when the phase of the voltage gain v_{out}/v_{in} shift up to 1 degree and the best *-3dB* bandwidth obtained by simulation were 129.6MHz for the CFOA and 108MHz for the VFOA.

Table. 4. SIMULATION RESULTS AT UNIT-GAIN AMPLIFICATION

parameters		**CFOA**	**VFOA**	***unit***
DC bias Current I_{01}		50	75	[µA]
Total power consumption		2.4	2.4	[mW]
R_F=0				
C_C=C_1=C_2	$R_G \to \infty$	400	1000	[fF]
	R_G = 1kΩ	325	430	
DC gain error	$R_G \to \infty$	1.55	**0.141**	[%]
	R_G = 1kΩ	1.68	0.57	
F@1° phase error (FPE)	$R_G \to \infty$	3.74	0.9	[MHz]
	R_G = 1kΩ	2.47	1.06	
Bandwidth (BW)	$R_G \to \infty$	**129.6**	88.6	[MHz]
	R_G = 1kΩ	98.8	90.17	
Gain bandwidth product (GBW)	$R_G \to \infty$	127.6	88.5	[MHz]
	R_G = 1kΩ	97.1	89.65	
R_F=10kΩ, $R_G \to \infty$				
C_C=C_1=C_2		110	2850	[fF]
DC gain error		3.82	0.141	[%]
FPE		1.07	0.357	[MHz]
BW		70	32	[MHz]
GBW		67.3	32	[MHz]
Best frequency responses				
C_C=C_1=C_2		400	670	[fF]
R_F		0	0	-
		∞		

In case of the VFOA, if we want to reach a bandwidth of 129.6MHz (obtained with the CFOA), the current consumption must be increased of about 90% and the DC bias current must be set to 150µA instead of 75µA initially (in this case $C_{C(VFOA)}$=0.9pF). Table 3 shows that the CFOA offers the best frequency performance and the VFOA the best gain precision.

Note that for the CFOA only (*because of the negative node of the VFOA is buffered* **[23,24]**, when R_G is infinite, the opamp gain $A=\alpha R_Z/R_X$ because equal to $A'=\alpha R_Z/(R_X+R_F)$. Consequently, increasing R_F will insure a better stability, but a lower gain precision **[24]**. This has been confirmed by simulation (see Table 4 for R_F=10kΩ)

Non Inverting amplification: For G_0=10, Fig.12 shows the voltage gain responses versus frequency in the cases of no compensation and of compensation (comp. W1 and

W2); Here, at G_0=10, the ideal compensation capacitance values are 50fF and 60fF for the CFOA and the VFOA respectively (comp. W_2). If the compensation capacitances remain the same as the one chosen to compensate the amplifier when G_0=1, the bandwidth is drastically low (comp. W_1) **[24]**.

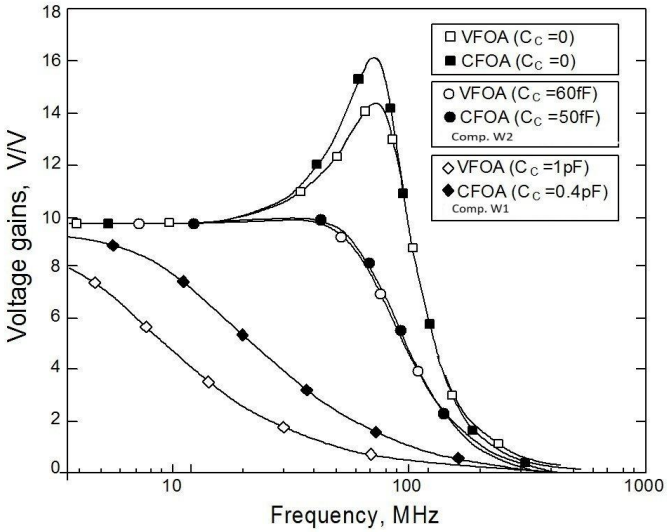


Figure 12. CFOA and VFOA frequency response at G_0=10, R_G=1kΩ, R_F=9kΩ :
No compensation : ■ CFOA (C_C=0), □ VFOA (C_C=0)
Comp. W_1 : ◆ CFOA ($C_C^{(1)}$=0.4pF), ◊VFOA ($C_C^{(1)}$=0.1pF)
Comp. W_2 : ● CFOA (C_C=50fF), ○ VFOA (C_C=60fF)
(1) with R_2=0 and $R_G \rightarrow \infty$

Fig.13 shows the slew-rates in case of the non-inverting amplifier applications when the close-loop gain is equal to G_0=10 (*at small-signal*) and with an input pulse of 150mVcc. Fig.13 shows that the CFOA and VFOA exhibit a high slew-rate when C_C is set versus the gain G_0 (comp. W2).

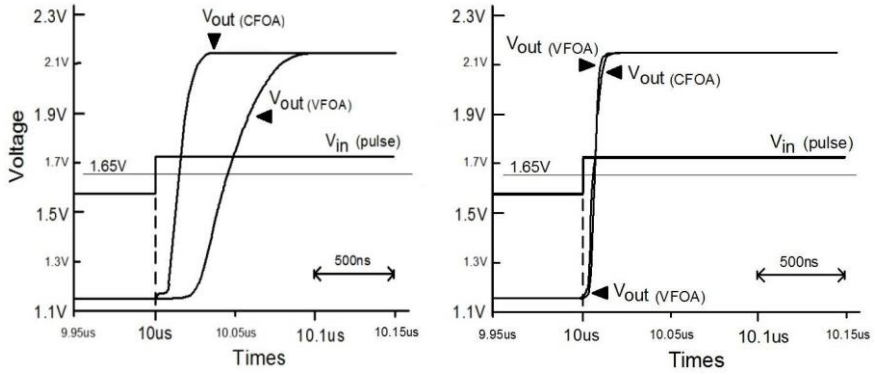


Figure 13. CFOA and VFOA output voltages when Vin is a pulse :
.PULSE (1.575 1.725 1n 1p 1p 5u 10u) @ G_0=10 :
-**a**- Comp. W_1 : compensation capacitances set for G_0=1, R_F=0, $R_G \rightarrow \infty$,
C_C(CFOA)=400fF and C_C(CFOA)=1pF
-**b**- Comp. W_2 : compensation capacitances set for G_0=10, R_F=9kΩ, R_G=1kΩ,
C_C(CFOA)=50fF and C_C(VFOA)=60fF

For R_G=1kΩ, the frequency performances (phase shift-error) at G_0=10 is shown in Fig.14 (comp. W2). A phase error shift of 1 degree always occurs around 1MHz for the VFOA. When G_0<3 the phase error occurs at higher frequencies for the CFOA, which means that, in our case, the CFOA provides betters frequency performance at low voltage gain.

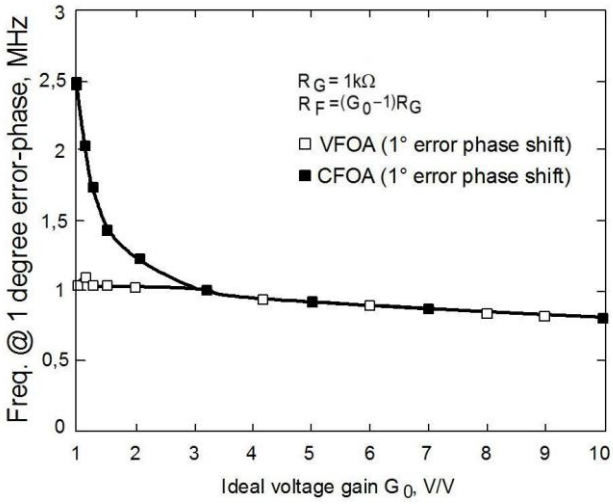


Figure 14. Frequency performances using C_C values in Fig.11 (comp. W2).

Fig. 15 shows the corresponding gain-bandwidth product (GBW). The GBW when C_C is set to G_0=1 is also drawn in Fig.15 (comp.W1).

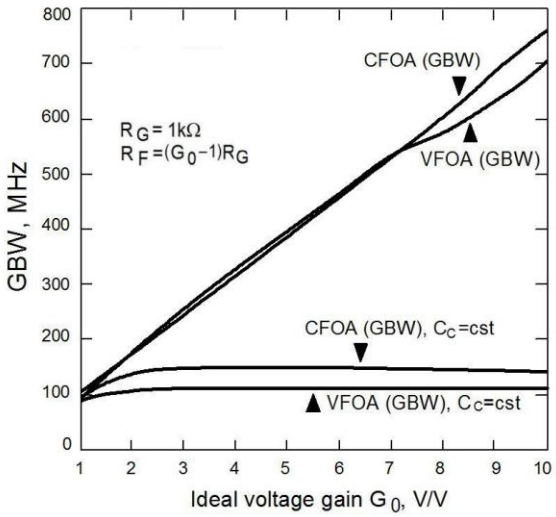


Figure 15. Gain Bandwidth product GBW
versus G_0 using C_C values in Fig.11 (comp. W2) and constant C_C (comp. W1)

Decreasing the compensation capacitances for G_0=10 (until the limit of resonance) provide a relatively same bandwidth of 80MHz and 75MHz for the CFOA and the VFOA respectively. Finally, the simulated voltage gain error is drawn in Fig. 16 for G_0 between 1 to 10.

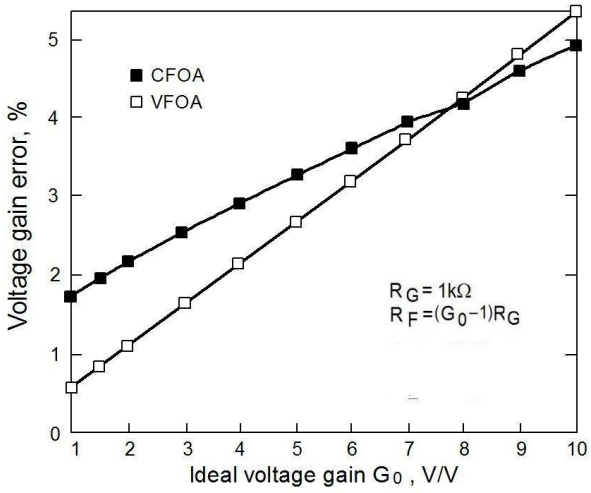


Figure 16. DC voltage gain error versus G_0 (comp. W1 or W2).

4. Conclusion

In this paper a comparison between similar CFOA and VFOA topologies has been proposed. The comparison has been made using the same transistor sizes and a similar power consumption. As the OTA is often used to define the voltage opamp (VFOA) input stage, this paper also shows that the OTC is a useful active cell allowing the CFOA input stages to be described. Considering the topologies simulated in this paper, the CFOA provides better frequency performances when it is used as unit (or low) gain amplifier. The VFOA has provided a better gain precision until a voltage gain of G_0=8. If the compensations capacitances are set in function of the voltage gain, the CFOA and the VFOA have provided relatively similar frequency performances when the voltage gain is high. We hope that this study will help the analog designers in future design of the CMOS OTA and OTC based opamps.

5. References

[1] Harold S. Black: "*Inventing the negative feedback amplifier*", IEEE Spectrum, vol. 14, pp. 54-60, Dec. 1977. (50th anniversary of Black's invention of negative feedback amplifier).

[2] H. Barthélemy, R. Vauché, V. Giès, S. Bourdel, J. Gaubert: "*Two-stage unbuffered CFOA based non-inverting resistive-feedback amplifier: a study based on the description of the operational transconductance conveyor (OTC)*", International journal of Analog Integrated Circuits and Signal Processing (AISCP), pp. 1-10, 2018.

[3] R. M. Thanki, H. R. Sanghani, R. K. Lamba: "*Design of Operational Transconductance Amplifier: Analysis of Schematic Circuit and CMOS Layout of OTA*", Publisher Lambert Academic Publishing 2011.

[4] R. Senani: "*Novel Analog Circuits using Op-amps, OTAs and Current Conveyors*", Ed. Lambert Acadmemic publishing, 2014-05-20, ISBN-10: 3659537462.

[5] Texas Instruments: "*OPA 860: Wide bandwidth operational transconductance amplifier (OTA) and Buffer*", SBOS331C- Revised august 2008, pp.1-27.

[6] R. Senani, D. Bhaskar, A. K. Singh, V. K. Singh: "*Current Feedback Operational Amplifiers and Their Applications*", Ed. Springer Science + Business Media New York 2013.

[7] K.C. Smith,A. Sedra: "*The current conveyor: a new circuit building block*". Proceeding IEEE CAS, vol. 56, no. 3, p. 1368-1369, 1968

[8] A. Fabre, O. Saaid, F. Wiest, F. Boucheron: "*High frequency applications based on a new current-controlled conveyor*". IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 43, no. 2, p. 82-91, 1996.

[9] Texas Instruments: "OPA 861: *Wide bandwidth operational transconductance amplifier (OTA)*", SBOS338G - Revised May 2013, pp.1-23.

[10] Analog Device: "*LTSPICE*", http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

[11] P. Antognetti, G. Massobrio: "*Semiconductor device modelling with spice*", Ed. Mc Graw-Hill, New-York 1990.

[12] Multi-Project Circuits: "*Products: IC Manufacturing : AMS 0.35 C35B4*", cmp.imag.fr/product/ic, www.ams.com.

[13] S-A. Tunheim: "*Implementation of CMOS Low Cost and Low Power RF-ICs*", Oslo, Norway, Wireless Systems Design Conference and Expo 2002, San Jose CA, February 25-28, pp. 1-11, 2002

[14] H. Barthélemy, S. Meillère, S. Bourdel: "*Single ended rail-to-rail CMOS OTA based variable-frequency ring-oscillator*", Proceedings of the 2004 International Symposium on Circuits and Systems (ISCAS '04), vol. 4, pp. 537-540, 2004.

[15] E. Bruun: "*Feedback analysis of transimpedance amplifier circuits*", IEEE Transaction on Circuits and Systems : part I, Vol. 40, No. 4, pp. 275-278, 1993

[16] I. Pandiev: " *Design and stability analysis of CFOA-based amplifier circuits using Bode criterion*", Systems Science & Control Engineering: An Open Access Journal, Vol. 3, pp. 367–380, 2015.

[17] M. Ron: "Anatomy of a voltage-feedback op amp," EDN, Oct 27, pp. 40, 2005

[18] M. Djebbi, A. Assi, M. Sawan: "*High-Frequency Offset-Compensated CMOS Current-Feedback Operational Amplifier*", 46th Midwest Symposium on Circuits and Systems, MWSCAS, 2003.

[19] H. J. Motlak: "*Design of CMOS CFOA Based on Pseudo Operational Transconductance Amplifier*", World Academy of Science, International Journal of Engineering and Technology, vol:8, n° 1, 2014

[20] S. Pennisi: "*High-performance CMOS current feedback operational amplifier*", 2005 IEEE International Symposium on Circuits and Systems, Kobe, vol. 2, pp. 1573-1576, 2005.

[21] OPA 3695: "*Triple,Ultra-Wideband,Current-Feedback operational amplifier with disable*", Texas-Instrument, SBOS355A–APRIL 2008–REVISED SEPTEMBER 2008, 2008.

[22] STMicroelectronics : "*Operational amplifier stability compensation methods for capacitive loading applied to TS507*", ST Microelectronics AN2653, Application note, rev. n1, 2007, pp. 1-22.

[23] Texas Instruments: "*Stability Analysis of Voltage Feedback OpAmps Including Compensation Techniques*", SLOA020A, Mixed Signal Products , Texas Instruments, March 2001

[24] Texas Instruments: "*Current Feedback Amplifier Analysis and Compensation*", SLOA021A, Mixed Signal Products, Texas Instruments, March 2001