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# Investigation of trap induced power drift on 0.15 $\mu\text{m}$ GaN technology after aging tests

F. Magnier<sup>a,b,\*</sup>, B. Lambert<sup>a</sup>, C. Chang<sup>a</sup>, A. Curutchet<sup>b</sup>, N. Labat<sup>b</sup>, N. Malbert<sup>b</sup>

<sup>a</sup> *United Monolithic Semiconductors, 10 avenue du Québec, 91140 Villebon-sur-Yvette, France*

<sup>b</sup> *Laboratoire IMS – Université de Bordeaux, 351 cours de la Libération, 33405 Talence, France*

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## Abstract

This paper deals with a power drift occurring during the first hours of aging tests on a 0.15  $\mu\text{m}$  GaN-based technology. Its purpose is to characterize the kinetic and the electrical features of this parasitic effect. Output power drift has been monitored by substituting interim RF power measurements by pulsed-IV measurements during high temperature reverse bias tests. Moreover, the kinetic of the output power drift has been assessed by reducing the time between interim measurements. Additional aging tests were performed at different temperatures to found out if **the degradation is temperature activated**. An interpretation is proposed about an increase of trap density responsible for drain lag effect after aging test at temperature higher than room temperature.

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## 1. Introduction

For years now, GaN-based high electron mobility transistors (HEMTs) are developed for microwave power applications due to their large band-gap, high electron mobility and high breakdown voltage. However, these devices display degradation mechanisms and parasitic effects that for some are not well-known. To ensure reliability, electrical performances and stability for these transistors, it is important to study and understand those effects, leading to a lot of researches on this subject [1-2-3].

Multiple parasitic effects have been found on GaN-based HEMTs like gate leakage current decrease or on-state resistance increase over time [4]. An output power drift has been observed after RF burn-in on GaN HEMTs for radar applications [5]. Even on mature GaAs technologies, Hwang has demonstrated a recoverable power drift after pulsed-IV stress test on pseudomorphic HEMTs [6].

In this paper, a power drift is investigated on a 0.15  $\mu\text{m}$  GaN technology submitted to High Temperature Reverse Bias (HTRB) tests. Pulsed-IV measurements are used to characterize the evolution of the electrical behaviour of the transistor and correlated to the RF output power. The technology under test is first introduced. Then the power drift phenomenon is presented. In the third part, the characterization methodology is described. The last

part is dedicated to the interpretation of the results.

## 2. Technology description

The MMIC technology under development is based on AlGaIn/GaN hetero-structure grown on 70  $\mu\text{m}$  SiC substrate. A 0.15  $\mu\text{m}$  gate process is achieved by e-beam lithography on SiN layers. A source terminated field plate overhangs T-shaped gate. It helps improving voltage withstand and also reducing feedback capacitance, which enhance RF gain. A maximum drain current of 1.2 A/mm is achieved with 400 mS/mm associated transconductance. The measured output power is greater than 3 W/mm with a Power Added Efficiency (PAE) of 40 % at 30 GHz on 300  $\mu\text{m}$  transistors biased at  $V_{ds} = 20$  V and  $I_d = 200$  mA/mm.

This technology intends to cover applications up to 35 GHz.

## 3. Power drift: phenomenon presentation

During an aging test, the output power drift is characterized by a variation in the range of -0.5 dB after the first interim measurement at 5 hours. Fig. 1 shows the evolution of the output power during

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\* Corresponding author. [florent.magnier@ums-gaas.com](mailto:florent.magnier@ums-gaas.com)  
Tel: +33 (016) 986 3338

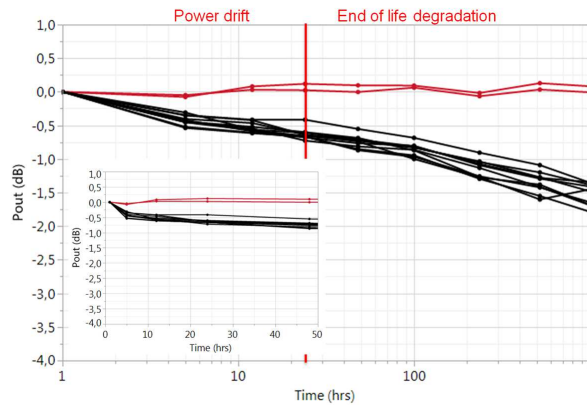


Fig. 1. Output power (at 5 dB gain compression) evolution during HTRB tests at  $T_{case} = 175\text{ }^{\circ}\text{C}$  ( $V_{ds} = 25\text{ V}$  and  $V_{gs} = -7\text{ V}$ ) of aged devices in black and references in red – RF measurement conditions are fixed at  $V_{ds} = 20\text{ V}$  and  $I_{ds} = 200\text{ mA/mm}$ .

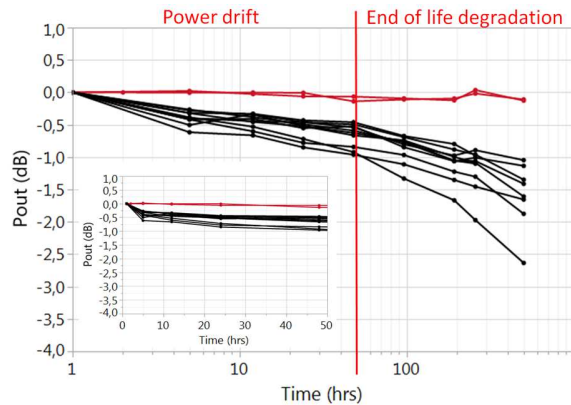


Fig. 2. Output power (at 5 dB gain compression) evolution during HTOL tests at  $T_j = 325\text{ }^{\circ}\text{C}$  ( $V_{ds} = 20\text{ V}$  and  $I_{ds} = 200\text{ mA/mm}$ ) of aged devices in black and references in red – RF measurement conditions are fixed at  $V_{ds} = 20\text{ V}$  and  $I_{ds} = 200\text{ mA/mm}$ .

HTRB test performed at  $V_{ds} = 25\text{ V}$  and  $V_{gs} = -7\text{ V}$  at  $T_{case} = 175\text{ }^{\circ}\text{C}$ . Same trend is also observed after High Temperature Operating Life (HTOL) tests performed at  $V_{ds} = 20\text{ V}$  and  $I_{ds} = 200\text{ mA/mm}$  at  $T_{case} = 175\text{ }^{\circ}\text{C}$  (see Fig. 2). This evolution is a parasitic effect that limits the performances of the technology. Indeed, after this initial drift, the output power remains constant until the degradation mechanism responsible for the transistor end of life occurs. The purpose of the study is to characterize the kinetic of the output power drift.

## 4. Methodology

### 4.1. High Temperature Reverse Bias tests

To characterize the kinetic of this parasitic

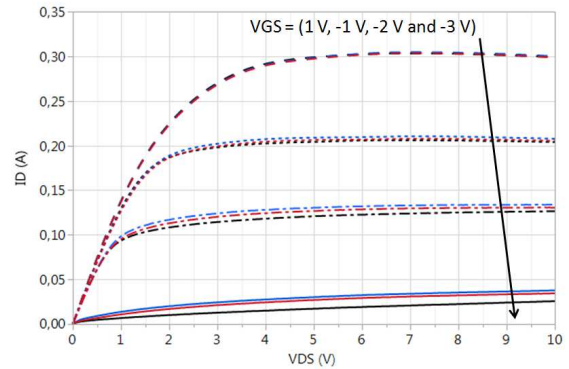


Fig. 3. DC output characteristic at  $V_{gs} = 1\text{ V}$  during HTRB test at  $175\text{ }^{\circ}\text{C}$  ( $V_{gs} = -7\text{ V}$  &  $V_{ds} = 30\text{ V}$ ); before aging in black, after 5 hours in blue and after 12 hours in red.

effect, High Temperature Reverse Bias (HTRB) tests have been performed with short interim measurements times. Such stress conditions allow a better control of the thermal effects during the stress. The applied life test conditions are  $V_{gs} = -7\text{ V}$  and  $V_{ds} = 30\text{ V}$  with a  $T_{case}$  ranging from  $25\text{ }^{\circ}\text{C}$  to  $200\text{ }^{\circ}\text{C}$ .

Transistors under test were soldered on copper carrier. HTRB tests were performed using a cryo-probe station from LakeShore Cryotronics; model TTPX. It operates over a temperature range of 4.2 K to 475 K.

### 4.2. Output power drift monitoring

DC measurements carried out at 5 hours and 12 hours of aging do not reveal any change at high gate voltage as shown in Fig. 3. Only a threshold voltage shift is observed at low gate voltage near threshold voltage leading to higher drain current. But it cannot explain RF power drop in saturation.

#### 4.2.1. Pulsed-IV measurements

Pulsed-IV measurements are suitable to characterize the dynamic electrical performances of the transistor and to correlate them with RF measurements. A methodology has been developed to calculate  $P_{out}$  from pulsed-IV measurements. The aim is to provide the analytical extraction of the output power during accelerated aging tests.

#### 4.2.2. Output power calculation method

##### - Parameters definition.

The output power of a transistor depends on the amplification class (see Fig. 4) defined by waveform of drain and gate voltages and resulting drain current. By definition,  $V_{ds}$  is sinusoidal and  $I_d$  is always positive. Thus, the first harmonic components

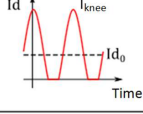
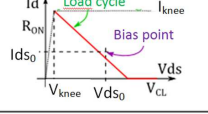
Class	Id temporal form	Load cycle - IdVd	Conduction angle $\varphi$
AB			$90^\circ < \varphi < 180^\circ$ $V_p \leq V_{GS0}$ et $V_{GS0} \leq \frac{V_{GS0MAX} + V_p}{2}$

Fig. 4. Definition of conduction angle and load cycle for class AB amplifier.

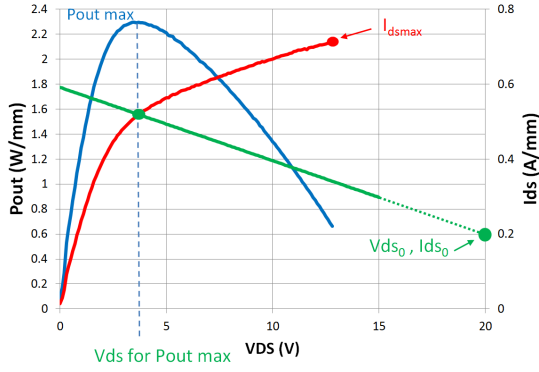


Fig. 5. Pulsed drain current in red, calculated output power in blue and associated load-line in green vs Vds.

of Fourier transform of both drain voltage and current are:

$$V_1 = \frac{V_{CL} - V_{knee}}{2} \quad (1)$$

$$I_1 = \frac{I_{knee}}{2\pi} \cdot \frac{2\varphi - \sin(2\varphi)}{1 - \cos(\varphi)} \quad (2)$$

$V_{knee}$  and  $I_{knee}$  are defined in Fig. 4.

From previous equations, Pout can be defined as:

$$Pout = \frac{I_1 \cdot V_1}{2} = \frac{I_{knee}}{2\pi} \cdot \frac{2\varphi - \sin(2\varphi)}{1 - \cos(\varphi)} \cdot \frac{V_{CL} - V_{knee}}{4} \quad (3)$$

Where  $\varphi$  is defined as conduction angle equals to:

$$\varphi = \frac{\left(180 - \arccos\left(\frac{2}{\alpha}\right)\frac{180}{\pi}\right)\pi}{180} \quad (4)$$

Where  $\alpha$  is equal to the ratio between the maximum drain current of pulsed-IV characteristic (at  $V_{gs} = 1$  V) and the value of bias drain current used for load-pull measurements.  $V_{CL}$  is the peak voltage of the load cycle. It is defined as:

$$V_{CL} = \beta(V_{ds0} - V_{knee}) \quad (5)$$

Where  $V_{ds0}$  is the DC voltage bias for RF applications and  $\beta$  a fitting parameter defined below. Using output pulsed-IV characteristic at  $V_{gs} = 1$  V

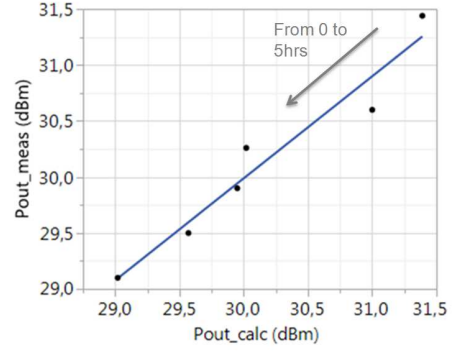


Fig. 6. Output power extracted from load-pull measurements at 4 dB gain compression versus output power calculated from pulsed-IV characteristics at  $V_{gs} = 1$  V ( $V_{GS0} = -5$  V and  $V_{ds0} = 20$  V) for one device during aging test.

(see Fig. 5) performed at quiescent point equal to  $-5V/20V$  to better represent RF swing, the output power is calculated with Eq.1 for each point of the output characteristic substituting  $V_{knee}$  and  $I_{knee}$  with drain voltage and current values. Maximum output power is then extracted and compared to the initial output power measured by load-pull.  $\beta$  is then fitted in order to have the maximum calculated Pout equal to initial output power measured.

Drain voltage and current values at Pout max define one point of the theoretical load-line while the second one ( $V_{ds0}$ ;  $I_{ds0} = 20$  V; 200 mA/mm) is the bias conditions for load-pull measurements. Then, extracted load-line and  $\beta$  parameter are kept constant for other calculation performed during interim measurements of aging tests.

- Application during aging tests.

Using Eq.1, Pout calculation is performed for all interim measurements substituting  $V_{knee}$  and  $I_{knee}$  with drain voltage and drain current at the intersection between pulsed output characteristic and extracted load-line.

Thanks to this internal methodology, theoretical available output power was extracted and plotted in Fig. 6 for one device during aging test as a function of the output power measured with load-pull. A linear correlation is found between the values of the output power measured and calculated.

Thus, interim RF power measurements can be substituted by pulsed-IV measurements to monitor output power drift. Pulsed-IV measurements are preferable than load-pull ones because less dependent on measurements uncertainties coming from calibration time stability and the sensitivity of the measurement environment.

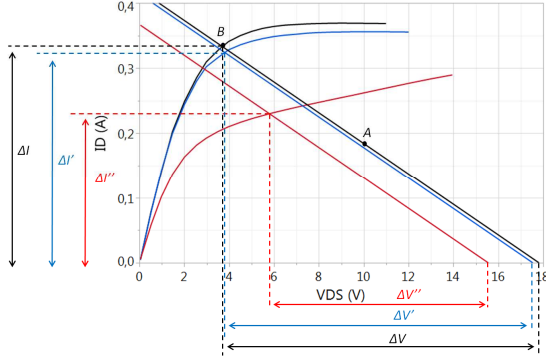


Fig. 7. Pulsed-IV characteristics at  $V_{gs} = 1V$  ( $V_{gsq} = 0V$  and  $V_{dsq} = 0V$  in black,  $-5V$  and  $0V$  in blue and  $-5V$  and  $30V$  in red) – Corresponding load-line to extract gate and drain lag, defined like a class-A amplifier.

#### 4.2.3. Gate lag and drain lag extraction

Pulsed-IV measurements were performed at three different quiescent points ( $V_{gsq}/V_{dsq}$ :  $0V/0V$ ;  $-5V/0V$ ;  $-5V/20V$ ) to assess the impact of HTRB stress at different interim measurements. Pulsed-IV measurements were performed using APMS pulsed system from MC2 with APMS-DA software. The pulse period is equal to  $30 \mu s$  with a duty cycle of 1%. Both gate lag and drain lag ratios are extracted in order to provide more insight contribution on traps responsible for power drift.

To extract gate lag and drain lag ratios, we used an internal power calculation definition based on a theoretical load-line defined in output characteristic at  $V_{gs} = 1V$  for quiescent points of  $V_{gsq} = 0V$  and  $V_{dsq} = 0V$ . This load-line is determined using two bias points as class-AB amplifier. The first one A is at half of the drain current at  $V_{ds} = 10V$  and the second one B is at a drain current equal to 90% of the maximum drain current at  $V_{gs} = 1V$  in order to reach typical load-line in class AB. Thanks to the load-line, current and voltage excursion ( $\Delta I$  and  $\Delta V$ ) are available for the quiescent point at  $V_{gsq} = 0V$  and  $V_{dsq} = 0V$ . For the two other quiescent points, load-line slope is the same. The load-line is only shifted to match the point at half of the drain current at  $V_{ds} = 10V$  to extract current and voltage excursions in the same amplification class (see Fig. 7).

Then gate lag (GL) and drain lag (DL) ratios are extracted as follow (see Eq. 6 and Eq. 7).

$$GL = 100. \left( 1 - \frac{\Delta I' \cdot \Delta V'}{\Delta I \cdot \Delta V} \right) \quad (6)$$

$$DL = 100. \left( 1 - \frac{\Delta I'' \cdot \Delta V''}{\Delta I' \cdot \Delta V'} \right) \quad (7)$$

The calculation of the GL and DL in Eq. 6 and Eq. 7 enhances the current drop occurring within the

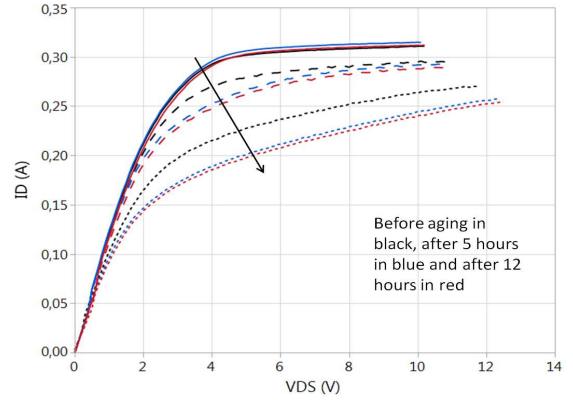


Fig. 8. Pulsed-IV characteristic before and during HTRB test measured at  $V_{gs} = 1V$  and  $V_{gs0} = 0V$  and  $V_{ds0} = 0V$  for solid lines,  $-5V$  and  $0V$  for dashed lines and  $-5V$  and  $20V$  for dotted lines with pulse period of  $30 \mu s$  and a duty cycle of 1%.

transition between ohmic and saturated regions on the contrary to the usual extraction made at a fixed  $V_{ds}$  value.

## 5. Results

### 5.1. Electrical signature and kinetic

As mentioned above, DC measurements do not reveal any change on the contrary to pulsed-IV ones. After aging tests, a decrease of the drain current is observed, especially in the transition between ohmic and saturated regions (see Fig. 8). Due to drain current collapse, both GL and DL ratios have increased and are correlated to output power drift.

While trapping phenomena have been extensively investigated in GaN HEMT [7-8], the purpose is to study the kinetic of the mechanism. Fig. 9 shows that both lag ratios are increasing after 30 minutes of HTRB test (first interim measurement) then remaining constant up to 24 hours when transistors are aged at  $175^\circ C$ .

No recovery has been observed for this phenomenon on different devices, even after storage of a device at  $175^\circ C$  for 2 days.

### 5.2. Impact of aging temperature

Similar HTRB tests were performed during 5 hours at different aging temperatures from  $25^\circ C$  up to  $200^\circ C$  to study the effect of the temperature on GL and DL ratios. In Fig. 10, the DL ratio is plotted for devices aged in HTRB conditions at  $25^\circ C$ ,  $100^\circ C$ ,  $150^\circ C$ ,  $175^\circ C$  and  $200^\circ C$ . Compared to HTRB at  $175^\circ C$ , at room temperature, no increase of the



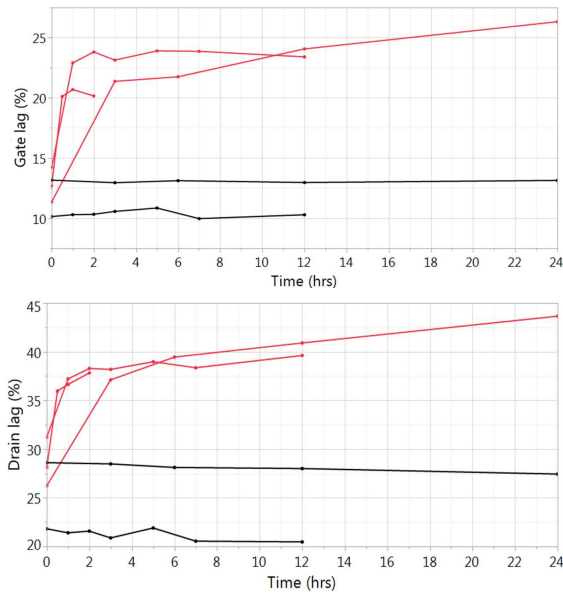


Fig. 9. Evolution of gate lag and drain lag ratios during HTRB tests at 175 °C for  $V_{gs} = -7$  V and  $V_{ds} = 30$  V (aged transistors in red, references transistors at aging temperature in black).

gate and drain lag ratios has been noticed. This means that the drain current drift in pulsed measurements and consequently GL and DL ratios increase are thermally activated. At higher temperature than room temperature, the GL and DL ratios increase after the first 30 minutes regardless of the temperature.

In Fig. 11, the DL and GL ratios increase versus aging temperature confirms that temperature is needed to activate the mechanism responsible for the power drift. Nevertheless, two hypotheses are still competing: (i) in the temperature range of 100 up to 150 °C, the GL and DL ratios increase after HTRB tests does not depend on the temperature. For temperature higher than 150 °C (175 °C and 200 °C), another mechanism might occur, explaining the larger increase of the GL and DL ratios after aging. (ii) GL and DL increase are dependent on aging temperature.

Thus, further investigations at lower temperature are needed to validate one of these two assumptions.

While it is observed that temperature above 25°C is necessary to activate the mechanism responsible for the power drift, no modulation of the time to reach a plateau is observed with the first interim measurement at 30 minutes.

## 6. Interpretation

As no drift of the DC measurements is visible on

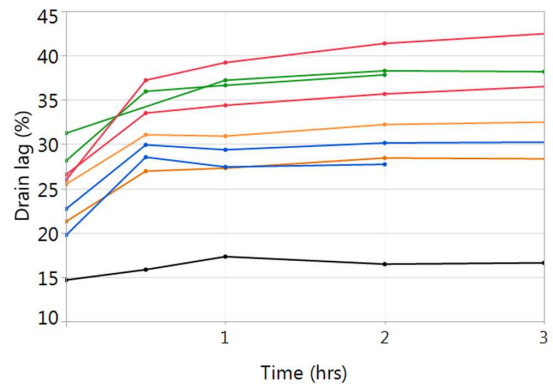


Fig. 10. Drain lag drift during HTRB tests with  $V_{gs} = -7$  V and  $V_{ds} = 30$  V (at aging temperature of 25 °C in black, 100 °C in orange, 125 °C in blue, 175 °C in green & 200 °C in red).

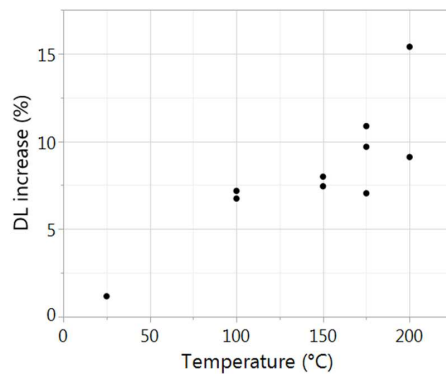
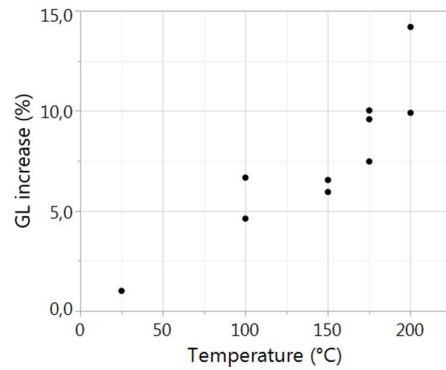


Fig. 11. Comparison of gate and drain lag ratio before and after HTRB tests ( $V_{gs} = -7$  V and  $V_{ds} = 30$  V) at different aging temperatures after 5 hours.

the contrary to pulsed-IV ones, the power drift is clearly induced by trap mechanisms. Output power drift is observed after aging tests and correlated with the increase of GL and DL ratios. Lag effects induce a smoothing of the transition between the ohmic and saturation regions of the output characteristic of the transistor in on-state operation. The effect is revealed

thanks to pulsed-IV characteristics at  $V_{gs0}/V_{ds0} = -5V/0V$  and  $-5V/20V$ .

In the literature, traps responsible for gate lag are presumed to be located in the barrier or at the surface, while traps responsible for drain lag are more likely located in the buffer [9].

During HTRB test, biasing conditions applied to transistors induces high electric field. Coupled with temperature, more traps centers are created and/or activated, thus increasing the amplitude of trap density resulting in output power drift. Trap density reaches saturation when no more trap centers can be created and/or activated with respect to the lateral electric field. The result is a stabilization of trap density and thus a stabilization of the output power.

At this stage of the study, trap location (for example at the surface or in the buffer) cannot be deduced from the data. Nevertheless, due to the high electric field, traps centers created and/or activated by HTRB tests are likely located between gate and drain area.

## 7. Conclusion

Power drift of GaN component has been studied, especially regarding its time constant and the impact of temperature. It is characterized by an output power drift around at the first interim measurement after accelerated aging tests in HTRB or HTOL conditions.

It has been shown that DC measurements are not able to monitor the drift on the contrary to pulsed-IV measurements. The transistor drain current drop occurs mainly within the transition between ohmic and saturated region on output characteristic, i.e. this transition becomes smoother. An original calculation based on the lag measurements has been proposed and allows getting a direct correlation with the transistor RF output power evolution. The GL and DL ratios increase lead to the output power drift seen after HTRB tests.

Regarding the kinetic of this effect, output power drift occurs before the first interim measurement after 30 minutes of HTRB stress. Then the values of lag ratios present no change. The time constant of this effect do not depend on different aging temperatures. However, temperature is needed to activate the phenomenon but the dependence with temperature is not clearly established.

This drift is probably due to an increase of traps density at the gate edge on the drain side. Electric field induced by HTRB tests along with temperature would create and/or activate traps thus increasing the trap density. This increase would lead to the

smoothing of drain current at the transition between ohmic and saturated region clearly detected in pulsed-IV measurements.

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