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# Impact of hot carrier aging on the performance of triple-gate junctionless MOSFETs

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**Abstract**— In this work, we investigate the impact of the hot carrier (HC) aging on the performance of nanoscale n-channel triple-gate junctionless MOSFETs with channel length varying from 95 down to 25 nm. The devices were electrically stressed in the on-state region of operation at fixed gate voltage  $V_g = 1.8$  V and drain bias  $V_d$  varying from 0.8 to 1.8 V, with the stress time being a variable parameter. The device degradation was monitored through the relative change with stress time of the threshold voltage, the subthreshold swing, the linear drain current and the gate current. We demonstrate that the HC degradation is exclusively due to the interface state generation when the stress voltage  $V_d$  is as high as  $V_g$ , following the energy driven HC model. For bias stress conditions with  $V_d/V_g < 1$  the threshold voltage and the subthreshold slope remain unchanged, whereas the on-state drain current is degraded, attributed to HC-induced damage restricted in the drain contact.

**Index Terms**— Degradation mechanisms, hot-carriers, junctionless, triple-gate MOSFETs.

## I. INTRODUCTION

JUNCTIONLESS (JL) multi-gate transistors have attracted much attention due to their high immunity to short channel effects (SCEs) and fabrication process simplification without requiring a complicated process to form the source/drain junctions [1]. In addition, the bulk conduction in JL transistors results in improved reliability, compared to the surface conduction of inversion mode (IM) transistors [2]. The high impact ionization rate in the drain region of n-channel JL nanowire MOSFETs [3], led to the investigation of their hot carrier (HC) degradation mechanisms. However, HC studies in JL multi-gate MOSFETs are limited to few works, referred on investigation of HC effects in triple-gate (TG) JL MOSFETs [4]-[6] and gate-all-around (GAA) JL nanowires [7]-[9]. Therefore, investigation of HC-induced degradation mechanisms in nanoscale JL multi-gate MOSFETs is a very

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important topic, since HC effect is a severe reliability issue in increasingly scaled transistors.

In multi-gate MOSFETs, HC effects become complicated compared to the IM devices because the conduction path of the drain current depends on the gate bias voltage. Comparative studies of HC effects have shown that the stress bias conditions for the worse device degradation are different in the JL and IM transistors depending on the device operation region [4]. In JL GAA MOSFETs, the HC degradation under on-state stress conditions is higher in relation to the off-state stress conditions due to the higher density of carriers confined in the center of the nanowire [8]. In p-channel TG JL MOSFETs the worst device degradation occurred at gate voltage  $V_g = V_t$  where  $V_t$  is the threshold voltage [5], whereas in n-channel transistors the worse device degradation occurred at drain voltage  $V_d = V_g$  [7], [8]. However, in conventional MOSFETs stressing at  $V_d/V_g$  ratio of bias conditions different than the worst case stress conditions, revealed new Si-H bond breaking mechanisms for interface states creation (such as, single-carrier process, multiple-carrier process, electron-electron scattering, dipole-field interaction, dispersion of Si-H bond energy) [10], [11].

In this work, we study the HC degradation of nanoscale n-channel TG JL MOSFETs stressed at fixed  $V_g$  in the on-state region of operation and different  $V_d/V_g$  bias conditions by monitoring the relative change with stress time of the threshold voltage  $\Delta V_t$ , the interface state density  $\Delta D_{it}$  through the relative change of the subthreshold swing and the linear drain current  $\Delta I_d$ , extracted from the experimental transfer characteristics in the linear region ( $V_d = 0.05$  V). The HC degradation mechanisms are supported with the experimental data of the gate current  $I_g$ .

## II. EXPERIMENTAL DETAILS

The HC experiments were performed on n-channel TG JL MOSFETs with fin height  $H_{fin} = 10$  nm, fin width  $W_{fin} = 18$  nm and channel length  $L$  varying from 95 down to 25 nm, fabricated by CEA-LETI. The high-k metal gate stack consists of HfSiON/TiN/p<sup>+</sup>-polysilicon with an equivalent oxide thickness equal to 1.2 nm and the doping concentration of the channel is  $2 \times 10^{19}$  cm<sup>-3</sup>. Details of the device fabrication processes are presented in [12].

In the HC experiments, the devices were stressed in the on-state operation region by applying fixed gate voltage above the flat-band voltage ( $V_g = 1.8$  V), drain bias voltage  $V_d$  varying from 0.8 to 1.8 V, with the source and substrate terminals

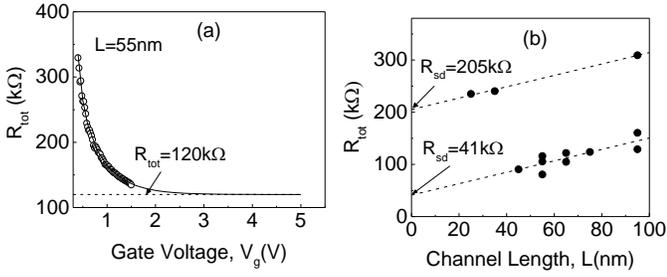


Fig. 1. (a) Total resistance  $R_{tot}$  as a function of gate voltage  $V_g$  for TG JL MOSFET with  $L = 55$  nm before stress. Symbols are experimental measurements and solid line is a second-order exponential curve fitting to the experimental data. (b) Extracted series resistance  $R_{sd}$  for TG JL MOSFETs.

grounded and the stress time being a variable parameter. The stress was interrupted at selected stress times to measure the transfer characteristics ( $I_d$ - $V_g$ ) using an Agilent B1500/1530 Semiconductor Device Analyzer. No observable recovery was found in the device characteristics after HC stress.

### III. RESULTS AND DISCUSSION

Due to the high source/drain series resistance  $R_{sd}$  of the investigated devices, the second derivative of the drain current method for extracting the threshold voltage  $V_t$  cannot be used [13], since the transconductance  $g_m$  and, therefore, in JL transistors the measured  $V_t$  would be underestimated [14], [15]. The series resistance  $R_{sd}$  has been extracted following a simple extraction technique based on the measured total resistance  $R_{tot} = V_d/I_{d,tot}$  as a function of the gate voltage, where  $I_{d,tot}$  is the measured drain current and  $R_{tot}$  is the sum of the source/drain series resistance and the channel resistance [15]. After determining the constant value of the total resistance  $R_{tot}$  in the voltage range of  $V_g > 2$  V for different channel lengths, the  $R_{sd}$  value can be estimated from the intercept of the linear extrapolation of the  $R_{tot}$  versus gate length  $L$  plot [15]. Fig. 1(a) shows experimental plot of  $R_{tot}$  versus  $V_g$  for a typical TG JL MOSFET with  $L = 55$  nm and a second-order curve fitting to the experimental data, resulting in a constant value of the total resistance  $R_{tot} = 120$  k $\Omega$  in the voltage range of  $V_g > 2$  V. The extracted constant values of  $R_{tot}$  for different channel lengths are presented in Fig. 1(b). Two separate groups of data are observed, showing a linear decrease of  $R_{tot}$  with decreasing  $L$  resulting in values of  $R_{sd} = 41$  and 205 k $\Omega$ . This finding reveals the occurrence of series resistance variability in the JL transistors. Once  $R_{sd}$  has been determined, its effect on the drain current can be eliminated by correcting the measured drain current  $I_{d,tot}$  as [14]:

$$I_d = \left( \frac{V_d}{I_{d,tot}} - R_{sd} \right)^{-1} \times V_d. \quad (1)$$

The impact of the drain voltage on the HC-induced damage has been investigated by applying a fixed gate voltage  $V_g = 1.8$  V in the on-state regime and drain voltage  $V_d = 0.8, 1.2, 1.5$  and 1.8 V. Fig. 2 presents the experimental  $I_d$ - $V_g$  characteristics in semi-logarithmic and linear representation of typical long TG JL MOSFETs with  $L = 95$  nm, submitted to  $V_d/V_g < 1$  HC stress conditions for different stress times  $t_s$ . It

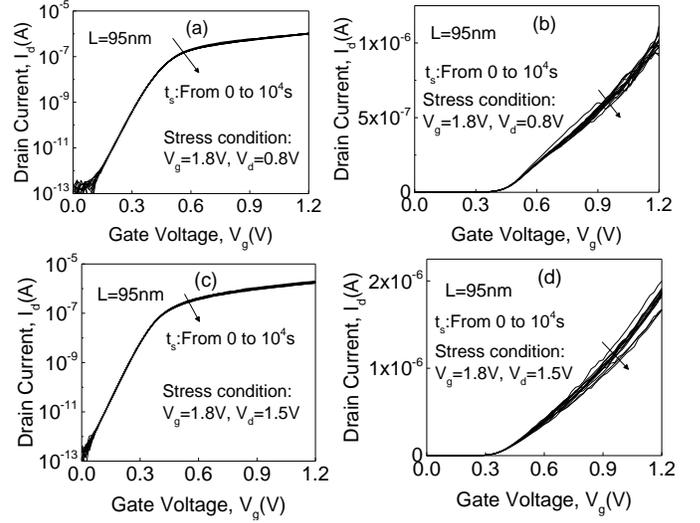


Fig. 2.  $I_d - V_g$  characteristics of TG JL MOSFET with channel length  $L = 95$  nm in semi-logarithmic and linear representation before and after HC stress at  $V_g = 1.8$  V,  $V_d = 0.8$  V and  $V_g = 1.8$  V,  $V_d = 1.5$  V, measured at drain voltage  $V_d = 0.05$  V and different stress times  $t_s$ .

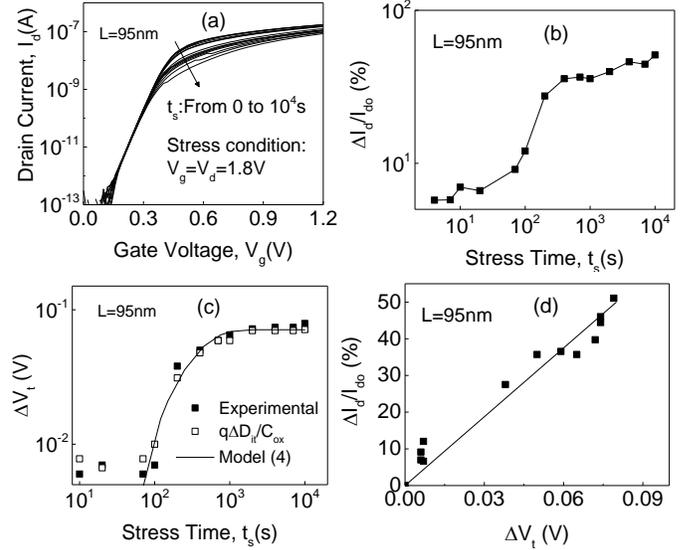


Fig. 3.  $I_d - V_g$  characteristics of TG JL MOSFET with channel length  $L = 95$  nm before and after HC stress at  $V_g = V_d = 1.8$  V, measured at drain voltage  $V_d = 0.05$  V after different the stress times  $t_s$ . (b) Variation with stress time of the relative drain current  $\Delta I_d/I_d$  (%) measured at  $V_d = 0.05$  V and  $V_g = 1.2$  V. (c) Variation with stress time of the threshold voltage shift  $\Delta V_t$  (solid symbols: experimental data, open symbols:  $q\Delta D_i/C_{ox}$ ). The line corresponds to the model (4) using the parameters  $V_0 = 0.071$  V and  $R_t = 0.007$  s $^{-1}$ . (d) Correlation of the experimental  $\Delta I_d/I_d$  (%) with  $\Delta V_t$ .

is clearly seen that when the  $V_d/V_g$  ratio of stress conditions is lower than unity no observable changes in the subthreshold slope and threshold voltage are observed, resulting only in a small degradation of the on-state drain current. This behavior indicates that the HC-induced damage is restricted inside the drain region, where the peaks of the lateral electric field and impact ionization rate are located [5], [9], [16]. This finding is in contrast to that found in IM transistors, where for  $V_d/V_g < 1$  small degradation level for  $I_d$  results in large degradation for  $V_t$  attributed to the low energy carriers mechanism (multiple particle process) [10].

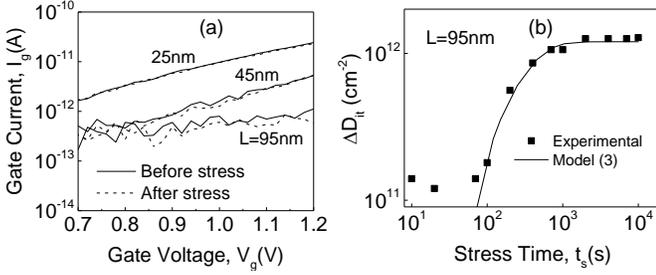


Fig. 4. (a) Gate current versus gate voltage, measured at drain voltage  $V_d = 0.05$  V before and after HC stress at  $V_g = V_d = 1.8$  V for  $10^4$  s in TG JL MOSFETs of different channel lengths. (b) Extracted interface trap concentration with stress time in TG JL MOSFET with channel length  $L = 95$  nm, stressed at  $V_g = V_d = 1.8$  V. The symbols are experimental data and the line the model results (3), using the parameters  $N_0 = 1.2 \times 10^{12} \text{ cm}^{-2}$  and  $R_{it} = 0.007 \text{ s}^{-1}$  in the stress time region above 50 s.

Fig. 3(a) presents the  $I_d$ - $V_g$  characteristics of long TG JL MOSFET ( $L = 95$  nm), submitted to HC stress at  $V_d/V_g = 1$  ( $V_g = V_d = 1.8$  V) for different stress times. The results of Figs. 2 and 3(a) show that the worst HC degradation occurs at  $V_d = V_g$  bias conditions, in agreement with the findings of previous work [7], [8]. The relative change with stress time of the macroscopic transistor parameters of the linear drain current  $\Delta I_d/I_d$  (%) =  $-100 \times (I_d(t_s) - I_{d,0})/I_{d,0}$  and the relative change of the threshold voltage  $\Delta V_t = V_t(t_s) - V_t(0)$  are presented in Figs. 3(b) and 3(c), respectively. At the initial stages of stress the degradation of  $I_d$  and  $V_t$  is relatively small, whereas for stress time above 50 s both parameters degrade fast tending to saturation. The correlation between  $\Delta I_d/I_d$  (%) and  $\Delta V_t$  presented in Fig. 3(d) shows that a high degradation level of  $I_d$  results in a small degradation of  $V_t$ . This finding indicates that in the long channel JL transistor, the HC-induced degradation at  $V_g = V_d = 1.8$  V is localized at the drain side [10], [17].

In order to clarify the origin of the degradation mechanisms of the macroscopic transistor parameters, we considered the microscopic transistor parameters, such as interface trap ( $D_{it}$ ) and oxide trap ( $N_{ox}$ ) densities. The change of the threshold voltage  $\Delta V_t$  with stress time can be correlated with the change of the interface trap density  $\Delta D_{it}$  and/or the change of the oxide trap density  $\Delta N_{ox}$  by the relationship [18]:

$$\Delta V_t = \Delta V_t(D_{it}) + \Delta V_t(N_{ox}) = q \frac{\Delta D_{it}}{C_{ox}} + q \frac{\Delta N_{ox}}{C_{ox}}, \quad (2)$$

where  $q$  is the elementary charge and  $C_{ox}$  is the gate oxide capacitance per unit area.  $\Delta D_{it}$  and  $\Delta N_{ox}$  have dimensions of states/ $\text{cm}^2$ . Given that the gate current is not increased after stress for all channel lengths as shown in Fig. 4(a), this implies that the threshold voltage shift is mainly due to the HC-generated interface states rather than to HC stress-generated gate oxide traps, that could give rise to stress induced leakage current (SILC).

The positive  $V_t$  shift after HC stress indicates the presence of negatively charged interface states, i.e. acceptor-like traps which are negatively charged when occupied. In n-channel JL transistors, the energy range  $\Delta E$  over which the interface states are occupied and contribute to the negative charge corresponds to the silicon band-gap. For assessing the relative importance

of the negative charge from interface states, considering uniform energy distribution of the interface states, the HC-generated interface trap density was extracted from the subthreshold swing change  $\Delta SS$  using the relation  $\Delta D_{it} = \Delta SS \cdot C_{ox} \cdot \Delta E / q \cdot kT \cdot \ln(10)$ . The dependence of the HC-induced interface states concentration  $\Delta D_{it}$  with stress time, extracted from the subthreshold slope change [18], is presented in Fig. 4(b) for the TG JL MOSFET with channel length  $L = 95$  nm. Figs. 3(c) and 4(b) show clearly that the threshold voltage shift with stress time is closely related with the HC-generated interface states density. The experimental  $\Delta V_t$  are compared to the calculated  $\Delta V_t(D_{it}) = q \Delta D_{it} / C_{ox}$  in Fig. 3(c). The coincidence of these data confirms that the HC degradation of the macroscopic TG JL transistor parameters is exclusively due to interface states created during HC stress. Thus, in the TG JL transistor with  $L = 95$  nm interface damage dominates the whole degradation, rather than HC injection into the gate oxide bulk defects. This result is different from that found in IM channel FinFETs, where the main degradation mechanism is the HC injection into the gate oxide bulk defects [18]. This differentiation may be due to the bulk conduction in JL transistors instead of the surface conduction in IM transistors.

For the TG JL MOSFET with  $L = 95$  nm, at the initial stages of stress  $\Delta D_{it}$  is low remaining almost unchanged [Fig. 3(c)]. As the stress proceeds further, above 50 s the interface states density increases tending to saturation. Similar behavior of the interface trap density with stress time has been observed in short channel IM FinFETs [18], [19]. Following the energy-driven HC model for single particle or multiple particle Si-H bond breaking process [20] and accounting for saturation of the degradation, in the stress time region above 50 s the interface states generation can be modeled by the relationship [10]:

$$\Delta D_{it} = N_0 \left[ 1 - \exp\left(- (R_{it} \cdot t)^{0.5}\right) \right], \quad (3)$$

where  $N_0$  is the saturation value of  $\Delta D_{it}$  and  $R_{it}$  is the interface states generation rate. In Fig. 4(b), the line corresponds to the model results obtained from (3) using the parameters  $N_0 = 1.2 \times 10^{12} \text{ cm}^{-2}$  and  $R_{it} = 0.007 \text{ s}^{-1}$ . At the same time, Fig. 3(c) shows that the threshold voltage change  $\Delta V_t$  follows the relationship:

$$\Delta V_t = V_0 \left[ 1 - \exp\left(- (R_t \cdot t)^{0.5}\right) \right], \quad (4)$$

where  $V_0 = 0.071$  V is the saturation value of  $\Delta V_t$  and  $R_t = 0.007 \text{ s}^{-1}$  is the threshold voltage degradation rate, which is equal to the interface states generation rate.

Fig. 5(a) presents the  $I_d$ - $V_g$  characteristics of a shorter TG JL MOSFET ( $L = 45$  nm), subjected to HC stress at  $V_g = V_d = 1.8$  V for different stress times. It is clearly shown that the transistor macroscopic parameters of the drain current, subthreshold swing and threshold voltage are degraded with increasing the stress time. The relative change with stress time of  $\Delta I_d/I_d$  (%) and  $\Delta V_t$  are presented in Figs. 5(b) and 5(c), respectively. The time dependent power law factor of  $I_d$  degradation in short TG JL MOSFET is 0.27, which is close to

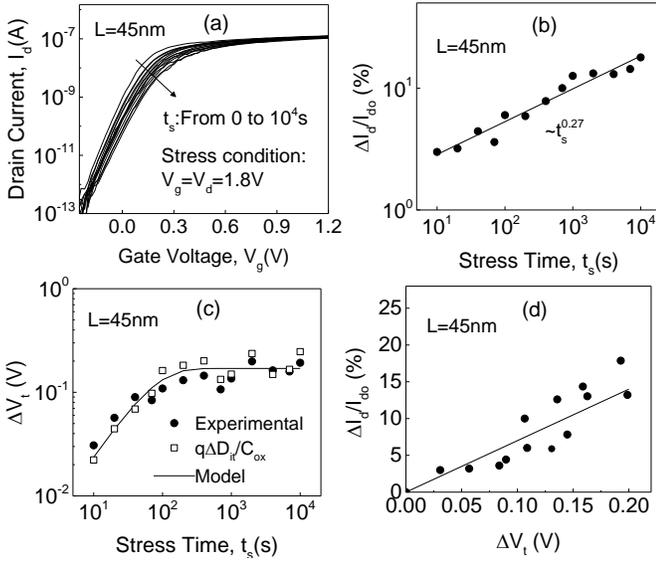


Fig. 5.  $I_d - V_g$  characteristics of TG JL MOSFET with channel length  $L = 45$  nm before and after HC stress at  $V_g = V_d = 1.8$  V, measured at drain voltage  $V_d = 0.05$  V after different stress times  $t_s$ . (b) Variation with stress time of the relative drain current  $\Delta I_d/I_d$  (%) measured at  $V_g = 1.2$  V. (c) Variation with stress time of the threshold voltage shift  $\Delta V_t$  (solid symbols: experimental, open symbols:  $q\Delta D_{it}/C_{ox}$ ). The line corresponds to the model (4) using the parameters  $V_0 = 0.17$  V and  $R_{it} = 0.03$  s $^{-1}$ . (d) Correlation of the experimental  $\Delta I_d/I_d$  (%) with  $\Delta V_t$ .

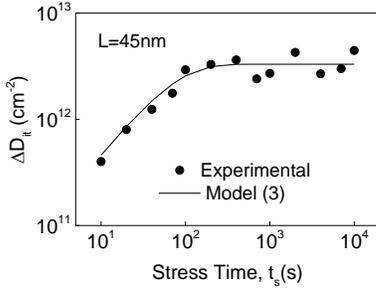


Fig. 6. Extracted interface trap concentration with stress time in TG JL MOSFET with channel length  $L = 45$  nm, stressed at  $V_g = V_d = 1.8$  V. The symbols are experimental data and the line the model results (3), using the parameters  $N_0 = 3.3 \times 10^{12}$  cm $^{-2}$  and  $R_{it} = 0.03$  s $^{-1}$ .

half of the typical time dependent power law factor (0.5) in large planar devices [16]. As shown in Figs. 5(c) and 6, the change in  $V_t$  and interface states density are increasing with stress time tending to saturation after about  $10^2$  s. Comparison of the experimental  $\Delta V_t$  with the calculated  $\Delta V_t(D_{it}) = q\Delta D_{it}/C_{ox}$  in Fig. 5(c) confirms that the HC degradation of the macroscopic device parameters is due to the HC-generated interface states. The interface states generation can be modeled by (3) with  $N_0 = 3.3 \times 10^{12}$  cm $^{-2}$  and  $R_{it} = 0.03$  s $^{-1}$  and the threshold voltage change by (4) with  $V_0 = 0.17$  V and  $R_t = 0.03$  s $^{-1}$ .

Fig. 7(a) presents the  $I_d - V_g$  characteristics of a short TG JL MOSFET with  $L = 25$  nm, stressed at  $V_g = V_d = 1.8$  V for different stress times. We note that a continuous degradation of the subthreshold swing is observed in the subthreshold region after long stress time ( $t_s > 200$  s), likely due to HC generation of interface states with continuous energy distribution in the silicon band-gap [21] and/or to a non-

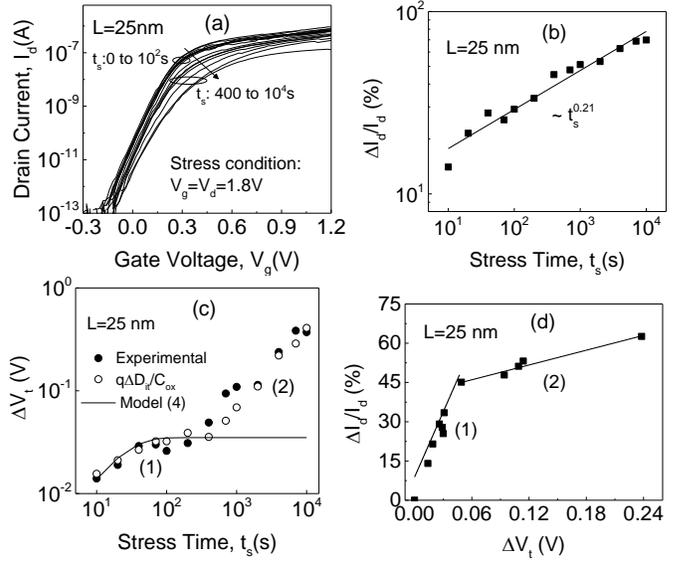


Fig. 7.  $I_d - V_g$  characteristics of TG JL MOSFET with channel length  $L = 25$  nm before and after HC stress at  $V_g = V_d = 1.8$  V, measured at drain voltage  $V_d = 0.05$  V after different stress times  $t_s$ . (b) Variation with stress time of the relative drain current  $\Delta I_d/I_d$  (%) measured at  $V_d = 0.05$  V and  $V_g = 1.2$  V. (c) Variation with stress time of the threshold voltage shift  $\Delta V_t$  (solid symbols: experimental data, open symbols:  $q\Delta D_{it}/C_{ox}$ ). The line corresponds to the model (4) using the parameters  $V_0 = 0.035$  V and  $R_{it} = 0.1$  s $^{-1}$ . (d) Correlation of the experimental  $\Delta I_d/I_d$  (%) with  $\Delta V_t$ .

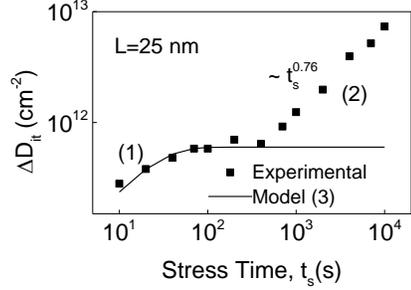


Fig. 8. Extracted interface trap concentration with stress time in TG JL MOSFET with channel length  $L = 25$  nm, stressed at  $V_g = V_d = 1.8$  V. The symbols are experimental data and the line corresponds to the model (4) using the parameters  $N_0 = 6 \times 10^{11}$  cm $^{-2}$  and  $R_{it} = 0.1$  s $^{-1}$ .

uniformity effect in their spatial distribution along the channel length [11]. However, to study the impact of the HC aging on the performance of the device with  $L = 25$  nm, an average value of the subthreshold slope was extracted from the transfer characteristics.

The change with stress time of the macroscopic transistor parameters  $\Delta I_d/I_d$  (%) and  $\Delta V_t$  are presented in Figs. 7(b) and 7(c), respectively. The time dependent power law factor of  $I_d$  degradation in short TG JL MOSFET ( $L = 25$  nm) is 0.21, which is less than half of the typical time dependent power law factor (0.5) in large planar devices [16]. The relative degradation of  $V_t$  is small at the initial stages of stress (time domain 1) and after about 200 s  $\Delta V_t$  increases fast (stress time domain 2). In Fig. 7(d), the correlation between the linear drain current degradation and the threshold voltage change is presented. In the stress time domain (1), a high degradation level of  $I_d$  results in a small degradation of  $V_t$ , indicating that at the initial stages of HC stress the degradation is localized at

the drain side. As the stress proceeds further (stress time domain 2), a small degradation level of  $I_d$  results in a large degradation of  $V_t$ , indicating that the degradation is along the channel length [10].

The dependence of the HC-induced interface states concentration  $\Delta D_{it}$  with stress time, extracted from the subthreshold swing change, is presented in Fig. 8 for the TG JL MOSFET with channel length  $L = 25$  nm. Comparison of the experimental  $\Delta V_t$  with the calculated  $\Delta V_t(D_{it}) = q\Delta D_{it}/C_{ox}$  confirms that the HC degradation of the macroscopic TG JL transistor parameters is exclusively due to interface states created during HC stress independently of the channel length [Fig. 7(c)]. For the short TG JL MOSFET ( $L = 25$  nm), at the initial stages of stress  $\Delta D_{it}$  increases slowly tending to a saturation as shown in Fig. 8 (stress time domain 1). In the stress time domain 1, the density of the interface states generation can be modeled by (3) using the parameters  $N_0 = 6.2 \times 10^{11} \text{ cm}^{-2}$  and  $R = 0.1 \text{ s}^{-1}$  and the threshold voltage change  $\Delta V_t$  follows (4) using the parameters  $V_0 = 0.035 \text{ V}$  and  $R = 0.1 \text{ s}^{-1}$ . It is noted that the interface states generation rate  $R_{it}$  is significantly increased from 0.007 to  $0.1 \text{ s}^{-1}$  when the channel length is reduced from 95 to 25 nm. Such behavior is expected due to the increased impact ionization rate at the drain of JL transistors of shorter channel length [9], [22]. As the stress proceeds further, for stress time exceeding 200 s (stress time domain 2), the interface states and threshold voltage degradation rates are increased following a time dependent law of the form  $\sim t_s^{0.76}$ . The high value of the time exponent (0.76) can be related to the non-uniform energy and/or spatial distribution of the HC generated interface states.

#### IV. CONCLUSION

The hot-carrier degradation mechanisms in nanoscale n-channel TG JL MOSFETs were extensively investigated by studying the evolution with stress time of the macroscopic (threshold voltage, linear drain current, gate current) and microscopic (interface states) device parameters. Devices with channel lengths 95, 45 and 25 nm were electrically stressed in the on-state region of operation at fixed gate voltage  $V_g = 1.8 \text{ V}$  and drain bias  $V_d$  varying from 0.8 to 1.8 V, with the stress time as a variable parameter.

For  $V_d/V_g < 1$  ratio of stress conditions, the HC-induced damage is located inside the drain region, resulting in a small degradation of the on-state drain current. When the stress voltage  $V_d$  is as high as  $V_g$ , the HC-induced degradation mechanisms are dominated by generation of interface traps. For long channel device ( $L = 95$  nm), the HC-induced damage is localized at the drain side with the interface states generation following the energy-driven HC model for Si-H bond breaking. For shorter device ( $L = 45$  nm), the HC-induced degradation is extended along the channel length, while for very short device ( $L = 25$  nm) the HC-induced degradation results in severe degradation of the subthreshold transfer characteristics, exhibiting a continuous degradation of the subthreshold swing.

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