

Characterization of a 4H-SiC High Power Density Controlled Current Limiter

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Most of silicon devices such as Schottky diode, MOSFET, MESFET have been realized in SiC and show good electrical and thermal characteristics [1]. Considering fault current limiters for serial protection, a lot of structures exists [2, 3], from conventional fuses to other complex systems such as circuit breakers, mechanical switches. Up to now, few specific SiC-current limiter were described [4, 5]. This paper presents experimental characterization of a bi-directional current limiter structure based on a vertical SiC VJFET. This device was designed for serial protection in order to limit I^2t value. In steady state, the voltage drop across the component must be as low as possible. In the limiting state, a current limiter must sustain a high current, under high voltage bias. The resulting high power density must not cause the failure of the component. We have focused our study on two critical process steps of such SiC devices, that are thermal annealing and metal ohmic contact formation focusing on their stability during working operation.

The temperature dependence of contact and sheet resistivities was measured using TLM structures. The extracted contact resistivities underline stability for N type Ni/SiC contact in the range of 175K – 450K. In this temperature range, the measured value remains constant around $40\mu\Omega.cm^2$ on highly doped layer as shown in figure 1. In case of a lower layer doping concentration, the contact resistivity temperature dependence remains low. The evolution of the sheet resistivity, R_{sh} is attributed to the carrier mobility temperature dependence. VJFET I-V characteristics allow correlating the experimental mobility change with temperature with the model used in simulation (figure 2). Based on specific resistance variation with temperature, the extracted mobility temperature dependence coefficient is $\alpha = 2,04$ (similar to values used in [6]). The RTA post implantation annealing effect on R_{\square} has been investigated (Tab1.).

This work underlines the fabrication requirement of good ohmic for high power density device. Both lowest value and thermal stability versus temperature are both needed. Measurements shown ohmic contact stability from 200 K up to 450 K (range of temperature reached during limiting mode). A post implantation thermal annealing and metal process have been setup and lead to optimistic results for the fabrication of higher capabilities devices (a rising up in terms of cells current). Additional measurements on packaged devices will complete these measurements in order to validate both high power density capability and thermal stability of the electrode contact of this high voltage current limiter.

[1] H.Matsunami, « Progress in Wide Bandgap Semiconductor SiC for Power Devices », invited paper, ISPSD'00 22-25 May 2000, Toulouse

[2] Sze, « Physics of semiconductors », p351-353, 2nd Edition Wiley.

[3] Semitec Corp. Current Regulative Diode Distributor.

[4] Siemens Corp. « Current limiter circuit », Patent n°W09727657, 30/07/97,

[5] F. Nallet « Electrical and Electrothermal 2D simulation of a 4H-SiC High Voltage Current limiting Device for serial protection application », pp287-290, ISPSD'00 22-25 May 2000, Toulouse.

[6] M. Ruff, « SiC devices : Physics and Numerical Simulation », IEEE Trans. Electron Devices ED-41 n°6 June 1994.

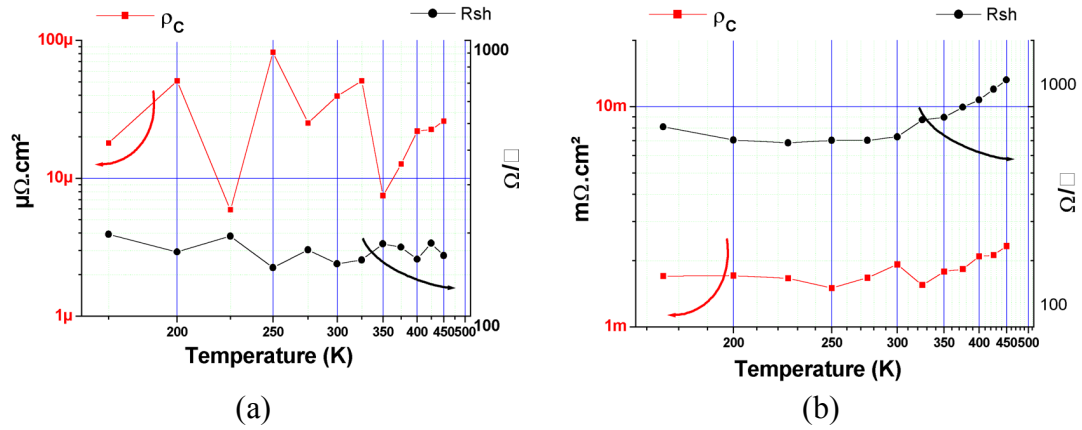


Fig. 1. Contact resistivity and R_{\square} variation versus temperature for high dose 10^{15} cm^{-2} (a), and low dose 10^{13} cm^{-2} (b) N implanted layers

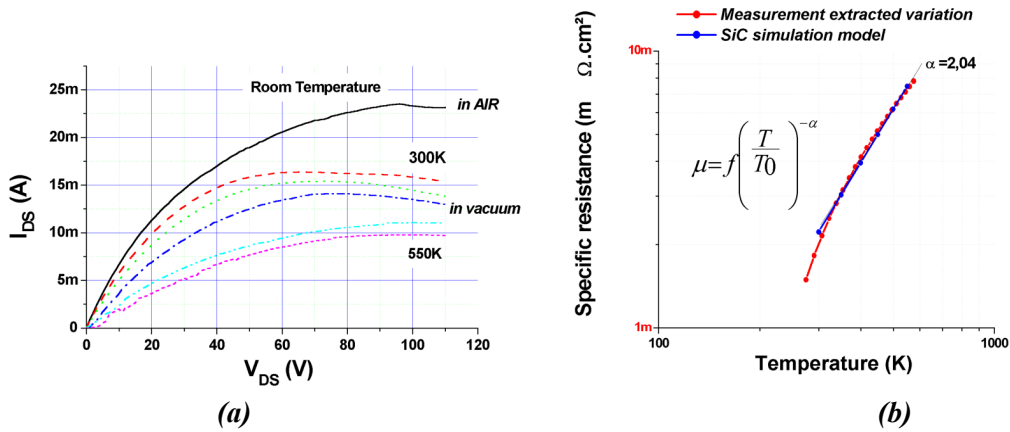


Fig. 2. VJFET thermal characterization: $I(V)$ (a) and specific resistance (b)

Annealing setup	N ⁺ layer (Dose = 10^{15} cm^{-2})	N layer (Dose = 10^{13} cm^{-2})
	R_{\square}	R_{\square}
1650 °C / 60min 4H	1105	4015
1700 °C / 30min	4H	3007
	6H	2886

Tab. 1. R_{\square} for two post implantation annealing setups