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# Exploiting Transistor Folding Layout as RHBD Technique against Single-Event Transients

Y. Q. Aguiar, F. Wrobel, J-L. Autran, F. L. Kastensmidt, P. Leroux, F. Saigné, V. Pouget and A. D. Touboul

**Abstract**— Radiation hardening techniques can be extensively used in the design level to improve the robustness of VLSI circuits used in space applications. Accordingly, this work analyzes the efficiency of transistor folding layout in improving the Single-Event Transient robustness of digital circuits. Additionally, diffusion splitting is proposed to reduce the area overhead of multiple-finger designs. Besides increasing threshold Linear Energy Transfer, results show that both techniques can also reduce the overall cross-section and the in-orbit SET rate for protons and heavy ions in LEO and ISS orbits.

**Index Terms**—Transistor Folding, Radiation Hardening by Design (RHBD), Single-Event Transient, Monte-Carlo simulation, Circuit Design

## I. INTRODUCTION

THE susceptibility to energetic particles increases as the transistor feature size is reduced [1-3]. Due to the extensive usage of electronics systems in harsh environments, mitigation techniques against radiation effects have been vastly investigated in literature [4-7]. Radiation hardening strategies can be explored from fabrication process modifications to different design implementations. Modifications of doping profiles, optimization of deposition processes and usage of different materials are examples of well-known Radiation Hardening by Process (RHBP) techniques. However, besides its higher cost, RHBP are typically several generations behind the state-of-the-art CMOS process, leading to low-grade performance. On the other hand, Radiation Hardening by Design (RHBD) has been shown to be effective in providing hardness to radiation effects [7]. These techniques can be implemented in different levels of abstraction from circuit layout to system design. The generation mechanisms of Single-Event Effects (SEEs) are strongly connected to the physical layout of integrated circuits (ICs), as, for example, the relation between the energy deposition and charge collection in the p-n junctions of transistors. Accordingly, several hardening approaches can be applied at circuit layout level such as the Enclosed Layout Transistor (ELT), guard rings, dummy transistors/gate or Dual Interlocked Storage Cells (DICE) [6-9].

The general goal of each technique is to reduce the charge collection efficiency of a given circuit so the overall Single-Event Transient (SET) pulse can be shortened and/or the collected charge does not exceed the critical charge. For instance, it can be acquired by reducing the sensitive collecting layout area (drain regions) and the parasitic bipolar effect, or even by promoting the pulse quenching effect via charge sharing. However, due to the multi-node collection at deeply scaled technologies, the charge sharing effect might also reduce the efficiency of well-known RHBD schemes such as the DICE designs and Error-Correction Codes (ECCs) due to multiple Single-Event Upset (SEU) and multiple SET occurrences [10]. Some investigation has been done towards the adoption of transistor folding technique as radiation hardening approach [6, 11-13]. Device level simulations and laser testing have shown a reduction on the SET susceptibility of single transistors and inverters [6, 11-13]. However, further study is needed to verify the applicability of this technique to harden a set of standard-cell logic circuits, for instance.

Accordingly, this work proposes the evaluation of the impact of a widely used layout technique, named transistor folding [14], to the SET robustness of basics logic circuits combined with diffusion splitting. The layout technique is adopted in different digital logic gates and its SET susceptibility is evaluated under heavy ions. A layout-based prediction methodology is used to calculate the SET cross-section through Monte Carlo simulations [15, 16]. Further, the in-orbit SET rates are predicted with OMERE package [17] for heavy ions and protons in Low-Earth Orbit (LEO) and International Space Station (ISS) orbits. Proton-induced SET rates are calculated from the heavy ion data using the METIS method [18, 19]. Besides exploiting the transistor folding technique, the novelty of this work also lays on the usage of transistor folding with split in the active area of the transistors on different combinational logic gates to reduce area overhead.

The paper is organized as follows: Section II presents the transistor folding layout technique and the state-of-the-art of RHBD techniques tackling the generation of SET; the sensitivity analysis methodology adopted is described in Section III; the results and discussions on the impact of folded

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transistor in the cross-section of standard cells, the usage of asymmetric layout and voltage variability are provided in Section IV; and, Section V summarizes and concludes this paper.

## II. TRANSISTOR FOLDING LAYOUT TECHNIQUE

Transistor folding is widely used to achieve improved performance and regularity in VLSI circuits [14]. When larger transistors need to be employed, but it exceeds the fixed cell height of a given design, the transistor folding layout technique is used. The folding technique consists in connecting parallel transistors with reduced channel width to achieve a large overall width. Given a transistor with a channel width  $W$ , the same  $W/L$  ratio, thus the same drive strength, can be achieved by connecting  $n$  transistors with width  $W/n$ . Fig. 1 presents the principle of folded transistor layouts in the case of a double-finger transistor. This layout technique divides the drain and source area into smaller partitions depending on the number of fingers. Due to the reduced source and drain areas, the diffusion-to-well capacitance is also reduced.

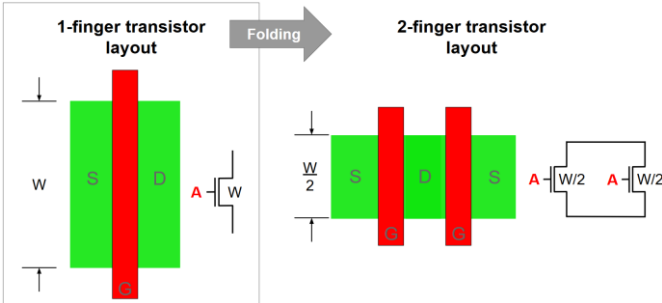


Fig. 1. Transistor Folding Layout technique.

Considering radiation effects, this technique provides a reduced collecting drain area maintaining the same drive strength. The transistor size of folded designs can be calculated following Eq. 1, where  $W_F$  is the width of each folded transistor,  $N_F$  is the number of fingers, and  $W$  is the transistor width in the original design.

$$W_F = \frac{1}{N_F} \times W \quad (1)$$

The transistor folding technique can be adopted along with other hardening techniques such as gate sizing or dummy transistors/gates. The work in [11] was the first to propose transistor folding along with gate sizing to harden a circuit against both SEUs and SETs. A 3D mixed-mode TCAD (Technology Computer-Aided Design) simulation was carried out to analyze the SET pulse characteristics considering alpha particle and heavy ions hit on the center of the drain junctions [11]. Different from the sizing approach, which increases the circuit drive strength at the cost of increased drain area, transistor folding is able to reduce the transistor drain area while keeping the same drive strength. The transistor sizing was able to improve the robustness only for low-energy particles while the transistor folding showed also improvement when considering high-energy particles [11]. In [12], different well structures and layout topologies were studied to evaluate the Propagation Induced Pulse Broadening (PIPB) effect in inverter chains. Accordingly, a double-finger inverter chain was

compared against a single-finger inverter chain. In agreement with [11], the heavy ion results show a reduction on the overall SET pulse width, but minimum influence in the PIPB effect. Inverter chains hardened with guard rings were also evaluated using single and double-finger layout configurations with laser irradiation in [6]. Again, results showed an insignificant pulse-broadening factor for the folded inverter chain, however, a wider SET pulse width average was observed [6]. The authors attributed this to the larger spacing between the drain junctions and the guard rings in the folded design, which limits the charge collection reduction provided by the guard rings. Most of the studies have provided analysis for chains of inverters, and mainly for 2-finger layout configurations. In this work, the transistor folding is adopted on an inverter, NAND and NOR gates, and analyzed through layout-based predictive Monte Carlo simulations. Furthermore, the analysis of diffusion splitting along with transistor folding is provided to overcome the area overhead of multiple-finger designs.

## III. METHODOLOGY

The target circuit layouts were designed following a commercial Process Design Kit (PDK) in a bulk 65-nm technology. Additionally, all designs are compatible with a standard-cell library. Minimum width, spacing and alignment/symmetry of each layer is carefully addressed to provide compatibility among the standard cells. The cell height is set to 13 tracks of metal pitch, i.e. 2.6  $\mu\text{m}$  high. To provide flexibility in cell routing, the metal 1 (M1) is primarily used for the intra-cell connections, except for some cases in which metal 2 (M2) is used horizontally. The PMOS transistor width is 760 nm while the NMOS transistor width is 540 nm. To analyze exclusively the impact of the folded layouts, the equivalent transistor sizing was kept the same for all cases. After all circuit designs are DRC (Design Rule Check) clean, LVS (Layout Versus Schematic) checked and logic and electrical characterization is performed, the collecting drain area information can be extracted from the GDS (Graphical Design System) format file and submitted to the MC-Oracle tool [15]. The proposed layout-based predictive simulation chain is divided into two steps: first, particle interaction simulations are performed using the Monte Carlo simulation tool, MC-Oracle [15][20], to calculate and generate an SET database containing all transient currents; second, SPICE electrical simulations are performed to account for the circuit response effects [16, 21-23]. All circuits were driving a fan-out 1 (FO1), i.e. an inverter was coupled to its output signal. Only the SET pulses with peak voltage higher than 0.6 V (half the supply voltage) are considered for the cross-section calculation. In addition to the double-finger designs (Fig. 1), quadruple-finger layout configurations are also considered in this work (Fig. 2). However, one of the drawbacks of increasing the number of fingers in the folding technique is the increase in layout area. Thus, to overcome the area increase, a Diffusion Splitting (DS) layout technique is proposed and shown in Fig. 2. Instead of using a single strip of active diffusion, a 2-row stacked diffusion transistor is used. Besides reducing the area overhead of the folding technique, DS improves the metal connection routability maintaining the same  $W/L$  ratio and the number of gate fingers. To deepen this analysis, the impact on the in-orbit

SET rates for heavy ions and protons and the effect of voltage fluctuation are also presented.

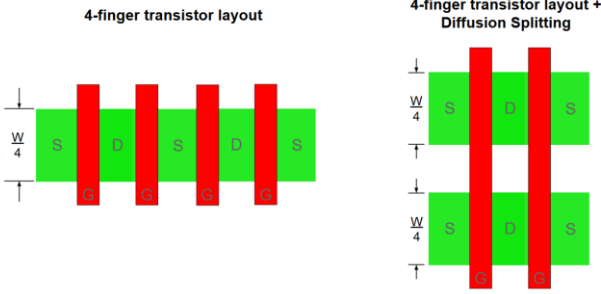


Fig. 2. Standard quadruple-finger folded transistor layout vs. folded transistor layout with Diffusion Splitting (DS) technique in which the diffusion strip is split into 2 strips and placed vertically aligned within each other.

#### IV. RESULTS AND DISCUSSION

This work analyzes the applicability of the transistor folding layout technique to be used as an RHBD technique in standard-cell libraries. The layout area information for the original design of the inverter, NAND and NOR gate along with the increase factor for its folded designs is shown in Table I. For the three cells analyzed, the double-finger layout configuration exhibited an area increase of approximately 1.5x the original single-finger layout area.

TABLE I

TOTAL AREA FOR EACH ORIGINAL CELL LAYOUT DESIGN ( $\mu\text{m}^2$ ) AND THE INCREASE FACTOR FOR ITS CORRESPONDENT FOLDED DESIGNS

	Original design ( $\mu\text{m}^2$ )	Folded designs		
		2-finger	4-finger	4-finger with DS
Inverter	1.560	$\sim 1.5x$	$\sim 2.4x$	$\sim 1.5x$
NAND2	2.444	$\sim 1.5x$	$\sim 2.6x$	$\sim 1.5x$
NOR2	2.444	$\sim 1.5x$	$\sim 2.6x$	$\sim 1.5x$

An area increase around 2.5x is expected when using quadruple-finger layout designs. However, if DS is used, the area overhead for the 4-finger designs can be reduced to the same observed in the 2-finger designs, i.e. approximately 1.5x greater than the original designs. Thus, DS provides an area reduction of 36% and 42% for the 4-finger inverter and NAND/NOR cells, respectively.

In Fig. 3, the simplified layout of the NAND designs containing only the metal1, diffusion and poly layers are shown. In standard-cell methodology, a fixed cell height is defined to provide regularity. Thus, as the number of finger is increased, the cell width is increased and, consequently, the cell layout increases. As the transistor sizing is kept the same, the diffusion splitting can be applied to reduce the impact in the layout area, as shown in the Fig. 3.

##### A. Impact on SET cross-section $\sigma_{SET}$

The SET cross-section  $\sigma_{SET}$  for the inverter designs under particle LET of  $78.23 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  is shown in Fig. 4. The folded designs have shown similar  $\sigma_{SET}$  for input 1 and input 0, thus using transistor folding may reduce the SET sensitivity dependence on the input signal in the inverter design at high LET. On average, the folded designs provide lower sensitivity than the original design with the greatest  $\sigma_{SET}$  reduction for the 2-finger layout configuration, approximately 42%. The 4-finger inverter shows improvement solely for the input 1, however, despite the area reduction, DS also reduced the  $\sigma_{SET}$ . To analyze the folding impact for low particle LET irradiation, Fig. 5 presents the SET cross-section for the inverter designs considering heavy ions with  $\text{LET} = 5.43 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . In this case, the greatest  $\sigma_{SET}$  reduction is observed for the 4-finger inverter with DS, about 37%. It can be observed that, for low LET, the  $\sigma_{SET}$  reduces with the increase of the number of fingers  $N_F$ , in agreement with 3D TCAD results obtained in [11]. As  $N_F$  increases, the collecting regions are reduced and sparsely distributed along the layout, then the charge sharing at low LET is limited. Thus, less folded transistors are affected by a single particle hit, leading to an improvement in the efficiency of the technique in reducing the  $\sigma_{SET}$ . Fig. 6 depicts the mean SET

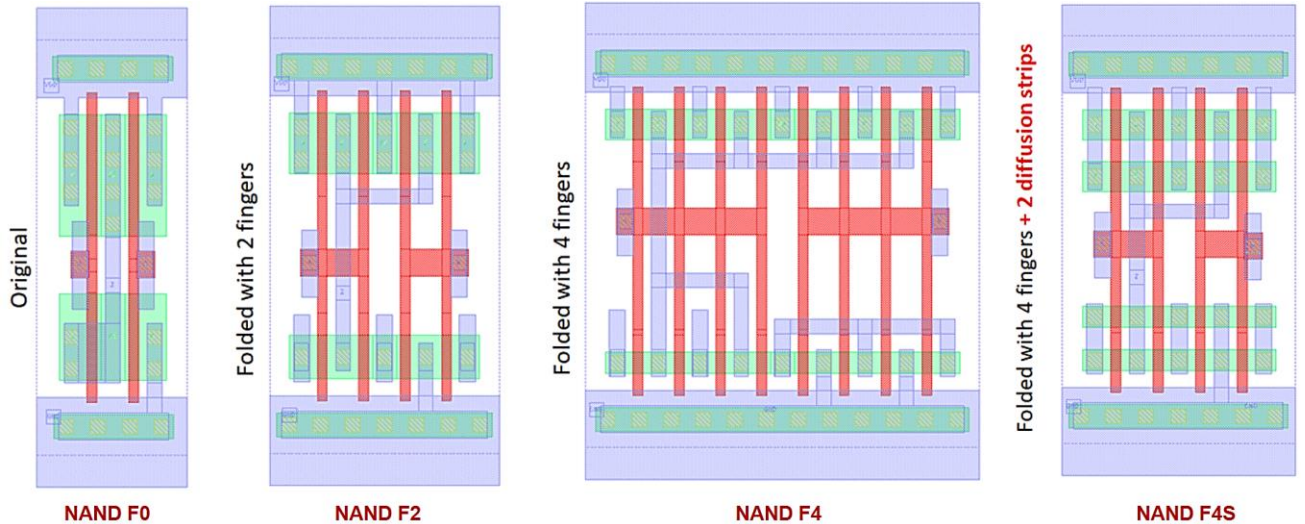


Fig. 3. Simplified layout design of NAND F0 (no folding), NAND F2 (2-finger design), NAND F4 (4-finger design) and NAND F4S (4-finger design with Diffusion Splitting). For clarity, only the metal1, diffusion and poly layers are shown.

cross-section curve for each inverter cell design considering the input 0 and input 1. Besides providing lower SET cross-section, the 4-finger designs (with and without DS) showed a higher threshold LET than the original design. For LET lower than 10 MeV.cm<sup>2</sup>/mg, the 4-finger inverter with DS is preferred, while for higher LET the 2-finger design is more suitable.

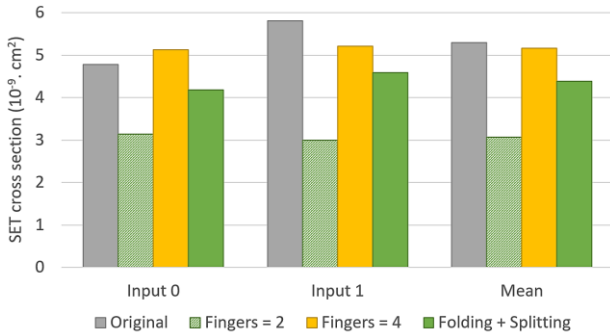


Fig. 4. SET cross section for the inverter designs under LET = 78.23 MeV.cm<sup>2</sup>/mg considering input 0, input 1 and the mean value.

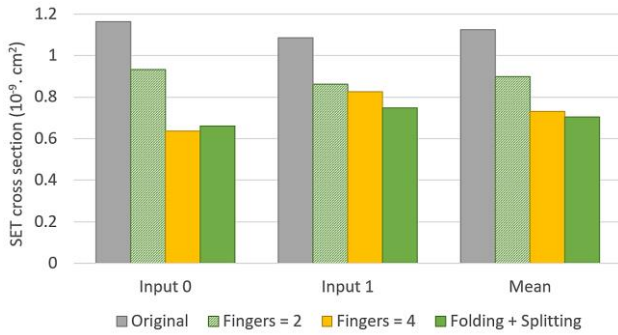


Fig. 5. SET cross section curve for the inverter designs under LET = 5.43 MeV.cm<sup>2</sup>/mg considering input 0, input 1 and the mean value.

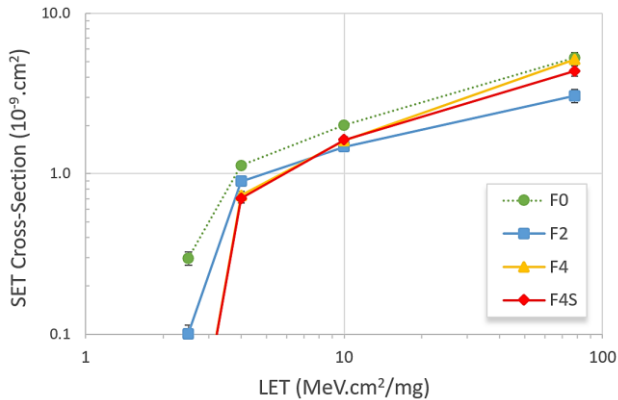


Fig. 6. Log-Log representation of the mean SET cross section curves for the inverter designs. No event was observed in the 4-finger designs (triangle and rhombus curves) for LET lower than 5.43 MeV.cm<sup>2</sup>/mg

Considering the NAND designs, Fig. 7 presents the SET cross-section  $\sigma_{SET}$  under 78.23 MeV.cm<sup>2</sup>/mg. Except for the 2-finger design, the folded designs provided a higher mean  $\sigma_{SET}$ . At high LET, the hardening efficiency of folded transistors is limited due to the complex input dependence observed on the cross-section. The folded NAND designs show a stronger input dependence than the original design, leading to a similar or lower  $\sigma_{SET}$  only for inputs (0, 0) and (0, 1). The worst-case input scenario for NAND gates is the input (1, 1), and, in this case, transistor folding exacerbates the SET sensitivity up to

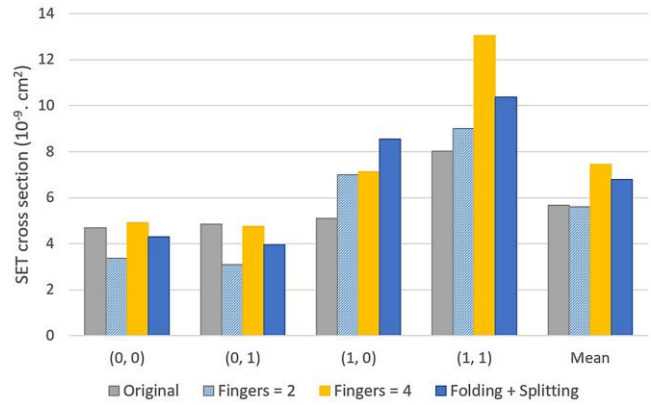


Fig. 7. SET cross section for the NAND designs at LET = 78.23 MeV.cm<sup>2</sup>/mg for each input signal and the mean value.

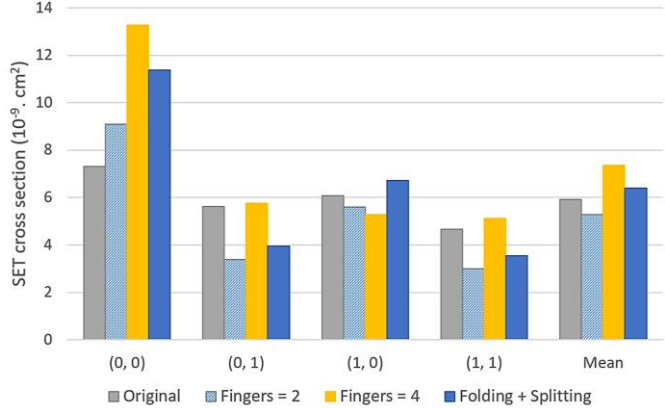


Fig. 8. SET cross section for the NOR designs at LET = 78.23 MeV.cm<sup>2</sup>/mg for each input signal and the mean value.

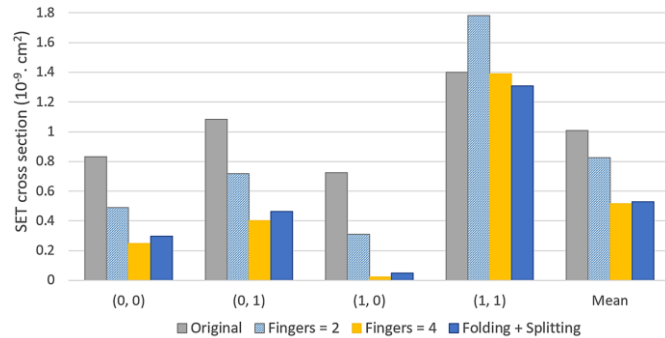


Fig. 9. SET cross section for the NAND designs at LET = 5.43 MeV.cm<sup>2</sup>/mg for each input signal and the mean value.

approximately 62% in the 4-finger design. For input (1, 1), all PMOS devices are sensitive to a particle hit, besides the lower restoring capability of NMOS devices, PMOS transistors collect more charge due to its larger drain area [22]. Similarly, in the NOR case, the input (0, 0) is the worst-case input scenario and it shows increased  $\sigma_{SET}$  when adopting folded transistors as shown in Fig. 8. This behavior is also observed for low LET as depicted in Fig. 9. To reduce the increased sensitivity at the worst-case input scenarios, transistor folding can be applied only in the pull-down (or pull-up) network to balance the overall SET sensitivity. The asymmetric designs are also considered in this work and discussed in the next subsections. Considering LET = 5.43 MeV.cm<sup>2</sup>/mg in the NAND design shown in Fig. 9, the 4-finger design showed the lowest  $\sigma_{SET}$ , and similar sensitivity is obtained with DS. Thus, it is important to note that, for low LET, increasing the  $N_F$  improves the overall

SET cross-section  $\sigma_{\text{SET}}$  as observed for the inverter design. This behavior can be seen in the SET cross-section curves in Fig. 10 and Fig. 11, for the NAND and NOR designs, respectively. At 10 MeV.cm<sup>2</sup>/mg, the folded designs provide similar cross-section than the original one. Except for the 2-finger NAND, all other folded designs provided a higher threshold LET than the original design. For LET lower than 10 MeV.cm<sup>2</sup>/mg, the 4-finger design with DS is preferred for both NAND and NOR. To summarize the impact of folded designs under the effects of low LET particles, Table II contains the SET cross-sections for particle LET equals to 5 MeV.cm<sup>2</sup>/mg.

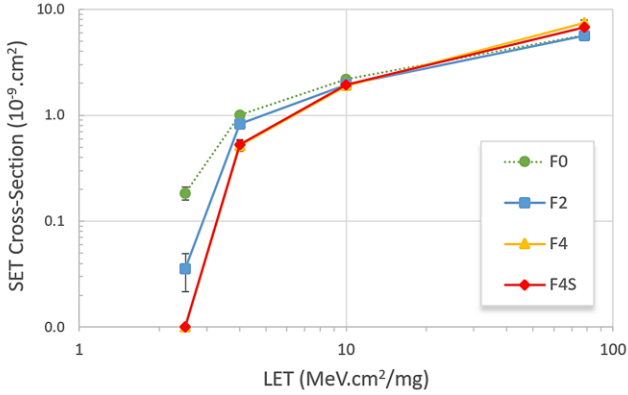


Fig. 10. Log-log representation of the mean SET cross section curves for the NAND designs. No event was observed in the 4-finger designs (triangle and rhombus curves) for LET lower than 5.43 MeV.cm<sup>2</sup>/mg

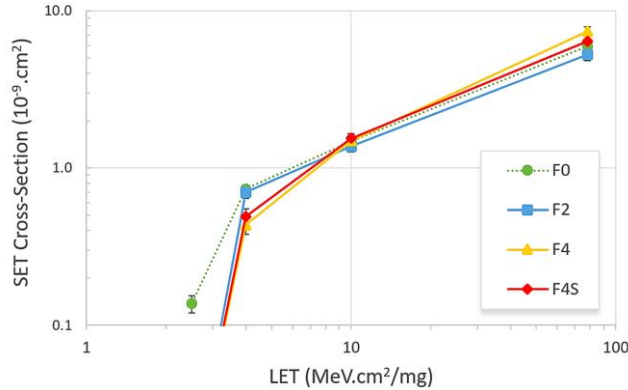


Fig. 11. Log-log representation of the mean SET cross section curves for the NOR designs. No event was observed in the folded designs for LET lower than 5.43 MeV.cm<sup>2</sup>/mg

TABLE II  
SET CROSS-SECTION FOR EACH ORIGINAL CELL LAYOUT DESIGN (10<sup>-9</sup>.cm<sup>2</sup>)  
FOR PARTICLE LET = 5 MeV.cm<sup>2</sup>/MG AND THE DECREASE PERCENTAGE  
FOR ITS CORRESPONDENT FOLDED DESIGNS

	Original design	Folded designs		
		2-finger	4-finger	4-finger with DS
Inverter	1.124	-20%	-35%	<b>-37%</b>
NAND2	1.010	-18%	<b>-49%</b>	-48%
NOR2	0.736	-5%	<b>-41%</b>	-33%

## B. Asymmetric designs

As observed in the last subsection, transistor folding can induce a higher SET cross-section for the worst-case input scenario of the NAND and NOR circuits. Fig. 12 provides the transistor network of the NAND gate and its truth table. For the worst-case scenario, highlighted in red, the *off* transistors, which are sensitive to particle hits, are issued from the pull-up network, i.e. PMOS devices. The folding technique has been equally applied to both pull-up and pull-down networks. To study the impact of asymmetric designs, the 2-finger design and the 4-finger design with DS are explored considering the transistor folding only in one of the networks.

The folding technique was applied only in the NMOS devices for the NAND gate, and only in the PMOS devices for the NOR gate. The SET cross-sections are shown in Fig. 13 for each design considering only the worst-case input scenario, i.e. the input combination (1, 1) and (0, 0) for the NAND and NOR, respectively. The number indicates the fingers, N/P indicates when only NMOS/PMOS devices are folded, and S indicates when diffusion splitting is adopted. For instance, the F4NS circuit is the 4-finger design with only NMOS devices folded and with diffusion splitting. This nomenclature is used in the remaining of the manuscript for the sake of compactness. For the LET = 78.23 MeV.cm<sup>2</sup>/mg, the greatest reduction on cross-section was observed for the 4-finger designs. The NAND F4NS circuit provides a reduction of 26.5%, while the NOR F4PS circuit reduces the cross-section in approximately 29.7%.

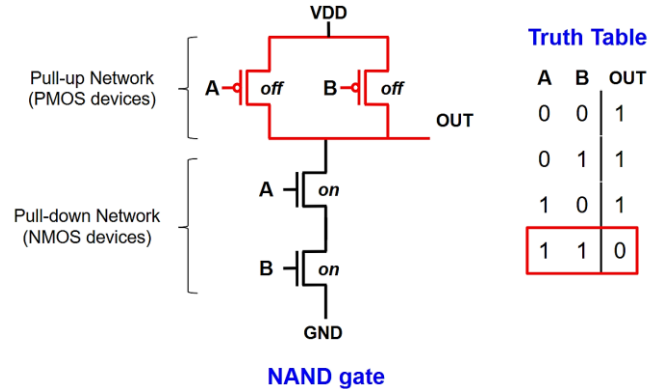


Fig. 12. Transistor network of an NAND gate and its truth table. *On*-state and *off*-state are indicated for the transistors considering the worst-case input scenario, i.e. input (1, 1).

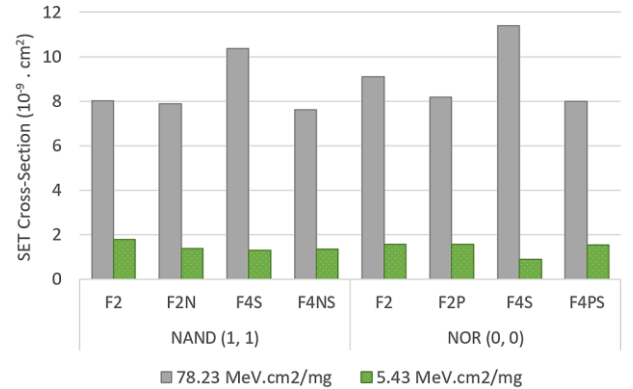


Fig. 13. SET cross-section for symmetric and asymmetric designs of 2-finger and 4-finger with diffusion splitting of NAND and NOR gates in the worst-case input scenario, i.e. input (1, 1) and input (0, 0), respectively.

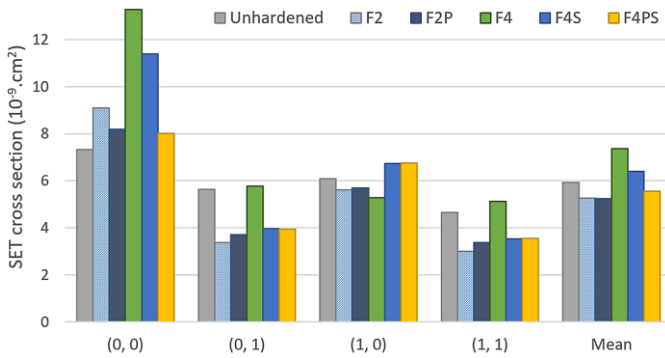


Fig. 14. SET cross section for the NOR designs at LET = 78.23 MeV.cm<sup>2</sup>/mg for each input signal and the mean value.

However, the asymmetric circuits are less effective when considering low LET particles as also shown in Fig. 13. Also, when adopting the asymmetric designs, not only the worst-case input SET cross-section is affected as can be seen in Fig. 14 in which the SET cross-section  $\sigma_{\text{SET}}$  for each input signal and the mean value are shown for the NOR gate. Due to a small increase in the cross-section for the inputs (0, 1), (1,0) and (1, 1), the mean SET cross-section reduction for the F2P and F4PS circuits are 1% and 13%, respectively. These results reaffirm the importance of considering input dependence when hardening digital logic circuits. The impact of adopting asymmetric designs is also evaluated under voltage variability and analyzed on the in-orbit SET rates.

### C. Voltage Fluctuation

In addition to radiation effects, electronic circuits are susceptible to dynamic environmental variability, such as voltage fluctuations due to voltage drop and current derivative  $di/dt$  noise [24]. Previous works have shown that voltage variability reduces the reliability of circuits, especially when considering harsh environments under radiation effects [25,

26]. In [25], voltage variability has shown to reduce the threshold LET of different XOR topologies in FinFET and Trigate devices. Also, a reduction in the electrical masking capability of the gates and increase in the SET pulse width is observed in [26]. The IR drops due to the parasitic resistance of the power grids can lead to  $\pm 10\%$  variation on the supply voltage. Accordingly, all circuits were analyzed considering a voltage drop of -10% of the nominal supply voltage of the technology, i.e. 0.12V. The SET cross-section and the variation  $\Delta\sigma_{\text{SET}}$  (in %) are shown for each circuit in Fig. 15. As expected, a reduction on the supply voltage of the circuits reduces the driving capability and consequently reduces the recovery efficiency, leading to a higher  $\sigma_{\text{SET}}$ . The usage of diffusion splitting technique induces insignificant impact on the circuit robustness to voltage variability as similar SET cross sections are obtained for the F4 and F4S circuits. However, for the 3 logic gates (inverter, NAND and NOR), the F4 and F4S circuits showed the greatest  $\sigma_{\text{SET}}$  increase, ranging from 50% to 70%. Thus, as the number of fingers is increased, the circuit becomes more sensitive to the voltage drops. However, the asymmetric designs have shown to reduce the impact of voltage variability on the SET cross sections.

Considering only the inverter designs, the F4S circuit shows the lowest  $\sigma_{\text{SET}}$  at nominal voltage but it is the most sensitive to voltage drops, along with the F4 circuit. On the other hand, the F2 circuit provides the lowest  $\sigma_{\text{SET}}$  at -10% of the supply voltage, and also the lowest variation on  $\sigma_{\text{SET}}$ .

For the NAND gate, the F4 circuit provides the lowest  $\sigma_{\text{SET}}$  at nominal voltage, but it increases up to 66% with 10% reduction on the supply voltage. In this case, the unhardened circuit is the least sensitive design to voltage variation, leading to approximately 24% of increase in the  $\sigma_{\text{SET}}$ . However, under voltage drop, the lowest  $\sigma_{\text{SET}}$  is still observed for the asymmetric design F4NS circuit. Compared to the unhardened

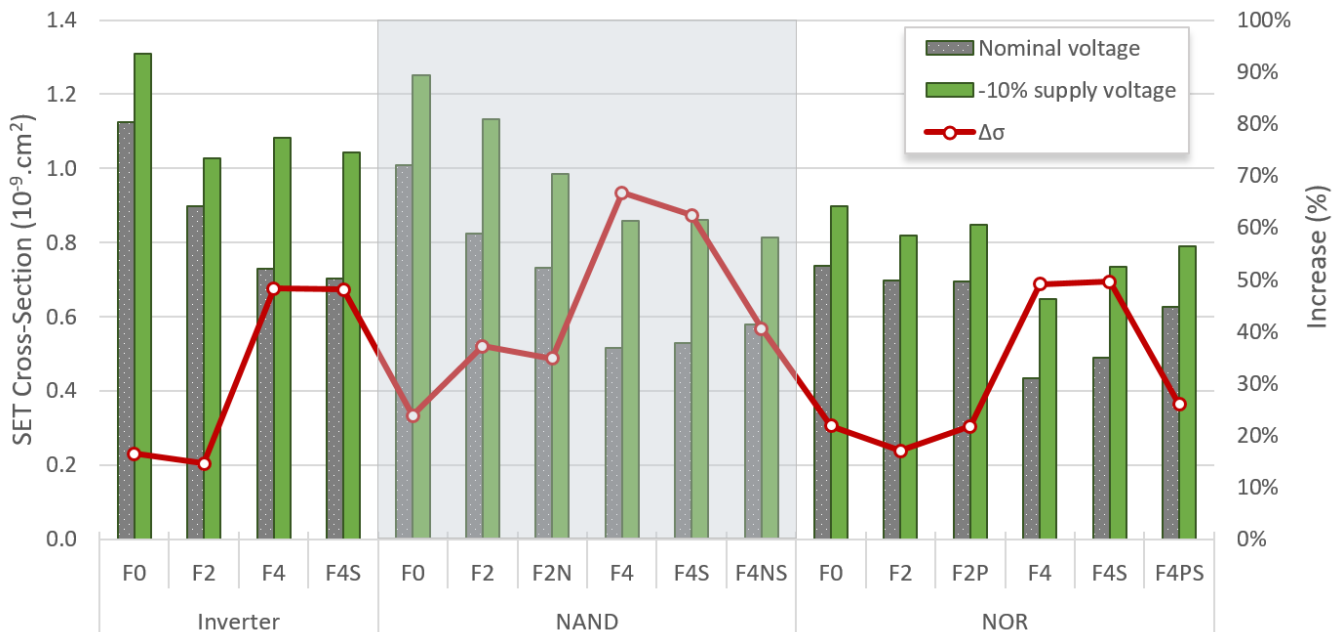


Fig. 15. SET cross section considering a voltage drop of 10% over the nominal supply voltage and a particle LET of 5 MeV.cm<sup>2</sup>/mg. The percentage increase  $\Delta\sigma_{\text{SET}}$  in the cross section is also shown in red line.

NAND circuit, when the voltage fluctuation is considered, the F4NS reduced the  $\sigma_{\text{SET}}$  up to 35%.

For the NOR gate, similarly to the NAND gate, the F4 circuit provides the lowest  $\sigma_{\text{SET}}$  at nominal voltage, but high sensitivity to the voltage drops, resulting in approximately 49% increase in the  $\sigma_{\text{SET}}$ . However, it still provides the lowest  $\sigma_{\text{SET}}$  during voltage fluctuation. The diffusion splitting used in F4S increased its cross-section, but it still provides a lower  $\sigma_{\text{SET}}$  than the F2 circuit, with the same area overhead.

#### D. Prediction of in-orbit SET rates

Based on the SET cross-section curves calculated with the current database provided by MC-Oracle, the in-orbit SET rates were estimated for the Low-Earth Orbit (LEO) and International Space Station (ISS) orbits with the OMERE software. OMERE is a tool dedicated to the analysis of space environment and radiation effects on electronics developed by TRAD and CNES [17]. The Integral Rectangular Parallelepiped (IRPP) approach is used to predict the SET rate, i.e. it is calculated by the convolution of the heavy-ion cross section data with the particle flux in the aforementioned orbits. This approach is a standard method specified by the European Cooperation for Space Standardization (ECSS) [27]. The NASA AP8MIN trapped radiation model is used for the proton fluxes under solar minimum conditions [28]. For the Galactic Cosmic Rays (GCR) fluxes, the international standard ISO 15390 model is used [29]. A fixed shielding of 1 g/cm<sup>2</sup> is considered. The calculated heavy-ions SET rates are shown in Fig. 16. Firstly, it can be noticed that all folded designs exhibit lower rates than its unhardened version (F0 circuit) for both orbits. In the case of the inverter, the F4S circuit provides the lowest rate with a reduction of approximately 82% and 77% in the ISS and LEO orbit, respectively. Similarly, for the NOR gate, the F4S showed the lowest SET rate. The folded transistor and diffusion splitting provided about 66% and 55% of reduction on the SET rate for the ISS and LEO orbit, respectively.

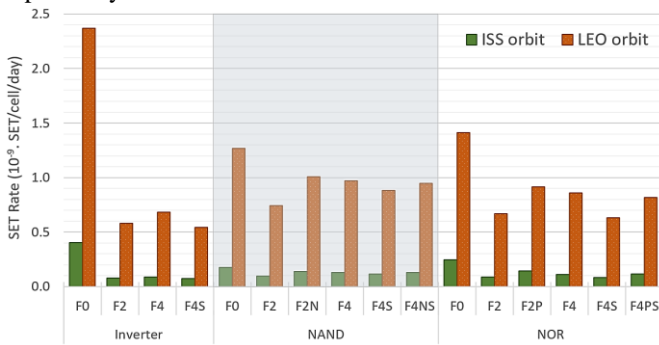


Fig. 16. Heavy-ions SET rate estimated with OMERE [17] for each circuit and its hardened version considering the LEO (800km, 98°) and ISS (400km, 51.64°) orbit. The SET cross section average of each input signal is used.

On the other hand, the F2 circuit is expected to have a lower rate for the NAND gate. Although the cross-section calculations were performed for heavy ions, the protons are expected to dominate the SEE rates in the LEO and ISS orbits. Due to its improved accuracy when compared to analytical models, the METIS method [18, 30, 31] was used to predict the proton-induced SET cross section curves from the heavy ions data. The sum of the SET rate induced by heavy ions and protons are

shown in Fig. 17. As expected, the overall SET rate increased considerably. However, in this case, the F4 and F4S circuits are no longer the most hardened designs. The F2 circuits have shown the lowest rate for the inverter and NAND gate, for both orbits. For the NOR gate, the asymmetric design F2P provided the lowest rate, about 10% reduction for the two orbits. Except for the F2N, one can notice that whenever the asymmetric design approach is adopted, a reduction on the overall SET rate is observed.

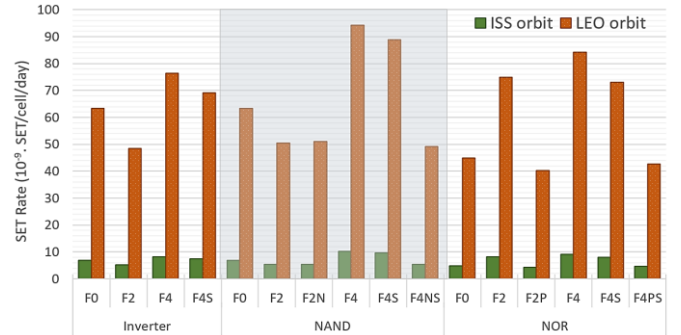


Fig. 17. Total SET rate estimated with OMERE [17] for each circuit and its hardened version for the LEO (800km, 98°) and ISS (400km, 51.64°) orbit considering heavy ions and protons. Proton-induced SET rates are estimated with the METIS method [18, 19]. The SET cross section average of each input signal is used.

#### E. Transistor Scaling and Angular Dependence

With the increasing demand of better performance and low power in critical systems, advanced technology nodes have been studied to be employed in future missions. Due to the scaling of transistors, the hardening efficiency of these techniques might be reduced as the charge sharing effects are increased in response to the close proximity of the collecting zones in the advanced technology nodes. However, in FinFET technologies, the three-dimensional structure of the transistor impacts on the charge collection process and a reduction on the charge sharing effects might be expected as shown in [32]. Further, if an SOI technology is adopted, the hardening efficiency would be highly improved due to the lack of the diffusion contribution in the charge collection [33].

Concerning the angular effect in the charge collection, folded transistors have shown a low angle dependence as investigated in [34]. In fact, only the NMOS transistors have shown an increase in the total collected charge. For the worst-case scenario, in which the particle strikes the center of the drain area with a tilt angle of 60°, the total collected charge of a 4-finger NMOS transistor can be 20% higher than the collected charge in original design, without transistor folding. Thus, a very weak angle dependence can be expected in the SET cross-section of the folded designs, especially for low LET due to the reduced charge sharing. Further, according to [35], deeply scaled CMOS technologies present a marginal difference on the overall charge sharing effect between normal and angled strikes.

## V. CONCLUSIONS

Physical layout design influences the main SEE mechanisms in VLSI circuits. Accordingly, RHBD techniques can be adopted at layout level. This work has analyzed the efficiency of transistor folding layout in improving the SET immunity of



digital circuits. In addition to the higher threshold LET, the results show that folded designs can provide lower SET cross-section, especially at low LET. The number of fingers were also explored. For LET lower than 10 MeV.cm<sup>2</sup>/mg, the hardening efficiency of the folded designs increases as the number of fingers is increased. However, at high LET, the 2-finger designs showed the best performances. Increasing the number of fingers increases greatly the final layout area. Thus, a layout technique was proposed to overcome the area overhead of multiple-finger designs. In the diffusion splitting approach, the active diffusion is split into two strips and placed vertically aligned within each other. Besides reducing the layout area, diffusion splitting may also improve the SET cross-section depending on the circuit topology, input signal and ion LET. Due to the strong input dependence of these techniques, it was also proposed to adopt asymmetric designs, i.e. applying the hardening techniques only in the PMOS or NMOS devices, depending on the worst-case input scenario of the logic gate. Voltage variability was also explored due to its impact on the reliability of deeply scaled technologies. The folded designs have shown a higher sensitivity to voltage fluctuation. However, the usage of asymmetric design showed to reduce it. And, lastly, the in-orbit SET rates were predicted for the LEO and ISS orbits. When the SET rate is only calculated for heavy ions, all the folded designs provided lower rate than the unfolded designs. However, the protons dominate the SEE rates in the LEO and ISS orbits. When protons are taken into account, the 2-finger designs (symmetric and asymmetric) and the asymmetric 4-finger design with DS are the most hardened circuits.

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