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# Multi-Level Multiplexed Power Converter Topology for 1500V Applications

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*Abstract*—This paper presents a DC-AC multi-level converter topology that is well adapted for high voltage conversion ratio and will be used to transfer power between a 1500V DC source and 400V/480V AC load or grid. This topology is intended for 1500V Applications. The main potential applications are Uninterruptible Power Supply (UPS), Solar Photovoltaic (PV) Systems and Energy Storage Systems (ESS). The proposed converter topology achieves very high efficiency, up to 98,7% in single conversion architecture using only low-cost silicon (Si) devices with a low blocking voltage.

*Index Terms*—Multilevel converter, Multiplexed topology, Uninterruptible Power Supply, Solar PV systems, ESS,

## I. INTRODUCTION

Over the last decade, there has been an increase in the installed capacity of utility scale solar PV and datacenter plants, and ESS is often strictly required to level the power delivered by high power PV plants. In these fields a power of several megawatts becomes quite standard and the power of some facilities even exceeds one hundred megawatts. This increase in power has also led to the increase of the DC bus voltage up to 1500V.

The choice of the 1500V standard voltage is mainly linked to economic gain. Although the length of PV panels and/or battery strings is longer than conventional installations, it allows saving on wiring, connections and combiner boxes, and reduces the number of inverter stations to be installed. This choice also increases the efficiency of the system, directly impacting the net profit of the operating company: ohmic losses in DC conductors are reduced and allow using cables with a smaller cross-section and moreover the risk of system failure is lower which is translated into better overall reliability associated with reduced downtime because less DC components (wiring, connections, boxes, etc.). That said, 1500V is expected to be the next voltage class, which will reduce the total cost of PV and UPS systems on a large commercial and utility scale. These savings translate into a significant advantage that drives the growth of the 1500 V market; several GW/year and several MW/year are respectively expected in the PV and the UPS markets.

This new mainstream forces power converter manufacturers to redesign converter topologies with the aim of keeping the same levels of efficiency, cost and volume. From the introduction of the first well known multi-level topologies [1– 3] to their industrial maturity, many applications have taken advantage of their improved performances [4–6].

Even if many industrial applications have been able to adopt these multi-level converter topologies, the transition to the 1500V standard is still a big challenge. Most manufacturers still choose to use traditional three-phase topologies such as classic 2L-VSI or multi-level topologies with 3 to 5 levels maximum. To meet the requirements of 1500V systems, topologies with a low number of output voltage levels require high blocking voltage semiconductor devices and topologies with a high number of output voltage levels, require a large number of low blocking voltage semiconductor devices, leading to high system cost. In addition, to achieve a high DC bus voltage, it may be necessary to serialize several switches and capacitors. The main challenge of these applications is to maintain a high efficiency at high voltage conversion ratio. This requirement is even stronger for UPS that need double conversion and for which losses are an extra cost for the user.

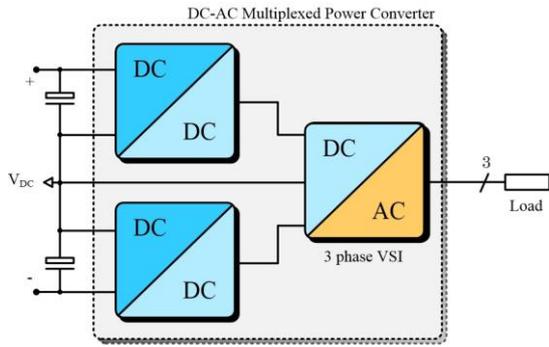


Fig. 1: Proposed Multi-Level Semi-Multiplexed DC-AC Power Converter Architecture.

In order to overcome the limitations and constraints of standard topologies at high voltage conversion ratio, some new proposals have been done. In [7], it is proposed to share flying capacitors per each phase leg as a solution to high number of devices and high input voltage. However, each leg is generating almost the full amplitude of output voltage leading to high power switching losses. In [8], with the introduction of Multiplexed choppers family concept, authors want to optimize the overall number of devices and efficiency by means of multiplexing the voltage generated by each stage. Nevertheless, extra balancing circuit is needed for regulating the dc bus points, leading to a bulky final solution. In [9] another topology with reduced number of switches is introduced but switches with a high voltage rating are required and the control is quite complex. Other recent developments in the field [10, 11] show similar approach in the idea of reducing the common mode voltage but at the expense of higher cost and higher losses due to the need of bus balancer.

This paper proposes a new multilevel Multiplexed converter topology family [17] especially intended for high-power UPS, Solar PV systems and ESS applications, which achieves very high efficiency, up to 98,7% in single conversion architecture using only low-cost silicon (Si) low blocking voltage semiconductor devices.

The structure and conversion stage topologies of this MultiLevel Multiplexed topology will be described in Section. II. The control strategy for the proposed topology is the described in Section. III, starting with the basic principle and then describing more in depth chopper and inverter modulation. Simulation results are presented in Section. IV. Finally, the conclusions are given in Section. V.

## II. NEW MULTIPLEXED CONVERTER TOPOLOGY

### A. Power Converter Structure

The proposed power conversion architecture (introduced by *Schneider Electric*) is shown in Fig. 1 and it is composed of three parts: The input voltage source (PV strings, battery strings or conventional dc bus voltage made of capacitor banks as in typical back-to-back conversion systems), the two symmetric DC-DC Step-Down chopper stage and three phase DC-AC output inverter.

The main feature of the architecture is to supply the output three-phase DC-AC voltage inverter stage via two DCDC Step-Down chopper stage without any filtering elements between both stages. Thus, the inverter is directly cascaded by Top side (Top) and Bottom side (Bot) choppers and it plays the role of a multiplexer, hence the name of "Multiplexed Converter" (i.e. "xPlexed"). The proposed architecture can be considered as an entire single AC-DC (active rectifier) or DCAC (inverter) conversion stage. Depending on the application, several conversion configurations are possible. In this way, more than one conversion stage can be combined.

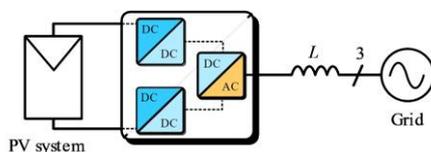


Fig. 2: Solar PV system or ESS application conversion architecture using xPlexed topology

For Solar PV system and ESS applications, a single conversion stage is needed (see Fig. 2), to connect the grid to a 1500V PV panel strings or battery pack system. For UPS application two conversion stages are required (see Fig. 3); a grid side rectifier or AFE (Active Front End) and inverter are connected in back-to-back configuration. A battery pack system can be connected via a DC-DC converter or even directly to the dc bus.

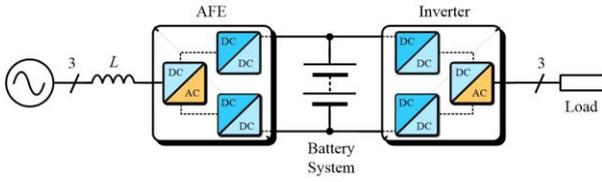


Fig. 3: UPS application conversion architecture using *xPlexed* topology

### B. Converter Stage Topologies

In principle, the DC-DC chopper and DC-AC inverter can be any converter with two or more voltage levels. However, for a DC bus at 1500V we will consider different combinations of multi-level topology from 3 to  $n$  levels, where  $n$  is the number of voltage levels at the output of each converter. Fig. 4 shows the power circuit of the three-phase 5-level Multiplexed DC-AC inverter with 3-level Flying Capacitor chopper and 3L-TNPC inverter configuration. In this paper we will mainly focus on this configuration.

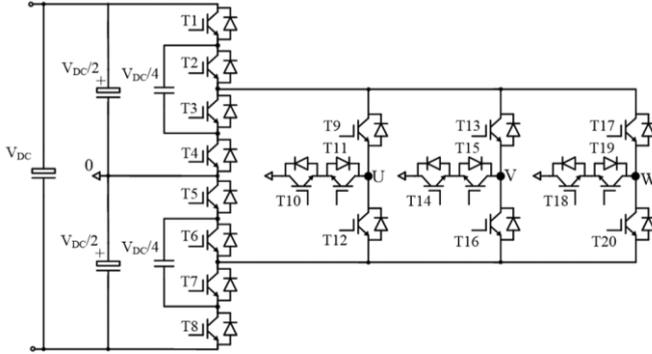


Fig. 4: Proposed 5-level Multiplexed DC-AC Inverter with 3-level-Flying Capacitor Chopper topology and 3-level-T type NPC Inverter topology

The output voltage levels depend mainly on the number of levels of the chopper and inverter stage. Moreover, for a given topology for both the DC-DC chopper stage and the DC-AC inverter stage the output voltage levels will depend on the amplitude of the output voltage. In this way, for a Multiplexed topology consisting of 3-level chopper and inverter stages, under rated conditions, it is possible to obtain a five-level output voltage waveform at the output terminals of the converter.

### C. Semiconductor selection

One of the main features being efficiency and low cost, the selection of semiconductors becomes essential. Only silicon components are used in order to reduce the total cost to the maximum but of course wide band gap components could be used to reduce losses and so improve efficiency.

TABLE I: Specifications and characteristics of the Multiplexed Converter.

Parameter	Symbol	Value
Nominal Power DC bus voltage	$P_N$	50 kW
Load voltage	$V_{DC}$	900-1500 V
Output frequency	$V_{Load}$	400V-480 V
	$f_{Load}$	50-60 Hz
Chopper switching frequency	$f_{Chop} f_{Sw}$	8 kHz
Inverter switching frequency		16 kHz
Flying Capacitor	$C_{fly}$	150 $\mu$ F
Load Filter inductance	$L_f$	200 $\mu$ H
Load Filter capacitance	$C_f$	50 $\mu$ F

The first originality of this topology is that the choppers deliver square voltage waveforms with steps of one fourth of the DC bus; assuming that an appropriate control pattern is used, the voltage applied to the inverter switches may thus be limited to 3/4 or even 1/2 the DC bus voltage, which of course helps maintaining a high efficiency. In our case, the inverter is realized with 1200V, 75A High Speed IGBTs *IKY75N120CS6* from Infineon. The typical voltage across the semiconductors of the flying capacitor chopper is 1/4 of the DC bus voltage, and 650V, 75A Low- $V_{CE,sat}$  IGBTs *IKZ75N65ES5* from Infineon have been selected

here. In order to handle the high current of the load and to reduce the conduction losses, each switch consists of four devices in parallel.

### III. CONTROL STRATEGY FOR XPLEXED ARCHITECTURE

#### A. Basic principle

Unlike conventional three-phase topologies, the multiplexed topology does not have independent phase legs. Therefore each conversion stage module must be controlled separately. As a basic principle of modulation, sinusoidal modulation can be used to make it simple.

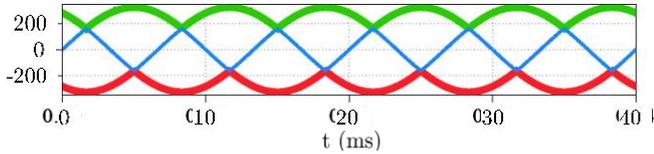


Fig. 5: Voltage reference signals for chopper and inverter stage. green: Top chopper; blue: Inverter; red: Bot chopper

The main concept (see Fig. 5) is to generate the highest (in green) and the lowest (in red) part of the reference AC waveforms directly by the corresponding Top and Bot choppers so that at least two phases of the inverter can be saturated, the one connected to the phase with the highest voltage reference being saturated to a 100% duty cycle, the one connected to the phase with the lowest voltage reference saturated with a 0% duty cycle. Only the inverter leg connected to the phase with the intermediate voltage reference needs to switch to follow the sinusoidal middle reference (in blue). So, at any given moment there is only one inverter arm switching.

#### B. Chopper Modulation

Regarding the control of DC-DC choppers, the main objective is to generate the highest and lowest side of the reference voltage. The chopper section involving capacitors has a strong requirement to ensure that the average current is zero and that the voltage of this capacitor can be regulated. Another objective will be to minimize the static voltage seen by the inverter stage in order to respect the voltage rating of the inverter switches. As a first approach, self balancing mechanism can be tried by applying a carrier based PWM modulation scheme such as Phase Shifted (PS) [12]. Another possibility is to use Phase Disposition (PD) by means of state machines like in [13] and [14], but in this kind of schemes extra commutations are needed and the balancing of flying capacitor could become complex. We therefore use PS sawtooth carriers (cf. Fig. 6). Sawtooth type carriers at 8kHz switching frequency are used for having the absolute control of turn-on and turn off moments, or rising-up and falling-down instants of the voltage created by each chopper.

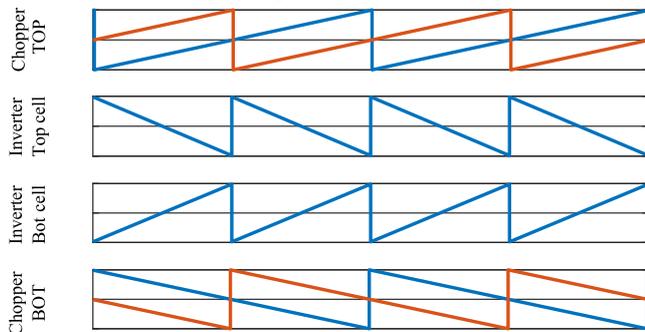


Fig. 6: Phase Shifted (PS) PWM carrier configuration for Top and Bot choppers (8kHz) and Inverter stage (16kHz)

Rising sawtooth carriers for the Top chopper and falling sawtooth carriers for the BOT chopper have been selected. In order to minimize the static voltage seen by the inverter stage over the majority operating points, there will be a relative phase shift of some switching periods between the Top and Bot choppers carrier signals. In this way when high modulation index is required, consecutive steps of voltage levels on the differential voltage of the chopper outputs can be avoided. The feature of the Flying Capacitor converter to double the apparent frequency at the output leads to a chopper switching frequency equal to half that of the inverter. Consequently, the switching losses are reduced too. This switching frequency ratio between chopper and inverter must be respected if the calculation of the inverter duty cycle (explained in the next section) is to be accurate.

### C. Inverter Modulation

The voltage generated at the output of the inverter must be synthesized by means of the voltage already switched by choppers. Hence, duty cycle for inverter is defined in function of choppers duty cycles and inverter voltage reference. For that, duty cycles of each output inverter arm are determined separately by means of two-dimensional look-up-tables using a pre-calculated PWM method. Contrary to the disadvantages of this type of techniques [15, 16], in this case, the computational cost of the algorithm is not high and duty cycles can be calculated with a high accuracy. The calculation of duty cycles is made off-line throughout two piecewise interpolations. For that, first of all, in Eq. 1 a virtual inverter average voltage

$\bar{V}_{m(i)}$  is calculated using a default chopper duty cycle array

$\alpha'_{c(i)}$  and its associated chopper output mean voltage  $V_{c(i)}$  as well as a default inverter duty cycle array  $\alpha_{m(j)}$  for  $\forall i, j \in [1, n]$  with  $n$  being the length of the array.

$$\bar{V}_{m(i)} = \bar{V}_{c(i)} + \left[ \frac{\bar{V}_{c(i+1)} - \bar{V}_{c(i)}}{\alpha'_{c(i+1)} - \alpha'_{c(i)}} \right] (\alpha_{m(i)} - \alpha'_{c(i)}) \quad (1)$$

This virtual inverter average voltage is the result of what is obtained at the output of inverter for a given duty cycle. The final duty cycle  $\alpha^0_m$  is calculated in Eq. 2 using the default stored array values and previously calculated inverter duty cycle values.

$$\alpha'_{m(i,j)} = \alpha_{m(j)} + \left[ \frac{\alpha_{m(j+1)} - \alpha_{m(j)}}{\bar{V}_{m(j+1)} - \bar{V}_{m(j)}} \right] (\bar{V}'_{m(j)} - \bar{V}_{m(i)}) \quad (2)$$

The two dimensional lookup tables are filled with  $\alpha_c^0$ ,  $V_m^0$  and  $\alpha_m^0$ . The result is a non-linear function  $\alpha^0_m = f(\alpha_c^0, V_m^0)$ , as shown in Fig. 7

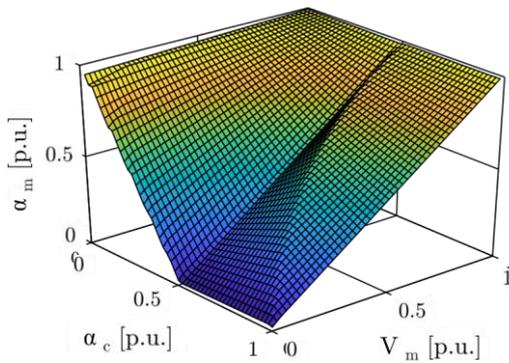


Fig. 7: Data points of  $\alpha^0_m$  inverter duty cycle for 2D-lookup tables.

It can be observed that for high values of chopper duty cycle  $\alpha_c^0$  and  $V_m^0$ , the inverter duty cycle  $\alpha^0_m$  is saturated to 100% duty cycle. And vice versa when  $\alpha_c^0$  is always high but  $V_m^0$  is low therefore  $\alpha^0_m$  is saturated to 0%. Hence, the applied modulation scheme has the intrinsic property of freezing the inverter phase legs when necessary. Once the duty cycle is computed, whatever scheme of modulation could be applied for the inverter output stage. Gate signals must be generated in function of selected topology. For our configuration, three-phase three-level TNPC has been chosen as inverter. For being compatible with the chopper modulation and mainly with the inverter duty cycle offline calculation we

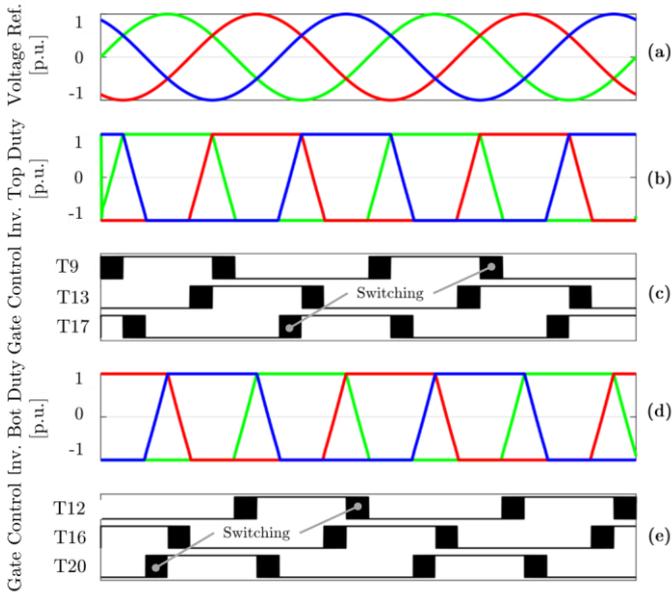


Fig. 8: Inverter output phase duty cycle and gate control signals. Three phase voltage reference signals (a); Duty cycles for the top side of the three-phase inverter (b); Gate signals for the outer top switches of the inverter (c); Duty cycles for the bot side of the three-phase inverter (d); Gate signals for the outer bot switches of the inverter (e).

must choose carriers at 16kHz switching frequency such that they are in counterposition to the chopper carriers as shown in Fig. 6. In this case, the upper switch cell must depend on the carriers of the Top chopper and vice versa. Moreover, each switch cell will guarantee ZVS operation for inverter arms (at least one turn-on or turn-off per switching period in function of the selected rising or falling front carrier configuration) thanks to the extra slight phase shift introduced between Top and Bot choppers and inverter stage carriers. The generated PWM signals for each inverter leg are depicted in Fig. 8. Consequently, the desired switching pattern is obtained for the inverter, thus only one phase leg is switching at a time.

#### IV. SIMULATION RESULTS

The Multiplexed converter has been simulated in the PLECS® software using specifications described in Table I. Fig. 9 shows the multilevel performance of the three-phase inverter (illustrated in Fig. 4) in open loop during steady state over one period of fundamental output frequency. It can be seen that natural balance of the flying capacitors voltage can be achieved through the control algorithm, which allows to generate a five-level output voltage waveform in each phase of the converter.

To evaluate the efficiency of the proposed topology, it will be compared with an existing three-phase multi-level topology: the five-level flying capacitor converter (5-level FCC). This comparison has been carried out using the specifications that are given at Table I, for the same number of output voltage levels, the same rated power, unity power factor and under the assumption that the junction temperature within the

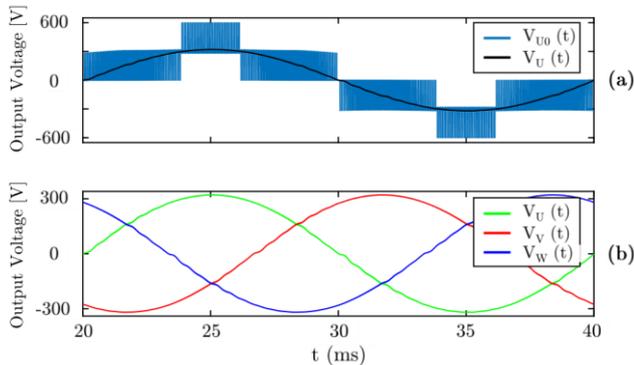


Fig. 9: Multiplexed inverter output voltage referenced to the DC-link midpoint and corresponding filtered phase load voltage,  $V_{vo}(t)$ ,  $V_v(t)$  (a). Filtered three-phase load voltage,  $V_{u,v,w}(t)$  (b).

semiconductor devices remains constant at 75°C at steady state (see Fig. 10). The proposed topology is able to achieve a maximum efficiency of 98,7% using only silicon components.

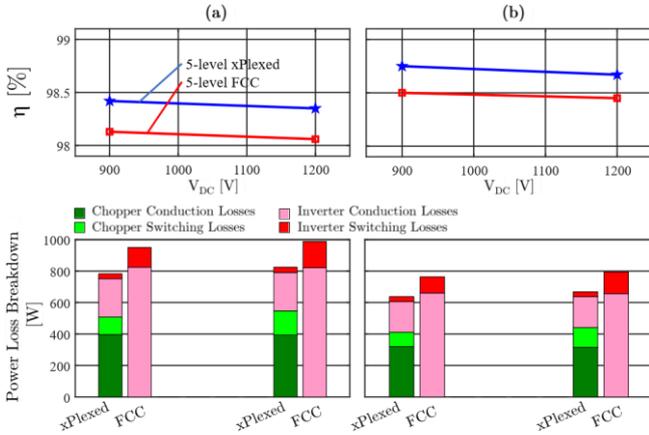


Fig. 10: Efficiency comparison and power loss breakdown for three-phase 5level *xPlexed* converter and three-phase 5-level FCC using specifications of Table I. Left (a):  $V_{Load} = 400V$ ; Right (b):  $V_{Load} = 480V$

Other advantages and drawbacks may arise from the comparison of both topologies. Regarding the number of devices and passive elements, the proposed topology uses less semiconductors and less flying capacitors (cf. Table II and Table ??), making the converter an interesting solution in terms of efficiency, volume and price.

TABLE II: Number of switch semiconductors in compared three-phase 5-level Converters.

Topology	N° Switches	Max. Blocking Voltage
5-level	3	$V_{DC}/4$
5-level FCC	12	$V_{DC}/2$
5-level FCC	24	$V_{DC}/4$

TABLE III: Number of Flying Capacitors in compared three-phase 5-level Converters.

Topology	Flying Capacitors	Capacitance	Rated Voltage
5-level <i>xPlexed</i>	2	150 $\mu$ F	$V_{DC}/4$
	3	150 $\mu$ F	$V_{DC}/4$
5-level FCC	3	150 $\mu$ F	$V_{DC}/2$
	3	150 $\mu$ F	$3V_{DC}/4$

## V. CONCLUSIONS

In this paper, a new multilevel converter topology was proposed. This topology has the ability to achieve a high step down voltage conversion ratio which makes it suitable for new low-medium voltage applications with wide range input voltage such as PV solar inverters and UPS systems. The fact of sharing serialized stages and so cascading inverter by choppers without intermediate filtering elements leads to a reduction of the voltage applied to the switches of the inverter (in some cases ZVS operation is possible), thus reducing the switching losses and indirectly the conduction losses (since switches with a lower voltage rating can be used). The switching losses in the inverter are also reduced because the Top (Max) and Bot (Min) voltage waveforms are synthesized by the choppers, so at any time only one of the inverter legs is switching. These features enables switching at relatively high frequency and helps in the end to obtain a high power density. Moreover, compared to conventional three-phase multilevel topologies it reduces the number of switches thanks to a form of mutualization of chopper stages and besides it uses only low-cost silicon low blocking voltage semiconductor devices reducing the overall cost of converter. An appropriate control strategy for the novel topology is presented. Simulations have been conducted on the PLECS® software

environment with good results and it is shown that the proposed solutions should bring a high efficiency for the coming prototype.

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