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Multi-barrier height characterization and DLTS study on Ti/W 4H-SiC Schottky Diode

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Abstract. Schottky barrier height (SBH) has been characterized on 4H-SiC Schottky diodes with metal contact of Ti/W by Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements between 80 K and 400 K. Multi-barrier has been recognized and calculated according to different models. No clear difference has been found between single barrier diode and diode with multi-barrier from DLTS tests. Evolution on the I-V characteristics has been observed after high temperature annealing. The effect of annealing at room temperature (RT) and high temperature DLTS scan (stress under high temperature) have also been studied on both static characteristics and DLTS results.

Introduction

Inhomogeneous barrier, which manifests as abnormal high current under low forward bias namely double or multi barrier phenomenon, has attracted attention among Schottky barrier diode (SBD) characterization for a long history, and not restricted to SiC devices. Similar phenomenon has been reported especially at low temperature, and it was highlighted that these ‘non-ideal’ diodes occurred regardless of growth technique, pre-deposition cleaning method, or contact metal [1-2]. Schottky barrier height (SBH) has been characterized on Ti/W 4H-SiC Schottky diodes by I-V and C-V measurements under wide temperature range. The evolution on forward I-V characteristics has been observed and investigated by high temperature annealing and accelerated stress with the help of Deep Level Transient Spectroscopy (DLTS).

Experimental Setup

Three 4H-SiC SBDs with metal contact of Ti/W have been investigated and labeled diode #1, #2 and #3. All SBDs with a square surface of 2.48 mm² were provided by our collaborator with a process of etch after sputtering. I-V and C-V characteristic have been measured in the cryostat between 80 K and 400 K with a step of 20 K in the dark to rule out the influence of light, with a *Keithley K2410* and a *Keysight E4990A Impedance Analyser*. Forward characteristics have been measured every 0.01 V with a limitation of 30 mA which is high enough for the study of exponential region of the diodes. Applied voltage varies from 0 V to -5 V with a frequency of 100 kHz to extract the linear performance on the plot of $1/C^2$ vs. V . On top of that, the DLTS tests have been realized with *FT-1230 HERA DLTS (High Energy Resolution Analysis Deep Level Transient Spectroscopy)* system provided by *PhysTech*.

Results and discussion

SBH Identification on Diode #1. As shown in Fig. 1, the forward I-V curves of diode #1 present a second barrier for temperatures below 240 K. The ideality factor n and saturation current I_s could be extracted from the ‘linear’ region in forward characteristic.

Modified Richardson plot. With the help of shallow doping concentration N_D and barrier height calculated from C-V measurements, flat-band SBH (Φ_{BF}) and the modified Richardson constant A^* can be obtained according to modified Richardson plot, as illustrated in Fig. 2 [3]. Two distinct Φ_{BF} are extracted with a higher SBH of 1.20 eV over the whole temperature range studied and the other SBH of 0.72 eV shows up at low temperature only. If considering the constant A^* over both paths and the effective surface of low SBH region should account for 10^{-8} of the total area. However, its influence on forward I-V characteristics could be the major factor especially at low temperature.

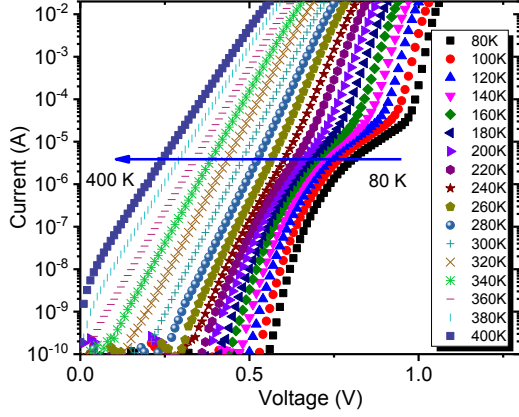


Fig. 1. Forward I-V characteristic on diode #1 between 80 K and 400 K.

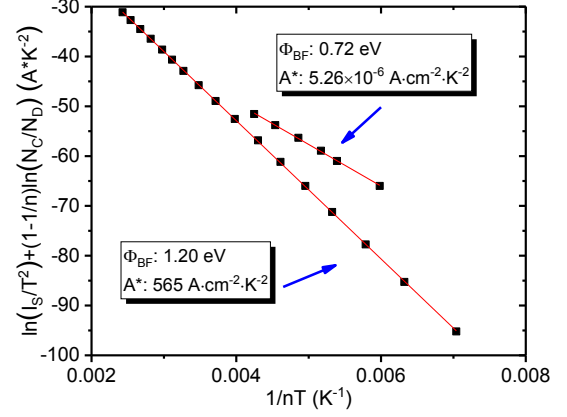


Fig. 2. Modified Richardson plot based on Φ_{BF} for diode #1.

Gaussian Distribution Model. Assuming that SBH is normally distributed on Gaussian [4], its mean barrier height and standard deviation can be extracted with the zero-bias barrier height Φ_0 calculated based on the A^* obtained above, as shown in Fig. 3.

Potential Fluctuation Model. To explain the temperature dependence of the ideality factor, Werner et al. assumed the SBH to be normally distributed, but the mean and standard deviation vary linearly with voltage [5]:

$$\bar{\Phi}_B = \bar{\Phi}_{B0} + \rho_2 V. \text{ and } \sigma_s^2 = \sigma_{s0}^2 + \rho_3 V. \quad (1)$$

Those parameters can be calculated with the plot illustrated in Fig. 4.

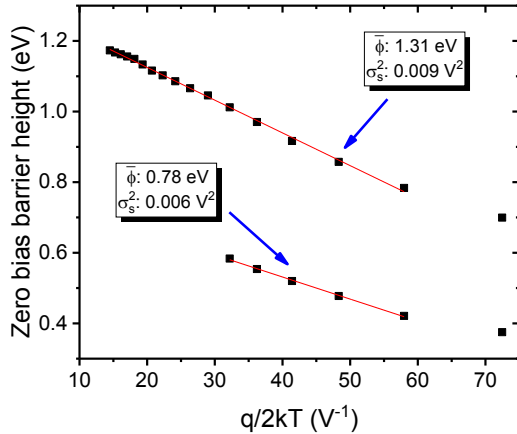


Fig. 3. Φ_0 as a function of $q/2kT$ on #1.

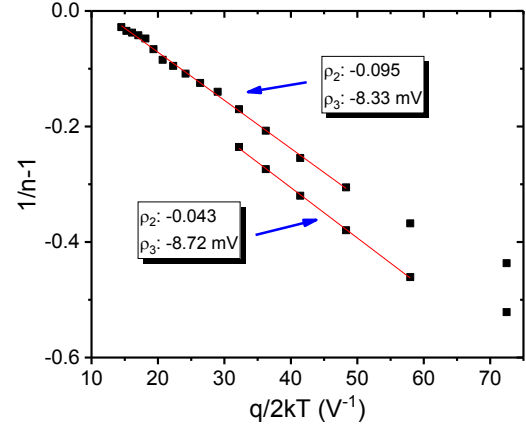


Fig. 4. $1/n-1$ as a function of $q/2kT$ on #1.

Discussion. Two different SBHs are recognized from various models. However, unlike Φ_0 that is strongly depend on temperature as shown in Fig. 3, the recalculated Φ_{BF} at each temperature based on its definition almost keeps constant and is closed to the SBH obtained by C-V (~ 1.19 eV). In addition, similar behavior between Gaussian distribution and potential fluctuation model is forecasted.

I-V Characteristics Evolution on Diode #2. During DLTS study, several temperature scans have been applied on diode #2 as shown in Fig. 5 with that of diode #1 as a reference. Even with almost the same results on DLTS spectra which indicates that no clear difference on trap levels can be found among the temperature investigated, the I-V characteristics could be rather different, as illustrated in

Fig. 6. Considering that samples are reserved in the vacuum dark chamber of DLTS system, the evolution of I-V characteristic could only result from the multi DLTS temperature scan applied.

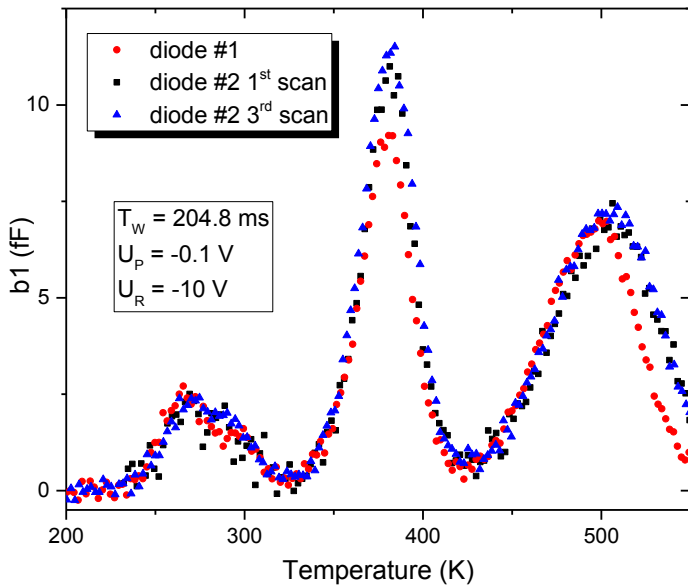


Fig. 5. DLTS signal (correlation b1) between 60 K and 550 K on diode #1 and #2 before and after double barrier shown up. The DLTS parameters selected for all the measurements are marked in the plot. No remarkable difference shows up on current DLTS between 20 K and 180 K either (not shown here).

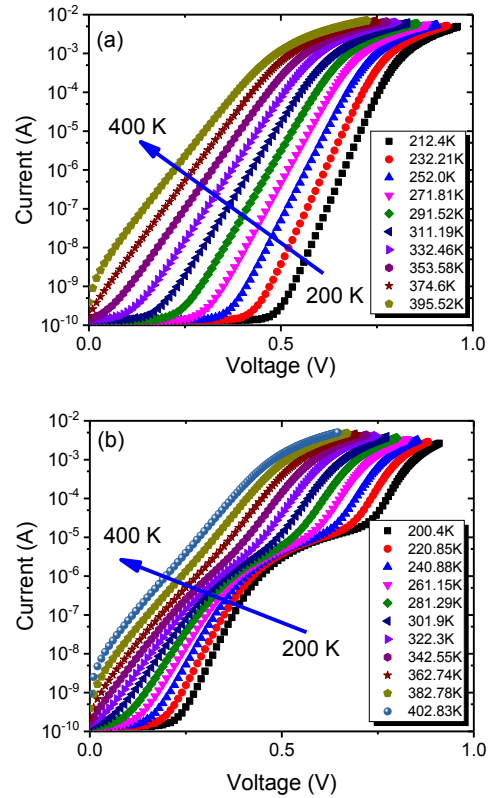


Fig. 6. Forward I-V curves on diode #2 during (a): 1st scan and (b): 3rd scan.

Table 1. Measurement steps and their conditions on diode #3.

Step	Measure	Temperature [K]	Condition	Label
1	I-V	60	–	IV-0
2	DLTS scan	60 – 300	2.5 h	Tempscan-1
3	I-V	60	–	IV-1
4	Annealing	550	AC track signal, 200 min	–
5	I-V	60	–	IV-2
6	DLTS scan	60 – 300	2.5 h	Tempscan-2
7	Annealing	300	Bias = -0.1 V, 3 day	–
8	I-V	60	–	IV-3
9	DLTS scan	60 – 550	6 h	Tempscan-3
10	I-V	60	–	IV-4
11	DLTS scan	60 – 550	$U_P = 0.5$ V, 6 h	Tempscan-4
12	I-V	60	–	IV-5
13	DLTS scan	60 – 300	3 h	Tempscan-5
14	Annealing	300	Bias = -0.1 V, 100 h	–
15	I-V	60	–	IV-6
16	DLTS scan	60 – 300	3 h	Tempscan-6

Annealing and Stress Investigation on Diode #3. In order to investigate the origin of the evolution on I-V characteristics, additional measurements have been adopted on diode #3 as listed in Table 1.

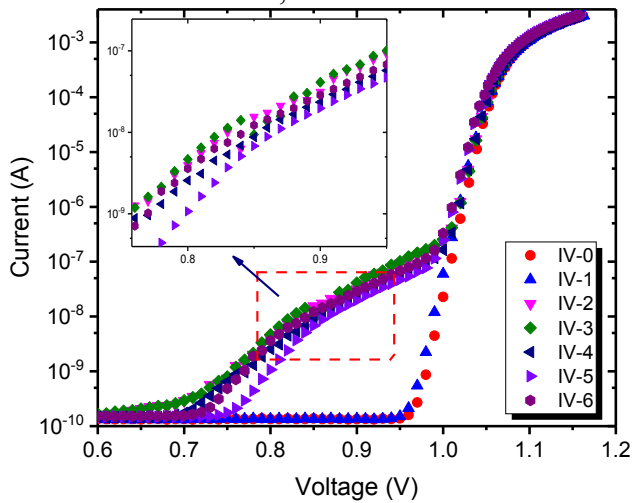


Fig. 7. Evolution on I-V characteristic on #3.

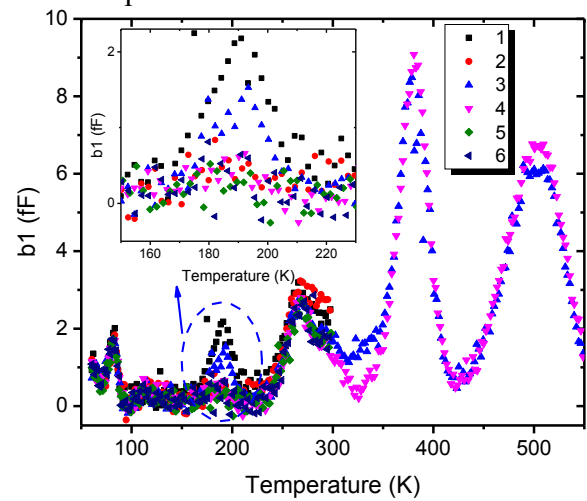


Fig. 8. Evolution on DLTS on diode #3.

Evolution on Forward I-V Characteristics. Fig. 7 shows the measured I-V at 60 K on diode #3 with labels illustrated in Table 1. It is clear that low temperature DLTS scans have no influence on I-V curve. However, multi-barrier shows up after high temperature annealing, while annealing at RT has no obvious effect on I-V characteristic. Furthermore, high temperature DLTS scans reshape the I-V curve, which indicates that possible pinch-off of low SBH takes place under both high temperature and bias stress, this could be annealed at RT to some degree.

Evolution on DLTS signals. Those DLTS signals (b_1) are illustrated in Fig. 8. It is worth highlighting that the peak at around 190 K of the DLTS signal which can be annealed at high temperature will recover at RT. Meanwhile, this defect level is eliminated after high temperature DLTS scan, or in other words the accelerated bias stress due to high temperature, and no recovery is found after RT annealing.

Summary

Multi-barrier has been identified by different models on 4H-SiC Ti/W SBD. No trap level found can contribute to the evolution on multi-barrier formation. However, a second barrier shows up after annealing at high temperature, and cannot be annealed at RT. High temperature DLTS scan, which regarded as accelerated bias stress owing to high temperature, also influences the SBH by reforming the low SBH region, and can be recovered a little at RT. High temperature DLTS scan will also wipe out several defect levels, while annealing at high temperature has only temporary effects on them. Furthermore, the characterization of metal/semiconductor interface is preferred in the future work.

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