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Measurement and Analysis of SiC-MOSFET threshold voltage shift

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Abstract

Silicon Carbide power MOSFETs are used in numerous studies to improve the efficiency or the performance of power electronic converters. However, the gate-oxide technology weakness is a main reliability issue of Silicon Carbide MOSFET transistors. The threshold voltage shift is a critical phenomenon that addresses the reliability of industrial power applications. It is important to have a better understanding of the phenomena implied in the gate threshold voltage shift. In this context, a static ageing test based on JEDEC standard is proposed and the resulting gate oxide stress is studied and discussed in this paper. Complementary testing was performed with dynamic reliability and gate oxide characterizations, such as the charge pumping technique. The results obtained are used to add insight to the current discussion of SiC MOSFET robustness. Additionally, test benches and measurement protocols are detailed.

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1. Introduction

Thanks to its superior electrical properties compared to Silicon, SiC is a promising material for high voltage and high temperature devices. However there are still a lot of reliability issues that remain to be understood such as oxide degradation [1], threshold voltage instability [2], [3] and short-circuit behaviours [4], [5] and [6]. Some of these key points are crucial to develop reliable power devices for industrial applications [7].

Reliability standards regarding ageing such components [8] have been written for Si power switches. But SiC transistors have not the same behaviour than Si devices during ageing [9]. So the scientific community is forced to question whether these standards are suitable for SiC devices or not and how they should be updated [10]. Meanwhile, standard tests are still a known base to provide more appropriate ageing test in a near future for SiC devices. This paper studies the gate instability behaviour in several ageing conditions: static HTGB (High Temperature Gate Bias) [11] and dynamic HTGS (High Temperature Gate switching) tests [1], [12]. The test bench designed for such reliability tests is also presented, along with the conditions of

measurements of the threshold voltage V_{TH} , which is a key parameter. Important findings about its instability have been already discussed [2], [11]. This article proposes a protocol to get rid of the temporary

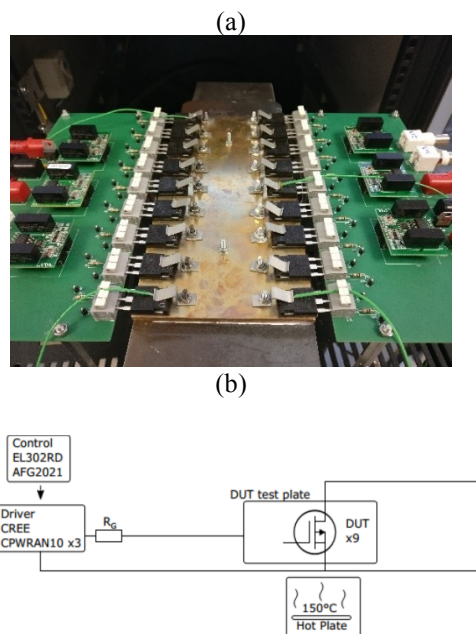


Fig. 1. (a) Ageing setup on the hotplate. 18 MOSFET (9x2) can be aged simultaneously (b) Scheme of ageing test

shift after stress. Moreover, several characterization techniques such as capacitance-voltage (C-V), charge pumping and current-voltage (I-V) measurements are used to monitor the gate oxide degradation during ageing.

To the best of our knowledge, no ageing data on industrial 1700V 45 mΩ SiC MOSFET (Metal Oxide Semiconductor Field effect Transistor) have been reported so far.

2. Experimental set-up

2.1. Test bench and ageing test definition

The test bench presented on Fig. 1 (a) has been designed to run both static (HTGB) and dynamic (HTGS) ageing tests on up to 18 MOSFETs at the same time. The hotplate enables a maximal temperature spreading of 2 °C.

HTGB+ (resp. -) consists in ageing the device by applying a positive (resp. negative) bias on the gate. Because this test is the most used in the industrial world, we decided to start with it in this study.

HTGS consists in ageing the device by applying a pulsed bias on the gate (switching alternatively from V_{GS}^{Low} to V_{GS}^{High}), with a given duty cycle. This test has become more and more common in recent reliability studies papers [12], [13].

During ageing devices were characterized using the Keysight B1506A for measuring datasheet-like characteristics and the B1500 for capacitance-voltage and charge pumping measurement.

2.2. Measurement protocols.

Ageing results on C2M0045170D (part number from Wolfspeed) devices will be presented. The main monitored parameters are the threshold voltage V_{TH} , defined as the gate voltage for which $I_{DS} = 18$ mA at

TABLE I. AGEING TESTS AND PARAMETERS

	Tests (1000 h 150 °C)	
	HTGB+	HTGS
V_{GS}	20V	$V_{GS}^{Low} = -10V$ $V_{GS}^{High} = 25V$
V_{DS}	Floating	
Ageing mode	Static	Dynamic $f = 20$ kHz
Devices	D29 → D37	$\alpha_{20\%}$: D10, 11, 12 $\alpha_{50\%}$: D13, 14, 15 $\alpha_{80\%}$: D16, 17, 18
Parameters	V_{TH} , $R_{DS(on)}$, I_{GSS}	

$V_{DS} = V_{GS}$, the gate leakage current I_{GSS} measured at $V_{GS} = 20$ V and the on-state resistance $R_{DS(on)}$ which is defined for $V_{GS} = 20$ V at the nominal current value $I_{DS} = 50$ A of the device. The I_{GSS} value measured at 20 V is used to check the integrity of the gate oxide. When I_{GSS} goes above a maximum value (fixed at 600 nA as stated on the electrical characteristics of the datasheet) the device is considered as a failed one.

The stress test was interrupted on a regular basis and the devices went through a full characterization i.e classic direct and reverse I-V characteristics, C-V and charge pumping measurements to monitor the variations of the main parameters V_{TH} , I_{GSS} and $R_{DS(on)}$.

Fig. 2 shows the degradation kinetic of V_{TH} recorded during the first measurement batch. As we can notice, the variation of V_{TH} as function of time shows instabilities. For instance, the V_{TH} value after 86 h of ageing time is not consistent with the previous characterization step. We realized later that V_{TH} is recovering as shown on Fig. 3 after a stress on the gate of the devices.

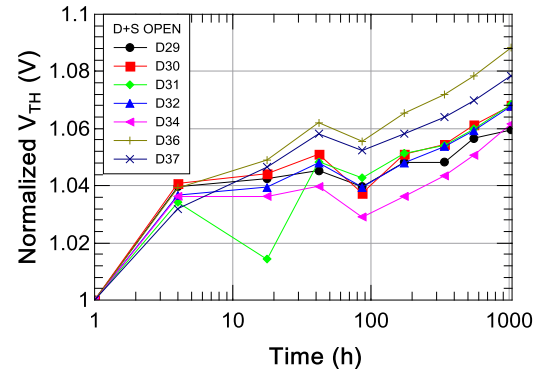


Fig. 2. Normalized threshold voltage shift during HTGB+ static ageing at ambient temperature on 1.7kV SiC MOSFET

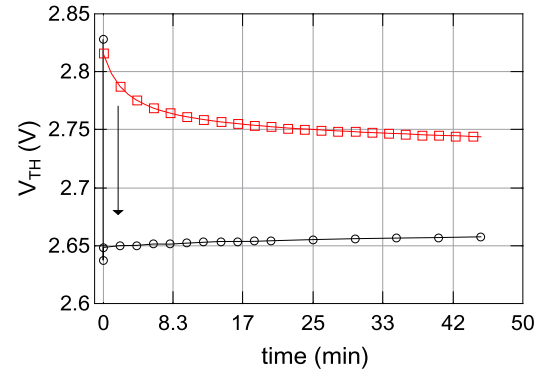


Fig. 3. V_{TH} shift measured directly after 20 min at 20 V at ambient temperature on a 1.7 kV SiC MOSFET (open squares) V_{TH} shift measured after an additional negative pulse on the gate $V_{GS} = -8V$ for 1 s, (open circles). Initial V_{TH} is 2.65 V

This relaxation phenomenon has a critical impact on characterization since it has the same order of magnitude of V_{TH} shift than the one induced by the ageing itself. Only the definitive degradation of the V_{TH} is interesting here. For example, even after a 20 min bias with $V_{GS} = 20$ V at ambient temperature on a brand new component, the threshold voltage is shifting back to pre-stress value with a very slow dynamic as shown on the Fig. 3. There is a time-dependent shift on the threshold voltage which seems to be related to the initial conditions after a positive bias. No stabilization has been observed up to ~ 60 min. To avoid this phenomenon we applied the following protocol, presented in [14] and shown on the Fig. 3 :

1. Negative bias of - 8 V during 1 s is applied.
2. Threshold voltage is measured.

All the following measurements (fig. 4) have been performed with this protocol.

2.3. Reliability testing plan.

Studied devices are 1700V-45 m Ω MOSFET that have been purchased at Wolfspeed and went under a stress plan presented in TABLE I.

3. Experimental results and discussion

I_{GSS} and $R_{DS(on)}$ data have been monitored but as they do not show any significant shifts, only V_{TH} parameter variations are described in the following parts.

3.1. HTGB+ static test.

All the presented DUTs went under a full characterization at $t = 0$ h (before any stress). The spreading of the V_{TH} between each device reached 1.05 V, which is very high.

Fig. 2 shows the variation of the normalized V_{TH} related to the initial threshold voltage value. A positive shift on the threshold voltage occurs and ranges from 5% to a maximum of 8% (270mV) for D36. This can be explained by negative charge trapping either in the SiO_2/SiC interface states or in deeper traps in the oxide.

In the literature, authors worked on reliability of lower nominal blocking voltage of 1.2 kV SiC MOSFET [12]. Earlier results [11] obtained on 1.2 kV SiC MOSFET for similar ageing stress conditions indicates a positive V_{TH} shift of ~ 2.5 V for $V_{GS} = 20$

V during a 1000h static test at 150 °C. First conclusion is therefore that 1.7 kV MOSFET are more reliable in terms of V_{TH} shift after HTGB ageing for 1000h.

3.2. HTGS dynamic test.

Working only on static ageing test is not enough to study reliability of the power devices. In this matter HTGS is closer to the real operation of MOSFET devices in power applications. Therefore V_{GS}^{High} and V_{GS}^{Low} , high commutation frequency and duty cycle are all parameters that companies are interested in. In this part, the influence of several parameters such as V_{GS} values, commutation frequency and duty cycle were investigated on 9 similar devices (see Fig. 4a). The frequency of 20 kHz was chosen because it is representative of the industrial application reality [7].

Fig. 4 (a) shows the V_{TH} shift after HTGS stress

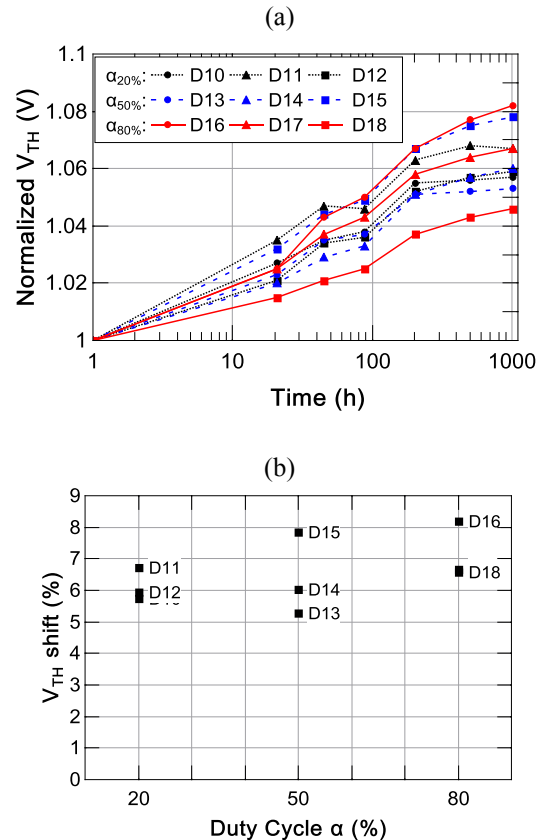


Fig. 4. (a) Normalized threshold voltage shift during HTGS static ageing at ambient temperature. (b) HTGS2 $\Delta V_{TH} / V_{TH}$ (%) for three different duty cycle, $\alpha = 20\%$, 50% and 80%

for three different duty cycles. Those testing conditions resulted in a mean positive shift on all the 9 DUTs of approximately $V_{TH}^{HTGS} = 170$ mV. Except for D18, they all undergo a $>5\%$ positive shift on their initial threshold voltage value. In more details, the mean values of relative V_{TH} shift vs. duty cycle from Fig. 4 (b) are 6.1 % for $\alpha = 0.2$, 6.4 % for $\alpha = 0.5$, and 7.2% for $\alpha = 0.8$.

So there is an increase of 1 % on the threshold voltage shift between devices aged with $\alpha = 20$ % and 80 %. The impact of the duty cycle was already pointed out in the literature [12] with a higher shift. This could be a consequence of the higher frequency of 20 kHz used in our experiments in regards to the frequency of 10 kHz used in [12]. Concerning HTGS, DUT with $\alpha = 50\%$ seems to have reached an asymptote at 1000 h of ageing.

It is common to extrapolate ageing data to see the critical parameters shift in a longer period of time. An average lifetime of 10 years is required for power converter applications. In this particular dynamic ageing case, extrapolation to 10 years indicates a shift of the threshold voltage of 20 % in the worst scenario (sample D18).

3.3. Gate oxide analysis

Characterizations of the SiO_2/SiC interface via C-V, charge pumping and gate leakage current add a deeper level of understanding.

Fig. 5 shows the gate current vs. the gate voltage (drain at 0 V) for three different temperatures: 25, 50 and 150 °C. Each sweep performed from 0 to 35 V is directly followed by another bias from 0 to -30 V. The gate leakage current starts to increase exponentially around 25 V and -15 V, and this increase is characteristic of the Fowler-Nordheim effect. It is interesting to note that the negative bias is not stable, as already showed in [15] on p-type MOS capacitors. For low negative V_{GS} , the p region under a part of the gate is in accumulation mode and, therefore the gate current is due to injection of hole from SiC into the oxide. It cannot come from injection of holes from the n region because the n region is not in inversion but depletion mode. For high positive V_{GS} , the FN regime is more stable (begins at ~ 28 V) and is due to the injection of electrons from accumulation layer in the n channel under the gate or from the N^+ source region. Although such high values of V_{GS} are not reached in ageing tests, these instabilities (present even at -8V or +20 V) may lead to small variations in effective charges trapped in the oxide, and to a small V_{TH} shift.

Quantitative data are difficult to obtain due to a lack of knowledge on the exact geometry of the component. To extract value of barrier height, exact surface of channel or of p-type region under the gate are mandatory.

Fig. 6 shows C-V measurements on sample D36 (similar data are obtained on all samples). The setup of the Keysight B1506A is using C_{iss} measurement, with shorted Drain and Source pads.

For $V_{GS} < -5$ V the n region under the gate is depleted, thus the measured capacitance is mainly the gate to source capacitance. No voltage shift is observed after ageing on this part of C-V.

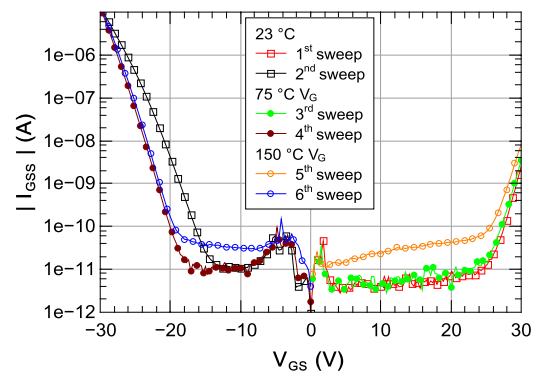


Fig. 5. C2M0045170D I_G - V_G characteristics vs. temperature

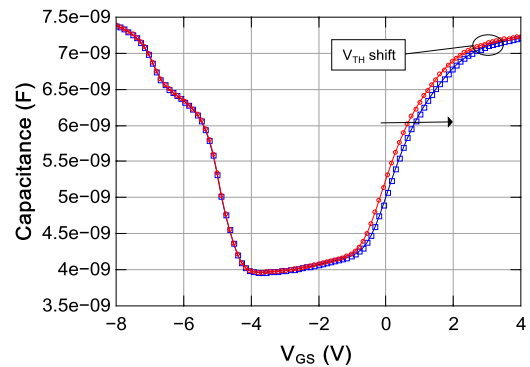


Fig. 6. C-V characteristics measured at 100 kHz on sample D36 initial C-V @t = 0 h in red circle and final in blue square @t = 1030.1 h on DUT D36 at ambient temperature.

For $V_{GS} > -1$ V, the n region under the gate is in accumulation mode, so the p region should be in inversion mode because V_{TH} is the voltage to apply to pass the structure from weak inversion to deep inversion. Only in this part, a positive V_{TH} shift (~ 230 mV) is observed, i.e. a negative charge has been injected in the oxide. It could be due to an injection of electrons in the oxide from the n region under the gate during the positive part of the ageing pulse. It is consistent with the fact that V_{TH} shift increases with the duty cycle.

Charge pumping measurement is another technique that should give precise interface trap density in a SiC MOSFET [16]. As the power structure of a SiC MOSFET does not allow access to the substrate thus it is not possible to directly measure the current I_{cp} , the method used is a modified three terminal, introduced by Passmore and al. in 2005 [17]. Sending a trapezoidal signal of frequency f with a fixed amplitude on the gate, the current is measured on the Drain with a high resolution SMU. Drain and source are kept grounded. Then the base value V_b of this signal is increased. Fig. 7 shows the current measured for different frequencies and the pumped charge Q_{CP} vs. f which is linear. This last curve is typical from charge pumping technique. Fig. 8 shows different CP curves obtained with different gate signal amplitude, using the same low level of V_{GS} . Maximum amplitude is obtained when the MOSFET is gone from inversion to accumulation mode. Shape of the curve is not usual for a MOSFET for microelectronics, but this could be explained by the complex structure of the power MOSFET, showing an oxide both on p-type and n-type regions. Shift of the curve towards negative voltage is consistent with the CP principle. The magnitude of the peak should be related to the interface trap density, and should be rather constant when $\Delta V > V_{TH} - V_{FB}$.

Fig. 9 shows charge pumping characteristics measured before and after a voltage stress on the device. The peak magnitude does not increase despite the ageing thus the stress does not create additional interface traps. The shift of the curve towards positive voltage comes from negative charges being definitely trapped in the oxide, in the same manner that we have discussed about C-V. In this case again without data on the gate technology, it is not possible to draw quantitative conclusions and the interface trap density is barely achievable. If an area of 14.3×10^{-6} m² is taken arbitrary (estimated roughly from the bare die datasheet and from SiC MOSFET available gate area),

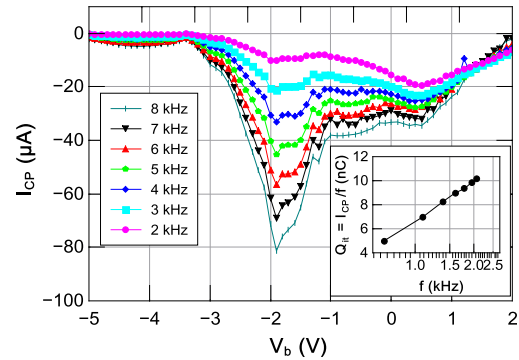


Fig. 7. Influence of frequency on charge pumping measurement on C2M0045170D at ambient temperature, for $\Delta V = 4$ V. Q_{cp} slope $\approx 2.46 \times 10^{-9}$ C.s

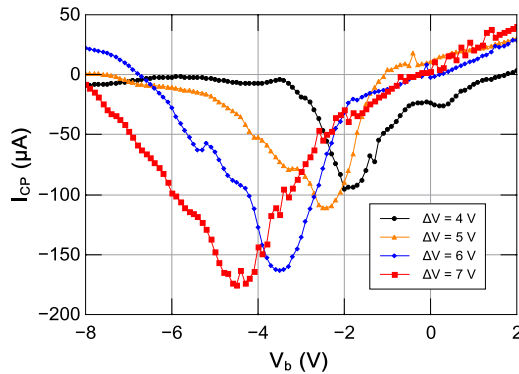


Fig. 8. Influence of gate signal amplitude ΔV on charge pumping measurement on C2M0045170D at ambient temperature, for $f = 10$ kHz

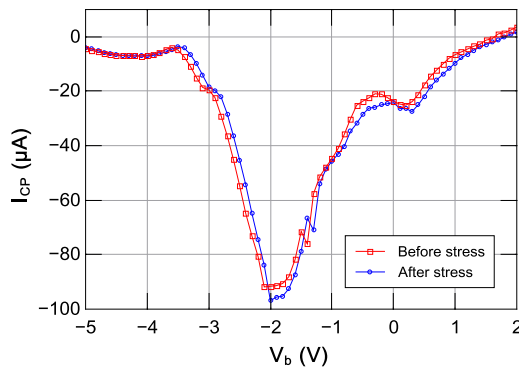


Fig. 9. Charge pumping measurement before and after a strong bias of 30 V for 12 h on a 1.7 kV gate.

then the density of trapped charges near the interface state D_{it} can be approximated to 3.4×10^{10} eV⁻¹.cm⁻².

4. Conclusion

This paper presents an ageing study on 1.7 kV 45 mΩ SiC-MOSFET. A lifespan of 10 years (~87600 h) is required by industrials on their application. In this scenario then for HTGB the shift is going up to 450 mV (12.7 %) of the initial threshold voltage value for D36. For HTGS the worst case is a 240 mV (14.2 %) shift for D16.

So the V_{TH} evolution during both static and dynamic ageing is worrying.

We have pointed out a very important phenomenon related to the stability of the recorded V_{TH} after ageing. Indeed, a relaxation phenomenon is observed and a measurement protocol was proposed to eliminate the component of V_{TH} that is rapidly recovered. Also a deeper investigation was performed by means of gate leakage current analyses, C-V and three terminal charge pumping measurements. They show that the degradation observed on the 1.7 kV threshold voltage during ageing is real, and non-recoverable and probably due to injection of electrons from the n-region into the oxide of the devices. Interface trap density does not seem to be modified after a high voltage stress (30 V for 12 h) on the gate.

In a near future, modeling of trapping/detrapping phenomenon will be performed. TCAD simulations with the complex structure of SiC MOSFET are also required for a better understanding of the semiconductor physics and charge pumping measurements.

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