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Topologies for high-voltage low-power integrated DC-DC converter

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Abstract

The conversion from a high-input-voltage to a low-output-voltage with low-output-power and large efficiency is challenging, particularly if a limited voltage technology is considered for silicon integration. After presenting few criteria, the paper reviews possible topologies for silicon integration of active devices. A preliminary demonstrator is experimentally analyzed to draw conclusions and prepare the specifications of a future integrated circuit.

Introduction

Along with the electric vehicles market penetration, batteries of new generation and with higher operating voltage are forecasted, bringing with them new needs in terms of power supply. The main battery voltage bus is very often as high as 400 V or even 800 V for the next generation of electric cars [1]. In parallel, more and more systems need to be powered directly from the high-voltage battery, for safety reason for example, like the Pyroswitch [2]. For this reason, a new category of dc-dc converter is emerging, with high-voltage input, low-voltage low-power output and with requirements concerning small-size and high-efficiency inevitably brought by the embedded context. Some constraints are presented in Table I.

Table I: Converter's general specifications

Input voltage	From 300 V to 1000 V
Output voltage	12 V
Output power	~ 1 W
Isolation	Reinforced isolation
Efficiency	> 85%

Literature is not abundant about high-voltage to low-voltage conversion, not to mention low-power. The conversion from 230 Vac rectified was studied in [3], without the isolation though, considering a two-stage approach: a capacitive voltage divider, based on a switched-capacitor converter, with a cascaded buck stage. Originality of the present work is to study an isolated converter while keeping a reasonably high efficiency to allow further increase of power density, and taking into consideration some aspects linked to the on-chip-integration possibilities of the power-stage.

To better present the topology review, it is necessary to explicit why such a conversion from high-voltage input to low-voltage low-power output is challenging. First, high step down ratio is always presenting a challenge in terms of efficiency, control and volume [4]. Additionally, a bulky transformer is needed to limit the losses due to high-voltage input. This conflicts with the small-size requirement. Finally, maximum input voltage is larger than most power switches breakdown voltage in silicon integration context, requiring series configuration.

It is worth investigating more complex unconventional topologies to address this particular conversion, as simple topologies could not bring satisfying solutions. A converter topology review is necessary to introduce a trade-off solution with respect to the transformer size and the active device voltage rating, i.e. limited by the microelectronics technology.

Topology review

To identify topologies more suitable to operate this conversion, a qualitative topology exploration is performed. The goal of this study is to identify structures presenting characteristics that could fit the application. To better underline the pros and cons of each of them, some criteria are selected.

Selected criteria

- **Maximum flux density:** Transformer size and losses are critical to respect specifications. For this criterion, the maximum flux density B_{MAX} is evaluated, based on maximum volt-second applied on primary side. Core losses inside the transformer are directly related to this parameter, it will therefore impact the design of the transformer (geometry, core material, etc.).
- **Electrical stress:** To manage the high input voltage, the power-stage requires high-voltage power-switches. Some structures can help reducing the voltage stress applied to the power-switches. It allows to decrease their size and improve their performances, as not many power switches can withstand 1 kV in silicon integration context.
- **ZVS:** Some topologies enable ZVS (Zero Voltage Switching) operation, allowing to reduce switching losses that can be very important due to high-voltage. This mode however requires to pay special attention to command of the power-stage.
- **Complexity:** In order to reduce power-stage size, one option is to reduce the amount of components needed and their size. If the transformer size is already described by the first criteria, the number of switches (MOSFETs, diodes), of capacitors, etc. is also an indication on the space that the power-stage will occupy on a board. Value and voltage rating of these components will of course have an impact on their size, and it can also give an indication on the possibilities to integrate them in a chip.
- Other criteria are important, as start-up, feed-back loop, stability approach, etc. but are not considered here.

Using these criteria, it is now possible to evaluate different solutions to comply with these conversion specifications.

Overview of some interesting topologies

An interesting approach in terms of genericity is the multi-converter arrangement. ISOP converters (Input Series Output Parallel, see Fig. 1) offer a reduction of the input voltage on each converter, making possible the use of a converter designed for a lower input voltage than the specification [5]. Moreover, if the converter brick is able to operate in ZVS mode, the ISOP arrangement will probably be able to operate in this mode. However, this type of solution requires the use of a bulky transformer with multiple primary windings, and with no reduction of flux density B_{MAX} . The use of a single transformer also requires a good synchronization of the different converters. Finally, an additional regulation is needed to ensure a good sharing of the input voltage.

Another possible approach consists in a converter with two-stages. As studied in [3], the combination of a 1st stage using Switched-Capacitor (SC) conversion and of an inductor-based 2nd stage (with no isolation) is offering very interesting characteristics. The SC converter enables small-size solution, as no

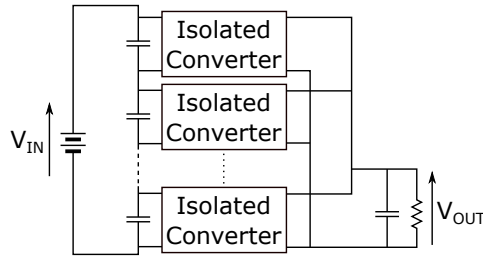


Fig. 1: ISOP arrangement

magnetic element is required, and can easily divide the input voltage by a fixed ratio [6]. Transformer-based stage then takes care of isolation and regulation of the output voltage. The second stage architecture is simplified since maximum voltage to process is reduced. It enables a reduction of stress on the transformer but also on the switches. An example of such topology is presented in Fig. 2. However, the SC converters are not able to operate in ZVS mode, leading to higher switching losses. Plus, the SC structure increases the number of high-voltage passive components (>100 V capacitors) that cannot be integrated easily. It means the final solution counts an increased number of external passives, which can also make the interfacing with an integrated controller difficult, because of the multiplication of I/Os.

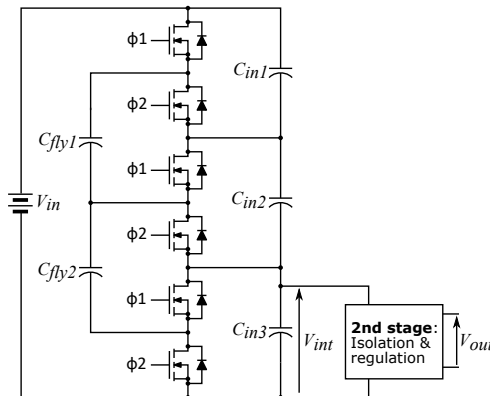


Fig. 2: Example of two-stage approach, with Switched-Capacitors first stage

Finally, another category of converters presents characteristics that could address the problem presented here: the multi-level converters. They are well known because they offer a way to efficiently reduce the electrical stress on switches [7]. Different types of multi-level exist (Neutral Point Clamp, Flying Capacitor, etc.), but only Multi-level Flying-Capacitor are considered here (Fig. 3). They allow a reduction of transformer excitation with the adequate switching sequence, leading to reduction of its size. They can be seen as a hybridization between a Switched-Capacitor based circuit and a classical inductor-based converter, and it is therefore more compact than the two-stage approach. Although the flying capacitor can bring an additional complexity, at start-up or in transient, it is also the case for the other structures, as they also relies on capacitive dividers. However, the multi-level topology presents the advantage of being a simple one-stage solution.

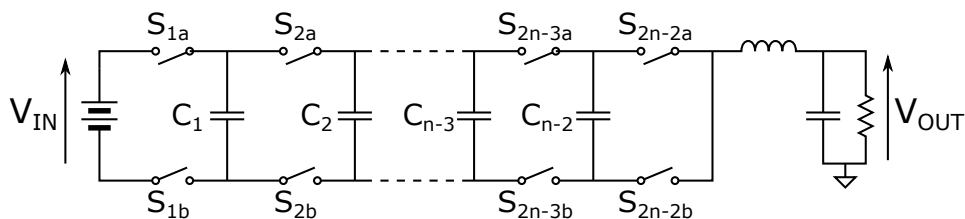


Fig. 3: Example of n-level flying-capacitor buck converter

Numerous topologies have been considered and many criteria have been confronted. It is not considered here to write a figure of merit for straight selection as integrability is not a quantitative figure. There is in fact no topology that is much more suitable than the others. So one criterion is the simplicity of the topology for the sake of robustness and safe operation. For this reason the multi-level flying-capacitor approach is selected in a first step for evaluation.

Proposed converter

Presentation of the topology

In Fig. 4 is shown the architecture of the proposed hybrid converter: a 3-level flying-capacitor with transformer interfaced as in FlyBuck topology [8]. Therefore, it is known as the 3-level Flying-Capacitor FlyBuck topology (3L-FC-FlyBuck). It counts four high-voltage power switches and one flying capacitor. Only the active switches with related drivers and the controller feedback solution are to be integrated on silicon. Passive components will be off-chip: the number of I/Os is in favor of this topology as well.

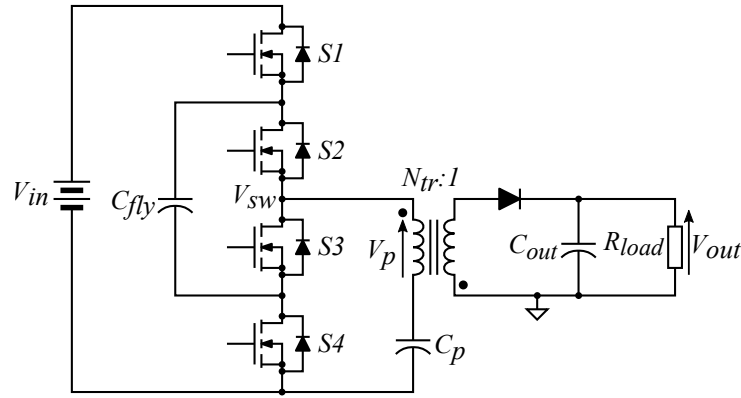


Fig. 4: Proposed converter topology - 3-level Flying-Capacitor FlyBuck

In a first step, the number of levels was chosen to be low as each additional level adds another degree of complexity to the power-stage (need to add one flying capacitor and two power MOSFETs for each additional level). Silicon integration also limits the maximum number of levels. If increasing the number of power MOSFETs in series can help reducing the voltage-stress, it also increases quantity of complex silicon circuits (gate driver, level-shifter, etc.) needed. A trade-off therefore exists between the voltage rating of the power switches and the complexity of the driving circuits, in terms of area and cost of silicon. When a silicon technology is selected the voltage rating of the active device sets a limit to the input voltage. Fortunately the topology in Fig. 4 may be extrapolated to cope with a higher input voltage when increasing the number of levels.

Fig. 5 is presenting the switching sequence of the proposed converter. A period is composed of 4 states (if not counting dead-times). Energy is stored inside the transformer when $S1$ or $S2$ are in ON-state. Energy is transmitted to the load when primary voltage (V_p) is negative, i.e. when both $S3$ and $S4$ are turned-on. Output voltage is set by the voltage on capacitor at primary (V_c), which depends on the duty-cycle, on input voltage but also on the dead-time. The balancing of volt-second applied on the primary leads to the following relation:

$$V_{OUT} = \frac{N_S}{N_P} * V_{IN} * \left(D + \frac{dt_{total}}{4 * T_{per}} \right) - V_f \quad (1)$$

With N_P the number of primary turns, N_S the number of secondary turns, D the duty-cycle of high-side switch, dt the total amount of dead-time to operate ZVS transition, T_{per} the switching period and V_f the voltage drop on the secondary side diode. In a first time, the slope of primary voltage (V_p) during transition phase is considered constant.

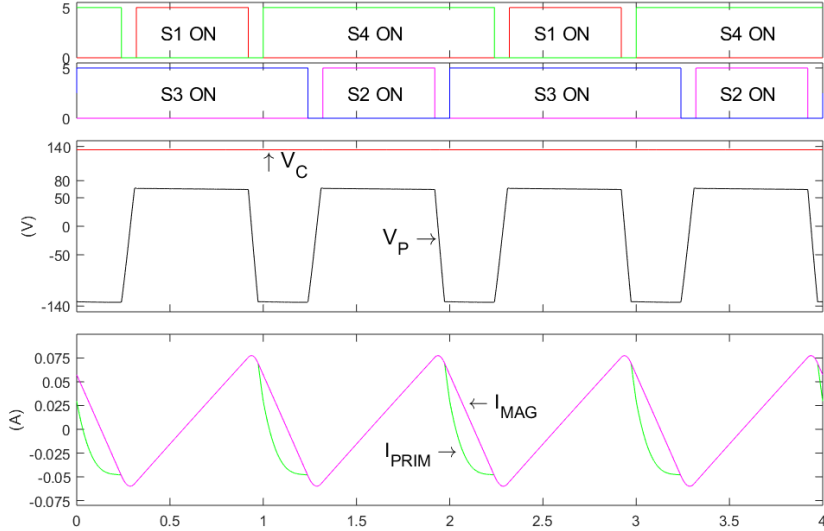


Fig. 5: Simulation waveforms of 3L-FC-FlyBuck

Main characteristics

The ideal voltage across the flying capacitor (C_{fly}) is, in steady-state, half of the input voltage. This helps reducing the amplitude of the voltage variations on the floating node (V_{SW}), which limits the transformer excitation (V_P) and voltage stress on the switches. Therefore, input voltage can be as high as two times the MOSFETs voltage rating. Moreover, if the flying capacitor voltage is close enough to its ideal value, the frequency seen by the transformer is the double of the switching frequency. This is because the two half periods show similar current and voltage waveforms.

ZVS operation is enabled thanks to current in the primary (I_{PRIM}) flowing in both directions, due to the magnetizing current's triangular waveform (I_{MAG}). The product of switching frequency (f_{SW}) and magnetizing inductance (L_{MAG}) sets the current available for ZVS transition for a determined input voltage. ZVS operation can be observed in Fig. 5, as some dead-time is left between turn-off and turn-on of two complementary switches. When a switch turns-on, its drain-source voltage is already close to zero, which drastically reduces switching losses.

The difference between the primary current (I_{PRIM}) and the magnetizing current (I_{MAG}) is the image of the current flowing in the secondary. The current flows through the diode only when both low-side MOSFETs ($S3$ and $S4$) are in ON-state. This limits the amount of time in which energy is delivered to the secondary, making it difficult to get to desired power when duty-cycle gets close to 50%.

Moreover, the primary current is used to determine a model (validated in simulation) for conduction losses in the MOSFETs, the transformer and the rectification diode. At this state it is difficult to write the specifications of the integrated circuit so a practical demonstrator is built.

Experimental results

A quick prototype is built on a standard PCB. MOSFETs gate control signals are generated from a digital resource. As a simplification, the gate drivers are supplied from an isolated dc source. Isolated gate driver are used to be able to control easily floating MOSFETs. The PCB demonstrator is shown in Fig. 6. The discrete components used to build this prototype are listed in Table II.

The waveforms presented in Fig. 7a are obtained with $V_{IN} = 400$ V, $f_{SW} = 125$ kHz and an effective duty-cycle around 30%, to get $V_{OUT} \sim 12$ V. Middle-floating-node (V_{SW} , in green), varies between ground level and $V_{IN}/2$. It shows that flying capacitor is indeed charged to half of the input voltage. The shape of the primary current (I_{PRIM} , in pink) is also similar to the one obtained in simulation. The perturbation observed in primary current (I_{PRIM}) during the transition phases (when V_{SW} is rising or

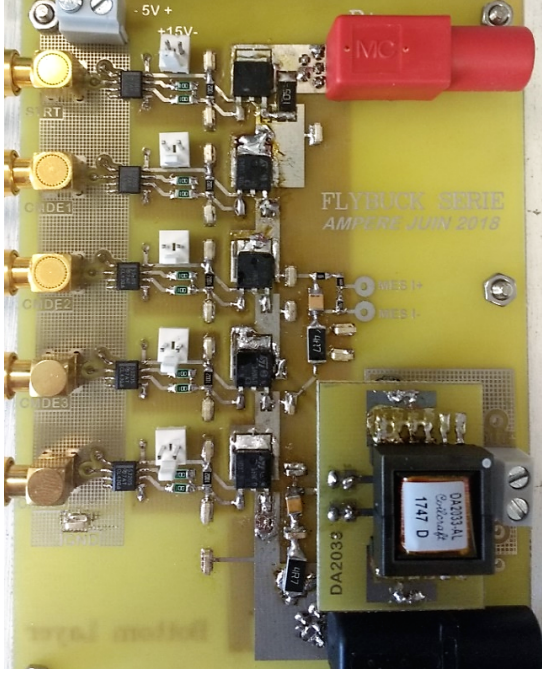
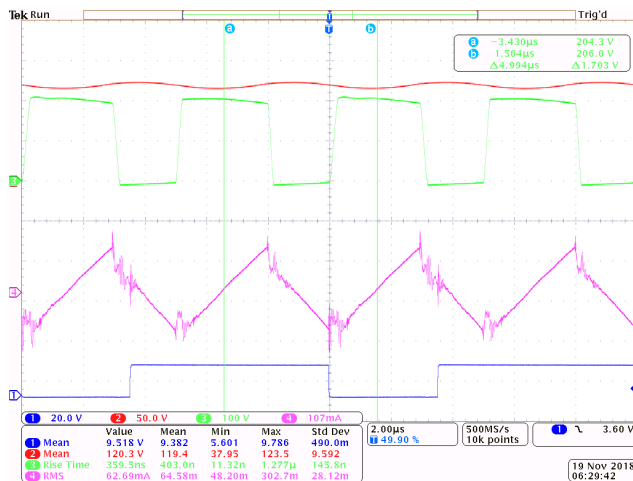


Fig. 6: PCB prototype with discrete components

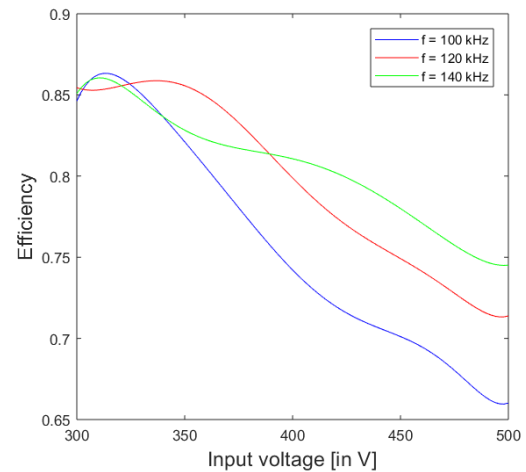
Table II: List of main discrete components

Power MOSFET	STD1HN60K3 from STMicroelectronics - $R_{DS} = 6.7 \Omega$ - $V_{DS-MAX} = 600 \text{ V}$
Transformer	DA2033-AL from Coilcraft - $N_P/N_S = 10$ - $L_{MAG} = 1 \text{ mH}$
Secondary diode	PMEG10020ELR from Nexperia - $V_F = 0.5 \text{ V}$ - $V_R = 100 \text{ V}$
High-voltage capacitances	22 nF, 630 V
Isolated gate-drivers	UCC5320SC from Texas Instruments

falling) is due to parasitic capacitances/inductance. Parasitic capacitance between primary and secondary of the transformer will sink some current during the transitions, while leakage inductance and junction capacitance of secondary diode will create ringing. The gate voltages of switch S_4 (in blue) also validates the ZVS mode: V_{SW} slowly falls before switch S_4 turns-on. Finally, voltage on primary capacitor (C_p , in red) is also very close to the expected value (i.e. effective duty-cycle times input voltage). As expect from simulation results, the two half periods are very similar in terms of voltage and current waveforms, leading to a doubled frequency on transformer.



(a) Main measured waveforms



(b) Power-stage efficiency for different frequencies

Fig. 7: Main waveforms on primary and efficiency measurements

Efficiency measured for a 1 W load and output voltage close to 12 V is presented in Fig. 7b. Even though good efficiency is obtained for input voltage lower than 400 V ($>75\%$), values observed for high input voltage are not satisfying, particularly at low switching frequency. The use of an inadequate transformer might be causing additional losses. Efficiency measurements only take into account the power delivered by input voltage supply, and don't include therefore the power needed to supply the isolated gate-drivers.

To understand how efficiency can be improved, a breakdown of the losses is computed for no-load operations (Fig. 8). No switching losses are considered as the power-stage operates in ZVS mode. Both conduction losses in switches and copper losses in transformer are modeled with DC resistances, using measured primary RMS current. Remaining losses are attributed to the transformer losses.

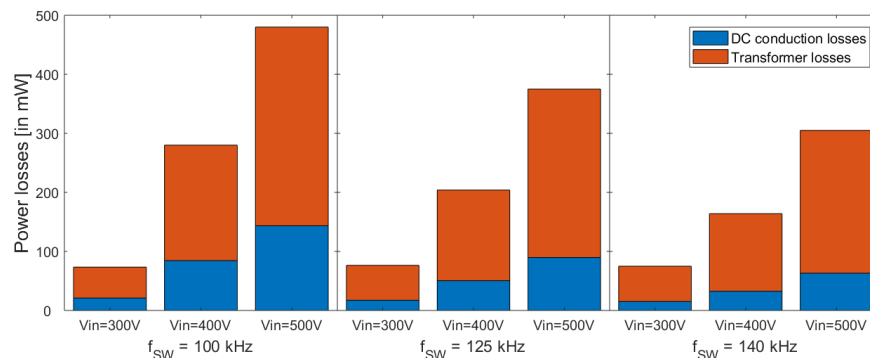


Fig. 8: Estimated power losses breakdown

Results show that higher switching frequency enables the reduction of both conduction losses and transformer losses. Lower conduction losses can be explained by lower amplitude of magnetizing current, as this amplitude is inversely proportional to the switching frequency. Transformer losses are coming from AC conduction losses (coil resistivity increasing with frequency due to skin effect and proximity effect) and from core losses (occurring in the magnetic core). As detailed transformer characteristics are not known, it isn't easy to identify with accuracy the main source of losses inside the transformer. Future design of the converter will therefore include a custom transformer with known characteristics.

To further improve the performances of the converter, transformer losses will have to be taken care of. If conduction losses can be reduced by decreasing the amplitude of the magnetizing current, core losses also need to be reduced. To do so, a material such as 3F4, adapted to higher switching frequency will be used. Using iGSE [9], value of core losses were computed for this material, and results concord with efficiency initial specification ($>85\%$).

Conclusion

Low-power converters with high-voltage input and low-voltage output become more and more common. Conventional converter topologies are not adequate to operate this conversion. Therefore, more complex solutions are reviewed and a PCB demonstrator is built using the 3-Level Flying-Capacitor FlyBuck converter topology. The functional operation of the converter seems satisfying enough to trigger a first integration circuit. The isolated gate-drivers will not be implemented in favor of level-shifters. The design of the IC driving the converter will improve solution performances, with higher efficiency and possibility to accept input voltage higher than power-switches breakdown voltage.

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