Ultrawideband Chipless RFID: The Reader Technology From SFCW to IR-UWB

Marco Garbati, Etienne Perret, Romain Siragusa, Christophe Halope

UWB Chipless RFID – the Reader Technology from SFCW to IR-UWB

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I. INTRODUCTION

RADIO frequency identification (RFID) is a widely employed wireless technology to identify items and animals (humans are in this category). The reader, which is usually controlled by a computer, transmits an interrogating signal towards the tag. This backscattered signal is in turn modulated from the tag, mostly with either binary phase shift keying (BPSK) or amplitude shift keying (ASK) technique. This is possible by the presence of an application specific integrated circuit (ASIC) [1].

Depending on the application there are different RFID technologies, and thus numerous types of tags [2, 3]. These communication systems are narrowband with dedicated frequency bands from low frequency (LF) to ultra-high frequency (UHF). Anti-collision protocols are used for a robust implementation. However its main drawback is the cost of the tag, which can be a limiting factor for some applications. A passive ultra-high frequency (UHF) RFID chip costs a few Euro cents, and it is costly compared with barcode labels. Thus, barcode technology is the world leader for item identification. The labels are extremely cheap to produce, and thanks to its well-known technology, the reader is affordable. It is easy to find commercially available barcode readers for a few tens of Euros. Currently the barcode reader is integrated in portable devices such as the smartphone using image post-processing techniques. The barcode label is worth only a fraction of a Euro cent because it can be realized on a paper substrate with a directly printed code.

The chipless RFID technology plays an intermediary role between the conventional RFID and the barcode. The tag does not have any chip and the circuit is directly printed on substrate. This characteristic allows the tag to be potentially as cheap as a barcode but with a higher read range, and the capability to be read without a line-of-sight condition. However, lower coding capacity is obtained [2, 4], but this can be mediated by sensor capability embedded on the tag [5- 7].

Much effort has been spent developing chipless tags. These solutions are often realized using costly substrate, with lithography or milling techniques [8-11] as proof of concept. Some chipless tags have been proposed on paper substrates to reduce the tag realization cost [12]. This article focuses on the reader part of the chipless RFID technology in the ultra-wideband (UWB) (3.1-10.6 GHz). A comprehensive overview of the reader technology from its origin is given. The design of the tags based on time-domain and frequency-domain approaches are first introduced to give insight into the reader architectures. The state of the art of frequency and time domain readers are discussed. Their main characteristics in terms of performance, read time, and spectrum characteristics are studied.

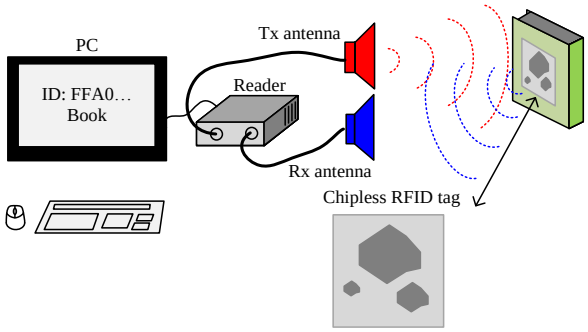

Fig. 1. Schematic of a chipless RFID system. The reader interrogates the tag with a UWB signal, and then the backscattered signal from the tag is analyzed to retrieve the tag ID.

II. WHAT IS A CHIPLESS RFID SYSTEM ?

Chipless RFID technology started at the beginning of this century, with the Richard Ribon Fletcher's PhD dissertation published in 2002 [13]. In 2005 Michael Pettus patented a chipless RFID system where the tag was composed of a multitude of RF antennas [14]. Each antenna provided a different orientation and phase characteristic so as to encode the tag (transponder) identification (ID). In that system the reader scanned an area and retrieved the tag information using radar imaging techniques. Since then, chipless technology has being seen continuous growth of interest world-wide, mostly from universities. It is a technique of identification where the tag does not have any electronic component attached to its surface. Only the EM backscattered properties of the tag are used for the identification.

A chipless RFID reading system is shown in Fig. 1. The tag is composed of a pattern (similar to a barcode) upon a substrate and is made of a conductive material. The pattern is

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realized with etching or printing techniques. The operating principle of a chipless RFID system is similar to radar applications, where no radar cross section (RCS) modulation is expected from the target. Contrary to RFID, the reader transmits a wideband signal to the environment, and the tag backscattered signal is measured and analyzed in the time and frequency domain to retrieve the desired information [2]. Signal modulation cannot occur in chipless RFID systems due to the absence of a chip in the tag. Thus, the chipless RFID is not compatible with narrow-band identification systems such as classic RFID.

A chipless RFID tag can be thought as a passive frequency selective device such as a filter, where the information is coded based on the impulse response of the tag: a wider available bandwidth means a higher coding capacity. A chipless RFID system needs to be compliant with UWB regulations in the band 3.1 - 10.6 GHz [15, 16]. Higher frequency bands are also being used in chipless RFID for different applications [17, 18], however these frequency bands are not the subject of interest in this article. The next section introduces chipless RFID tag technology.

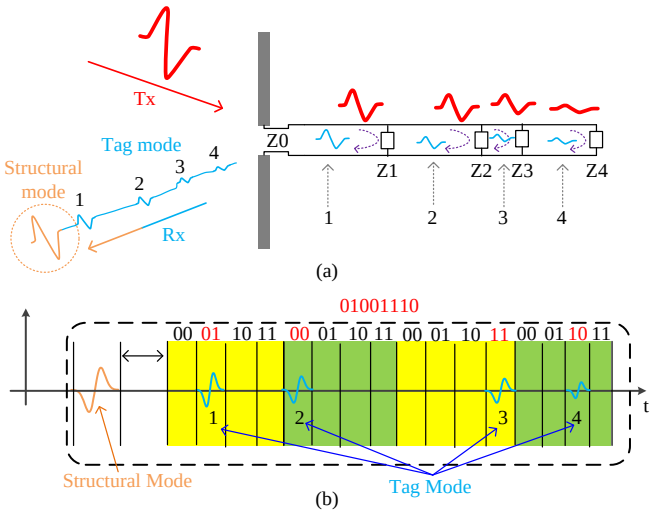


Fig. 2. a) UWB chipless RFID tag based on a time-domain approach. The tag has four impedance mismatches (Zi) that are the origin of the four main reflections back towards the reader. (b) The tag information is encoded in the delay between the structural mode and the four main reflections that form the tag (or antenna) mode.

III. Chipless RFID Tag: A Classification

Although this article focuses on chipless RFID reader, an introduction to chipless RFID tags is essential to simplify the understanding of reader design.

A chipless tag can be classified as either a time-domain or a frequency-domain tag [2]. The former tag is based on the reflectometry principle, and operates with the presence of a wideband antenna on the tag. A frequency-domain tag has the information encoded on its frequency signature [19-22]. For both categories, the wider is the frequency band employed, the higher the coding capacity.

A. UWB time-domain chipless RFID tag

In its simplest representation, an UWB time-domain chipless RFID tag is composed of one UWB antenna connected to a transmission line. Along the transmission line some impedance mismatches are imposed. A tag based on four reflections is shown in Fig 2 (a). Once interrogated with an UWB reader, the tag reflected signal can be analyzed in the time domain to find the location of the different reflections. The tag information is encoded in the position of those reflections. The tag response is composed of a structural mode and a tag (or antenna) mode. The former is due to the specular reflection of the tag. The latter is due to the tag behavior where the antenna is transferring energy to the transmission line, and where all the reflections due to impedance mismatches occur. The tag mode is the essential information in chipless technology, and is generally exploited to encode information. In the case of the time-domain chipless tag, the structural mode is also useful. It gives information about the tag distance, and is used to calculate the relative position of the reflections (impedance mismatches) to decode the tag ID. An example of this encoding technique is shown in Fig. 2 (b). The time domain is divided in four blocks, where each block corresponds to one reflection of the four that compose the tag mode (see Fig. 2 (a)). Based on the position of the reflections inside its area, a binary code is assigned. In Fig. 2 (b), the tag ID is 01001110 and a total number of 8 bits of information can thus be obtained.

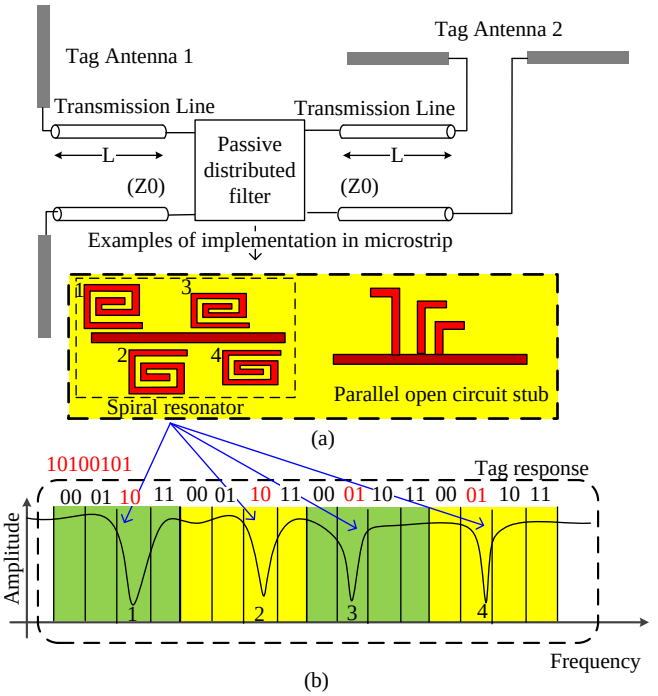


Fig. 3. Schematic of a frequency-domain UWB chipless RFID tag based on cross-polarization. Two examples of passive distributed filters are shown, one based on a spiral resonator [22], and the other one on parallel open circuit stubs [24].

Time-domain chipless tags exhibit a high read range, on the order of meters, at the expense of a low bit capacity (lower than 10 bits). This limitation is due to the dimension of the tag that increases with the bit capacity, i.e. the number of impedance mismatches. This family of chipless tag is more suitable for sensing applications rather than for identification

[23].

B. UWB frequency-domain chipless RFID tag

A UWB frequency-domain chipless RFID tag uses an approach based on its spectral response to encode information. The tag geometry is modified to account for specific amplitude and phase characteristics over the frequency band of interest. A well-known structure of such tag is composed of two UWB antennas (one for transmission and the other for reception), and between them a passive filter realized with distributed elements as shown in Fig. 3 (a).

If the passive distributed filter of Fig. 3 (a) is lossless, part of its input signal will be reflected, and part will be transmitted to the other antenna. The two antennas are linear polarized in a cross-polarization configuration (perpendicular direction). If a reading approach similar to Fig. 1 (UWB bi-static) is used to read the tag, the reader antennas have to be lined up with the tag antennas. The cross-polarization configuration measures only the part of the interrogating signal that crosses the tag filter, and therefore the part of the signal is encoded in the tag ID.

Two examples of passive filters compatible with microstrip technology are also represented in Fig. 3 (a). One is based on a microstrip line coupled with notch spiral resonators [22], and the other one is based on parallel open circuit stubs also coupled with microstrip line [24]. In the first solution each spiral filter (resonator) introduces a stop-band in the spectrum of the tag. The tag was designed for the band 3.1 - 7 GHz, and was realized in Taconic TLX-0 with dimensions of 8.8 cm × 6.5 cm. The information is encoded in the amplitude of the spectrum, and a 35 bit tag was proposed. By varying the dimensions of the spirals, their first resonant frequency mode will change. This principle is shown in Fig. 3 (b), where for simplicity the tag is represented with only four spirals.

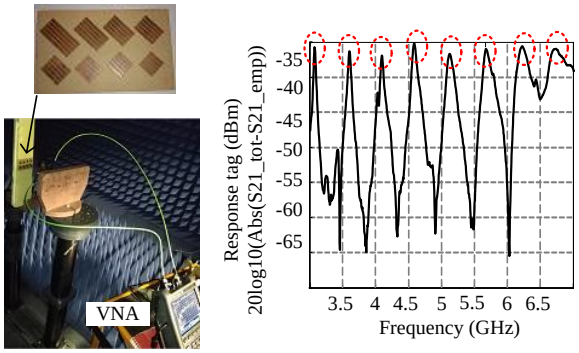


Fig. 4. Cross-polarization measurement of the frequency-domain UWB REP chipless RFID tag introduced in [29]. The measurement was performed in an anechoic environment. (a) Photograph of the test bench and the measured tag. The Agilent N9918A was used to measure the S-parameter (S21) with an averaging factor of 10. The tag was placed 15 cm from the dual-access dual polarization Satimo QH2000 antenna. In (b) the tag response where the positions of the eight resonant frequencies are underlined (red circles).

In [25] a frequency-domain chipless RFID tag that can operate in the UWB, and also in the frequency restricted industrial, scientific, and medical (ISM) bands, was designed. Only the filter section of the tag was implemented and characterized with laboratory equipment. Instead of focusing on the amplitude of the backscattered response, the authors encoded the tag ID on the filter phase response through the group delay. The filter was composed of cascaded commensurate C-sections where the length determines the frequency with a higher group delay variation. To retain a small filter dimension, a folding approach was proposed. The proposed architecture of a frequency-domain chipless RFID tag has a discrete bit capacity of around 40 bits. Last but not least, with this multilayered C-sections tag, a coding capacity of around 12 bits is estimated in the ISM bands. A reader in a bi-static configuration with two cross-polarized antennas is expected.

The RF Encoding Particle (REP) approach for chipless RFID technology has been introduced in [2, 26]. This approach allows for smaller tag dimensions. The tag structure is composed of several resonant scatterers (particles), in which the two tag antennas and filter functionalities (see Fig. 3 (a)) are enclosed [27- 28]. The REP approach is compatible with cross-polarization readings [29], and hybrid coding like frequency – magnitude coding which is used to increase significantly the tag encoding capacity [30]. The reading process of a depolarizing REP tag is shown in Fig 4 (a). The measurement was performed in anechoic environment with the tag introduced in [29] that was fabricated on Roger R04003 with a ground plane. The tag is based on eight scatterers where each is composed of five coupled rectangular patches, and has the first resonant mode frequency in between the band 3 - 7 GHz. The Agilent N9918A was used with the vector network analyzer (VNA) function as reader with 0 dBm of power emission in a cross-polarization configuration. The dual access Satimo QH2000 was employed with the tag placed at 15 cm. The background subtraction method was used for detection. Background subtraction consists of two measurements where the first is executed without the tag, and the second measurement with the tag. The two measurement results are then subtracted to remove the leakage of the antennas and the tag ID is retrieved. The measurement result using the bench in Fig. 4 (a) is shown in Fig. 4 (b). The eight resonant frequencies correspond to the circled eight apexes. The tag ID encoding is based on the position of those resonances in the spectrum. Next section introduces the reader technology.

IV. Chipless RFID Reader Introduction

A chipless tag can be viewed as a radar target possessing a specific and stationary signature. With chipless RFID technology, the remote reading of an identifier consists of analyzing the radar signature of the tag. That is, a chipless RFID reader is a type of radar, and clearly subject to regulations. To design low-cost tags that include a substantial amount of information (bit number), UWB regulations have to be taken into consideration [15, 16].

A chipless RFID reader can be designed either with a frequency-domain approach or with a time-domain approach. The frequency-domain approach expects the transmission of a harmonic which varies in frequency within the operative bandwidth of the tag. The reader architectures used in the literature are either based on stepped frequency continuous

wave (SFCW) or frequency modulated continuous wave (FMCW) architecture. A reader based on the time-domain approach transmits toward the tag a sub-nanosecond pulse and measures the backscattered signal from the tag, and is addressed with impulse radio UWB (IR-UWB). The hardware architecture is composed of a pulse generator and a time domain receiver. The frequency approach for the design of a reader is detailed with the next four sections.

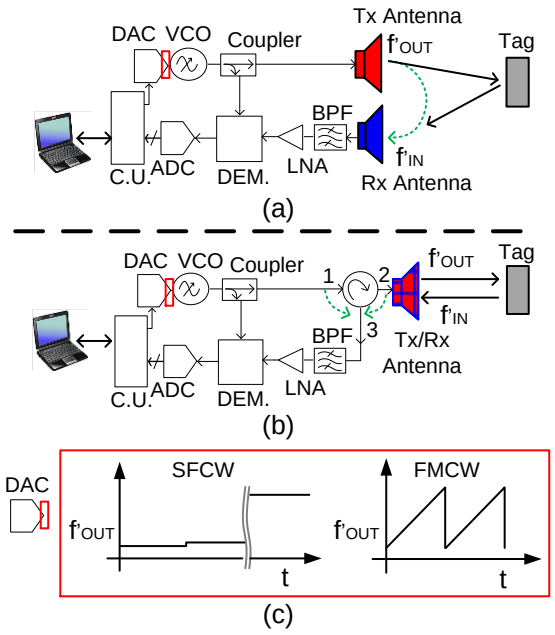


Fig. 5. Simplified schematic of a bi-static (a) and mono-static (b) UWB chipless RFID reader based on frequency approach. (c) VCO modulating signal in case of SFCW and FMCW approach.

V. Frequency-Domain Reader: A Classification

Two simplified schematics of a reader based either on SFCW or FMCW are shown in Fig 5. A bi-static configuration in Fig. 5 (a) is shown, where the transmitting and receiving antennas are distinct, and a mono-static configuration in Fig. 5 (b), where the same antenna is used for transmission and reception. Both topologies have a transmitter voltage-controlled oscillator (VCO) in transmission, whose center frequency is settled by a control unit (CU) through a dedicated digital to analog converter (DAC). A directional coupler at the VCO output is used as an input for the demodulator.

To design a reader, the designer must select between a bi-static or mono-static configuration. The choice depends on the topology of the tag that needs to be read and on the reader leakage. A mono-static architecture cannot read depolarizing based tags [29] because it would need transmitting and receiving antennas placed in cross-polarization orientation. The depolarizing principle takes advantage from the scarce cross-polarization attitude of the environment, which means lower clutter level at the reader input, and represents a robust implementation. The reader leakage is represented by the coupling between the two antennas (bi-static) and the imperfect isolation of the circulator (mono-static). The reader leakage is an important limitation in UWB chipless RFID applications (green arrows in Fig. 5), and so its reduction is vital to improve the reading performance [29].

In the SFCW approach the interrogating signal instantaneous frequency f'_{OUT} is approximately equal to the receiving signal instantaneous frequency f'_{IN}. This is due to the VCO modulating signal shown in Fig. 5(c) having a high sweep time. The information sought is the amplitude and phase difference between VCO output and the response of the tag for each frequency point in the band of interest.

In a FMCW approach f'_{OUT} is different from f'_{IN} due to the VCO modulating signal that has a low sweep time in the order of few ms as shown in Fig. 5(c). The next section focuses on the SFCW architecture.

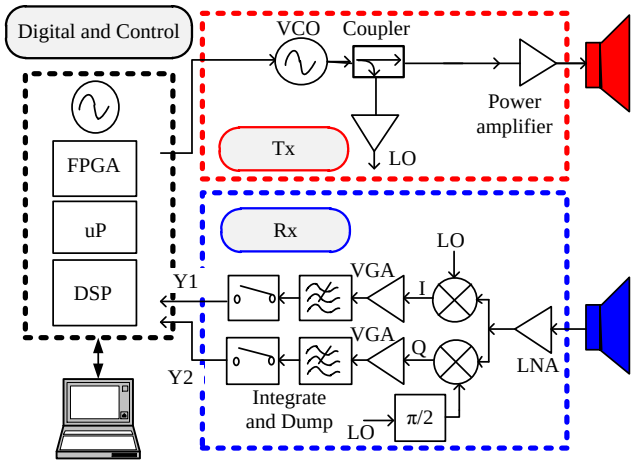


Fig. 6. UWB chipless RFID reader based on SFCW approach with I/Q demodulation scheme.

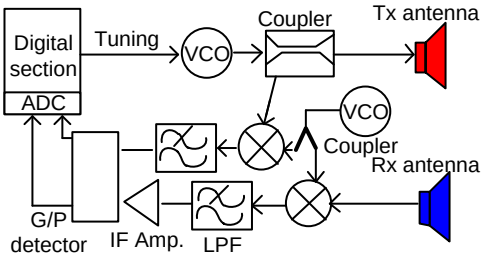


Fig. 7. FMCW Chipless RFID reader schematic block presented in [32]. A demodulation block based on heterodyne scheme is used. The estimated cost was of 4,500 €, where the antennas are not taken into account.

VI. SFCW Reader

The most employed chipless RFID reader based on the SFCW approach is the VNA as a result of its low noise bandwidth and high frequency resolution. With this solution, it is possible to easily read high bit capacity tags such as in [31]. A VNA is expected to cover the UWB between 3.1 – 10.6 GHz, as so is not a low cost reader solution for industrial production. A VNA can provide information about scattering parameters useful to retrieve the tag ID. Both frequency and time based tag can be read using scattering information. A tag can be read with high frequency resolution by setting the VNA with a low IF bandwidth. However, an increase of read time is expected.

The demodulation block of a SFCW reader can be based on an I/Q scheme to retrieve independently the phase and the

amplitude difference between the reader transmitting and receiving signal. The possible hardware architecture of a reader with such an approach is shown in Fig. 6. The reader of Fig. 6 represents a homodyne hardware configuration which unfortunately has low frequency and DC signals that exhibit dumping effects and pink noise.

A heterodyne configuration for a SFCW chipless RFID reader has been proposed in [32]. It utilizes a demodulation block composed of two coherent down-conversion blocks whose output goes through a gain-phase detector (AD8302 from Analog Devices). The schematic of the reader is shown in Fig. 7. The double down-conversion block implies the use of two mixers and VCOs. The reader bandwidth is between 5 - 9 GHz, and its hardware cost was of about 4,500 €. Experiments were performed in an anechoic environment with a 8-bit frequency-domain tag in the bandwidth 7 – 10.7 GHz. No read time information was given but is estimated to be tens of seconds if averaging was used.

To reduce the read time, readers based on the FMCW approach have been proposed to read both frequency and time domain based tag. The results have demonstrated the feasibility of this approach only with time-based tag as shown in the next section.

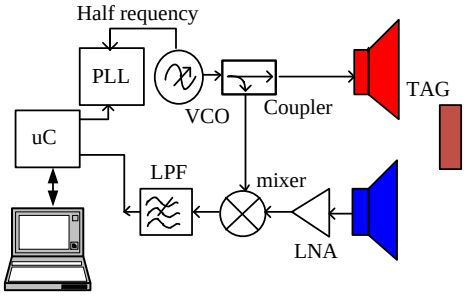


Fig. 8. FMCW chipless RFID reader schematic block presented in [33]. The reader is based on coherent demodulation and the hardware cost of 250 € is estimated (no antennas).

VII. FMCW READER

A FMCW reader is characterized in receive by the generation of a beat frequency after the demodulation block. This is a result of the difference between f'_{OUT} and f'_{IN}. The hardware architecture of a FMCW reader is similar to that of a FMCW radar.

A. Reading a Time-Domain Tag with a FMCW Reader

In [33] a compact and low cost chipless reader based on FMCW is proposed. It was designed for time-domain tag, and its hardware was optimized for reducing the total components cost. The proof-of-concept tag used was based on time domain reflectometry (TDR), with 16-phase shift keying (PSK) combined with 2-pulse position modulation (PPM) scheme reaching 20 bits of capacity. The tag dimension is 23.7 cm × 8.2 cm where the surface of the tag antenna is not taken into account. The reader central frequency operation is 7.825 GHz, with a bandwidth of 1.25 GHz, and a VCO sweep time duration of 10 ms.

The reader block schematic is shown in Fig. 8. The reader is based on coherent demodulation, and the transmitting signal instantaneous frequency is stabilized with a fractional synthesizer (PLL-based). As a consequence of the high power output of the VCO (10 dBm), and the high gain of the transmitting and receiving antennas (20 dBi), the reader does not need an output power amplifier. The demodulation block is composed of a mixer and a low pass filter (LPF). The read procedure is based on background subtraction plus a measurement with a calibrating tag. The tag has been optimized to work in co-polarization, where the reading was performed in an anechoic environment. The hardware implementation is low cost, and, not considering the antennas, has a cost estimate of about 250 €.

The reader hardware architecture in [33] is similar to that of a FMCW radar [34]. A time-domain UWB chipless RFID tag may be thought of as a different number of steady targets located in the direction of the reader [35]. Each target has a corresponding impedance mismatch (see Fig.2). This implies the absence of any Doppler effects that simplify the tag reading. The measured signal from the reader is composed of different beat frequencies, one for each impedance mismatch of the tag. The reader beat frequency resolution is proportional to the reader output bandwidth and to the VCO sweep frequency (1/sweep time). At higher bit capacity, a time-domain tag should be used with a reader with wider bandwidth and lower sweep time.

B. Reading a Frequency-Domain Tag with a FMCW Reader

The same architecture of [33], which is similar to a FMCW radar, can be used also to read a frequency-domain tag; this has been demonstrated in [36] where a bi-static architecture similar to [33] was used. The reader was designed to read frequency-domain tags with wide bandwidth (4 GHz), so as its realization cost is more important than the one in [33]. By not considering the antennas, the reader hardware component cost was estimated at about 650 €.

Reading a frequency-domain tag means retrieving the tag spectrum characteristic which is not something that can occur directly with a FMCW radar. From the analysis proposed in [36], the tag spectrum characteristics were embedded in the beat frequency signal amplitude and phase variations. A Hilbert transform was employed to retrieve the two components separately and a 9-bit frequency coded tag has been correctly read. However the analysis was based on significant approximations which can limit the scope of the reader technique. The influence of the antennas, the coupling, and the echoes from the environment were not considered. The read range was limited to a few centimeters. In [37], the design of a reader customized for dual polarized tags was presented. The hardware architecture was similar to [36] with the duplication of some circuit blocks.

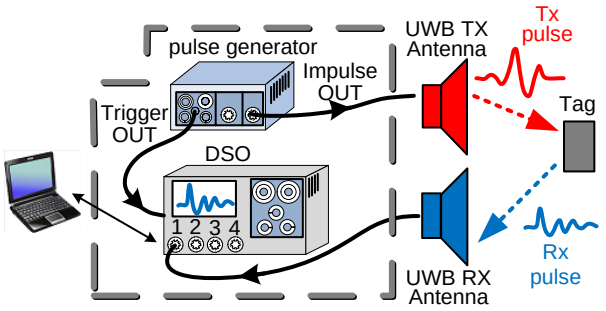


Fig. 9. IR-UWB chipless RFID reader realized with laboratory equipment. The pulse generator transmits an UWB pulse towards the tag (red signal), in turn the tag shapes the incoming signal and reflects it back to the reader (blue signal). The DSO can be triggered from the pulse generator. The computer identifies the tag through its signature (blue signal).

VIII. Frequency Domain Approach Read Time and Spectrum Characteristics

This section summarizes the chipless RFID reader based on the frequency domain approach with respect the read time and spectrum characteristic.

A. Read time

The main characteristics of the reader based on the frequency domain techniques are presented between Section V and VII are shown in Table 1. The reader proposed in [32] shows the wider bandwidth, while the one in [33] shows the lower output sweep time.

An important limitation of the frequency domain architecture applied to chipless technology is the excessive read time, which could easily reach several seconds. The sweep time of a read process is directly proportional to the bandwidth of the reader. In [36], the VCO sweep time is 500 ms with a bandwidth of 4 GHz. For an estimation of the row read time, all the post processing treatment, and an eventual data transfer to a central unit, should be added at the VCO sweep time. If a sweep averaging process is used, the read time could reach easily several tens of seconds. In [33] the sweep time is limited to 10 ms, providing a reader bandwidth of only 1.25 GHz, and the proposed reader could barely be employed for reading high bit capacity tags (frequency-domain tag).

TABLE 1
Frequency Domain Reader

Reader/ Parameter	*FMCW [33]*	*FMCW [36]*	*SFCW [32]*
Output sweep time (ms)	10	500	-
Power output (dBm)	10	30	15
Output -10 dB in UWB (GHz)	7.2 – 8.4	4 - 8	5 – 10.7

B. Spectrum characteristic

All the proposed reader solutions have to respect UWB emission regulations to be used in practical applications. In the USA the UWB regulations are enforced by the Federal Communications Commission (FCC), while in Europe by the European Telecommunications Standard Institute (ETSI) [15, 16]. The limits on power emission are restrictive, and the regulations distinguish between maximum mean power spectral density (PSD), and maximum peak power limits. Both limits are defined through the equivalent isotropic radiated power (EIRP). The maximum mean PSD presents a mask which differs between FCC and ETSI regulations, but between 3.1 GHz and 10.6 GHz the maximum level is -41.3 dBm/MHz. The maximum peak power limit also differs, and its maximum is 0 dBm over a bandwidth of 50 MHz.

A link-budget calculation for a SFCW reader, taking into account the regulations, can be formulated. The expression of the well-known radar equation is,

$$P_{rx} = \frac{EIRP_{tx} G_{rx} \lambda^2}{(4\pi)^3 R^4} \sigma, \quad (1)$$

where P_{rx} is the receiving power, $EIRP_{tx}$ is that one of the transmitting reader part. G_{rx} is the gain of the receiving antenna, R is the distance of the target, and σ is the target RCS. For a chipless RFID tag, σ can be in the order of -45 dBsm [26]. This value is referenced to a chipless RFID tag without ground plane with a structure based on REP approach. The gain of the reader antennas can be 20 dBi as in [33], and the tag distance R is on the order of 50 cm. Using these values in (1), the reader received power P_{rx} expressed in dBm (which is the unit of the $EIRP_{tx}$) is,

$$P_{rx}(dBm) = EIRP_{tx}(dBm) + 20\,dB - 45\,dBsm + 10\,log_{10}\left(\frac{\lambda^2 1m^2}{(4\pi)^3 R^4}\right), \quad (2)$$

where $1m^2$ was inserted to balance the expression once the RCS $\sigma(m^2)$ is expressed in dBsm. The maximum mean PSD is calculated over 1 ms for FCC regulations, and between 1 us and 1 ms for ETSI regulations with a bandwidth of 1 MHz. If a signal analyzer is used for the test, it needs to be set up in RMS-average power. Thus, for a SFCW chipless reader, if the sweep time is higher than 1 ms for each frequency point in the resolution of 1 MHz, from regulation, the transmitting signal will have a maximum $EIRP_{tx}$ of -41.3 dBm (FCC and ETSI maximum mean PSD mask). Substituting -41.3 dBm to (2) and supposing a frequency of 3.1 GHz (λ = 0.097m) the receiving power is,

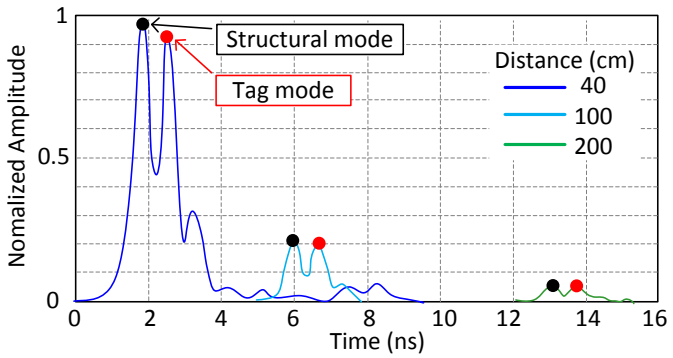
$$P_{rx} = EIRP_{tx} - 65\,dB = -106.3\,dBm. \quad (3)$$

The sensitivity of the SFCW chipless reader has to be lower than -106.3 dBm to read a chipless tag with a RCS of -45 dBsm [26]. This value of sensitivity is hard to find especially for low cost wideband systems. In addition the high gain of the receiving antennas (20 dBi) is incompatible with low cost wideband antennas realizations, thus the reader sensitivity should be even higher.

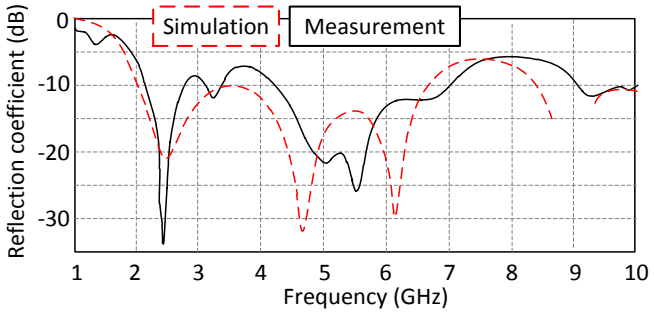
To increase the receive power (P_{rx}), the reader should have a short sweep time, which is the case for a FMCW reader. This will decrease the measured maximum mean PSD over the specified interval of time for 1 MHz (1 ms for FCC, 1 us -1 ms for ETSI). Other ways of increasing the transmit power to the tag are compression power methods such as pulsed frequency modulation (PFM); however, currently, no chipless RFID

reader based on FMCW have been proposed with such feature.

Different reader architectures based on IR-UWB have been proposed in the literature. Those solutions include commercial IR-UWB radars and custom designed readers. The next sections are focusing on IR-UWB architecture.



(a)



(b)

Fig. 10 (a) Normalized time-domain response of the tag at several tag-reader distances in a practical environment. The background subtraction technique and CWT were used. (b) Microstrip-fed UWB monopole tag measurement and simulation results of the reflection coefficient. Actual figures in [39].

IX. IR-UWB Chipless Reader

A chipless reading system based on the IR-UWB approach is shown in Fig. 9. This system makes use of typical laboratory equipment, where a pulse generator triggers the digital signal oscilloscope (DSO) and transmits a sub-nanosecond UWB signal toward the tag. The DSO measures the backscattered signal from the environment in a bi-static configuration. Alternatively, a circulator can be used to obtain a mono-static reader.

The IR-UWB configuration transmits an interrogating signal towards the tag, with the maximum possible instantaneous power since a sub-nanosecond UWB pulse is transmitted, and the maximum mean PSD over MHz (claimed in the regulations), is calculated over a period of time much higher than 1 ns (1 ms for FCC, 1 ms - 1 us for ETSI). Thus, the measured maximum mean PSD will be lower compared to a frequency domain approach. The UWB instantaneous pulse power is limited by the mask of maximum peak power, which is less restrictive than the maximum mean PSD mask.

A reader based on IR-UWB is intrinsically faster than one based on the frequency domain approach because no frequency sweep in transmission is needed. Conversely, a SFCW reader may have a better frequency resolution by adjusting the IF bandwidth. A reader based on IR-UWB has a higher noise bandwidth due to its wide-band receiver, which is translated into high sampling noise. The sampling noise of an IR-UWB reader is reviewed in section XIII.

Both, time and frequency based tags, once receiving the UWB pulse from the reader, respond with a signal that lasts several nanoseconds. Because of the use of sub-nanosecond signals, the DSO needs to have a wide input analog bandwidth and a high sampling rate. From a practical point of view, it is not feasible to use expensive laboratory equipment for chipless applications such as the ones presented in Fig. 9.

In an IR-UWB approach, a short UWB pulse signal is transmitted towards the tag. The measured tag response can be seen as the tag impulse response estimate [29]. The tag impulse response can be converted to the frequency domain to have the same information measured by a VNA. The variation of the gain of the UWB antennas with the frequency is generally not an issue in IR-UWB readers. In addition, the UWB antennas employed have a gain variation inside the UWB band of only few dB. If the tag has a very low RCS or a magnitude encoding technique is used, a reading based on a calibration process can be executed to take into account the variation of the antenna's gain with the frequency [29, 30]. The next section focuses on commercial IR-UWB radars used as chipless RFID reader.

TABLE 2
IR-UWB Commercial Radar and Reader

Model/ Parameter	*Novelda NVA-640*	*PulsON P400MRM*	*Geozondas GZ6EVK*	*Module [49]*	*Module [47]*
Principle of operation	Equiv. time (CTBV)	-	Equiv. time	Equiv. time	Equiv. time
Time resolution (ps)	From 26	30	From 12.5	10	10
Output -10 dB in UWB (GHz)	3 – 6	3.1 – 5.3	4 – 6 (-6 dB)	-	3 – 7
Input Bandwidth (GHz)	3 – 6	3.1 – 5.3	0.1 - 6	0.0045 - 3	1 - 8
Output Volt over 50 Ω (V)	0.420	-	5	5.6	2

X. IR-UWB Chipless Reader: Radar

Commercial IR-UWB radars can be used to read chipless tags [23, 29, 38-40]. These radars are able to transmit and measure sub-nanosecond UWB pulses, and a wideband analog to digital converter (ADC) is used in receive. Their cost is on the order of a few thousand Euros. The main characteristics of the three radars used in literature as UWB chipless RFID readers are summarized in Table 2.

In [38], a Novelda NVA A640 development kit IR-UWB radar was used in a bi-static configuration with two tapered slot Vivaldi antennas to read time-domain tags at a distance of up to 180 cm. In [29] the same radar model was successfully employed as a reader for frequency-domain tags placed 20 cm from the antenna using a depolarizing technique. In [23], a Time Domain PulsON P400MRM was used to read a time

coded tag used as concrete quality sensor. In [40], time coded tags were read up to 2 m with the Geozondas GZ6EV K IR-UWB radar evaluation kit, which is composed of the GZ6E sampler converter and the pulse generator GZ1120ME - 50EV. The radar solutions proposed as readers offer good performance; however they are only designed for localization and/or detection applications. In chipless RFID technology, as previously explained, a frequency domain tag is composed of several resonators to encode its ID. As shown in Fig. 4, resonators with the highest quality factor are the most suitable for encoding a large quantity of information. In practice, this implies a tag response duration of several tens of nanoseconds [30]. It is why a reader with a minimized jitter (as shown in section XIII and in [41]) and dedicated post processing are needed to decode the tag ID. In localization and detection applications, the target response lasts for only few nanoseconds (which correspond to the structural mode of the target), and the signal is analyzed with the use of optimal filters. Thus the minimization of the radar jitter in that case is not the most significant constraint. In addition these radars represent a black box solution that cannot comply with specific chipless requirements such as orientation independent tag reading [42]. Moreover their cost is still significant to represent a practical commercial solution.

An IR-UWB radar allows for a high read range because the transmitting energy is concentrated in a short period of time and so a high instantaneous power is transmitted towards the tag. A typical bi-static co-polarization measurement result of a time-domain chipless tag, at several distances up to 2 m in practical environment [39], is shown in Fig. 10 (a). The detection method was based on the background subtraction and used a continuous wavelet transform (CWT) in post-processing [40]. From Fig. 10 (a), both the structural and tag modes are detected. The tag consists of a microstrip-fed UWB monopole [43] fabricated on Rogers RO4003C substrate. The tag is composed of only one reflector which is an open-circuit at the ending point of the microstrip line. Its measured and simulated reflection coefficient are shown in Fig. 10 (b).

Most of commercial radar solutions used to read chipless tags are based on an equivalent time domain approach to help reduce the hardware realization cost as shown in the next section.

XI. Sequential Equivalent Time Approach

An IR-UWB chipless RFID reader can be designed for performing measurement in equivalent time (see Fig. 11), which allows for the realization of a low cost system with wide input bandwidth. The reading procedure can be executed with an averaging factor, by repeating the tag interrogation sequence. This can be useful in improving the signal-to-noise ratio (SNR) and to avoid outside disturbances from other EM signals [44].

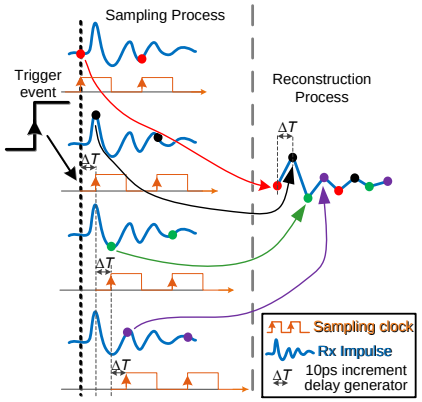


Fig. 11. Sequential equivalent time principle. The signal of interest (Rx pulse) is sampled with a low sampling frequency (Sampling clock), that does not respect the Nyquist Shannon theorem. In this way only a few points of the response of the tag are acquired. Numerous pulses are transmitted toward the tag, and for each response the sampling clock is shifted with steps of few picoseconds (ΔT).

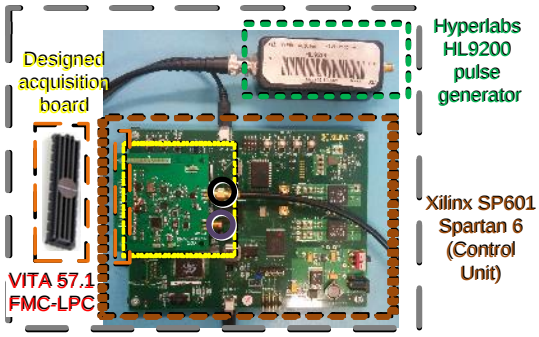


Fig. 12. Architecture of the reader proposed in [47]. The reader is composed of three parts: a pulse generator (UWB), an acquisition board and a CU, the Spartan 6 sp601 evaluation board. The system is multi-clock and both the sampling clock and the trigger for the pulse generator are synchronized with the low jitter clock generator on the acquisition board. (a) Block diagram. (b) Photograph of the reader.

In the sequential equivalent time algorithm, the reader transmits the same interrogating signal (a UWB pulse) toward the tag at intervals of time equal to the period of the pulse repetition frequency (PRF). Subsequently, the reader samples each backscattered signal, i.e. the response from the tag plus the environment contribution. The reader sampling frequency is much lower than the one required in the real time approach (Nyquist-Shannon sampling theorem). The sequential equivalent time algorithm is summarized in Fig. 11. The left-side shows the sampling process, and the right-side the tag response reconstruction. During the sampling process the reader acquires each response of the tag (Rx pulse), with a low sampling frequency (sampling clock); thus, the reader acquires only few points for each tag response. In the sampling process the sampling clock is shifted of few picoseconds ΔT between the different acquisitions, as shown in Fig. 11. This is needed to sample the tag response with a time resolution equal to ΔT. Each acquisition starts after a trigger event, which is usually generated by the reader control unit. In the reconstruction process, all the samples are recombined to obtain the complete response of the tag. The equivalent sampling frequency of the system is 1/ΔT. This approach allows the reader to emulate a high speed sampling system.

In the real time approach, a signal in the UWB spectrum (3.1 - 10.6 GHz) needs a theoretical minimum sampling frequency of 21.2 GSa/s, from the Nyquist-Shannon sampling theorem, to be acquired. In practice the sampling frequency should be higher to reduce the aliasing effects that reduce the SNR. From [45] the minimum bandwidth and the sampling rate of a DSO used to read the response of the UWB chipless tags with an accuracy of 3% should be 11.2 GHz and 44.8 GSa/s respectively. The pulse transmitted to the tag is assumed to have a rise/fall time (20 % - 80 %) of 50 ps.

In real time IR-UWB radars the UWB analog to digital converter (ADC) is the most expensive piece of hardware. Its cost can be reduced if the reader is designed around the sequential equivalent time principle. A low cost digitally controlled signal delay generator can be used to perform the shifting ΔT of the sampling clock (Fig. 11), and a low speed ADC, with or without a UWB sample and hold amplifier, can be used to convert the different acquiring points. In the next section, the design of an IR-UWB chipless reader based on sequential equivalent time is reviewed.

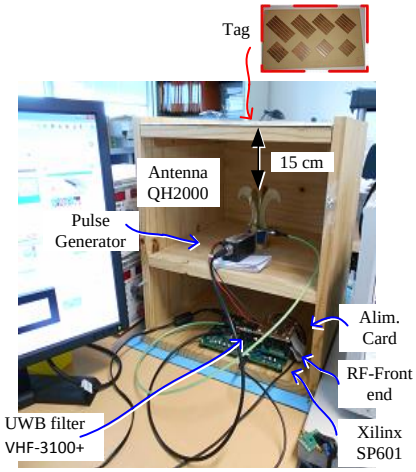


Fig. 13. Measurement bench for UWB frequency-based tags in practical environment for the reader introduced in [47] for a non line-of-sight condition.

XII. IR-UWB Chipless Reader: Hardware Architecture

The authors proposed two different readers based on IR-UWB and sequential equivalent time approach in [46, 47]. A photograph of the reader in [47] is shown in Fig. 12. The reader is composed of three main parts: the triggerable HL9200 pulse generator from Hyperlabs, the Spartan 6 FPGA SP601 evaluation board from Xilinx, and a custom designed mixed-signal acquisition board.

For the receiver the mixed-signal board is composed of a broad-band LNA, followed by a UWB sample and hold amplifier (the sampler), and a low cost ADC. The sampler is a commercial-off-the-shelf (COTS) component and, for UWB signals, its cost is less than 800 €. This component is able to sample an UWB (3.1 - 10.6 GHz) signal with a low sampling clock so as to give the time at the ADC, which is low speed, to digitally convert the sample.

The physical sampling frequency of the readers is 125 MHz, corresponding to a sampling period of about 8 ns. The read time as expected is reduced and is on the order of few ms with a minimum of 6 ms. This is a huge improvement compared to the architectures based on SFCW and FMCW (Frequency approach). The reader output bandwidth is of 3 – 7 GHz, and its hardware component cost (not considering the antennas) is estimated at 1,800 €.

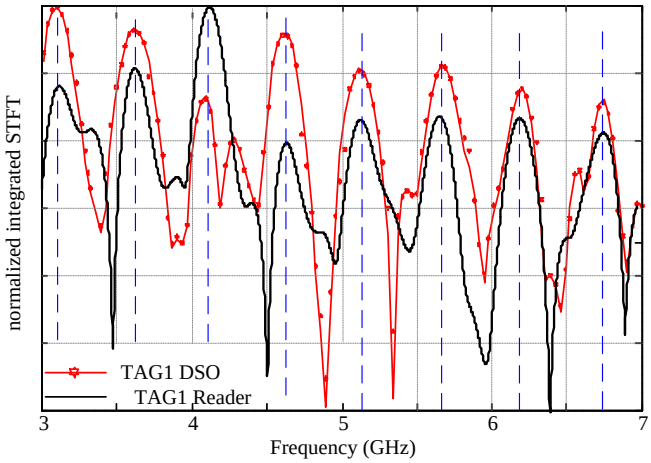


Fig. 14. Measurement results of the UWB frequency-domain tags in Fig. 4 and introduced in [29] with the reader presented in Fig. 13 (black line), and with the DSO (red line). As expected in both cases, the lines indicate identical resonant frequencies.

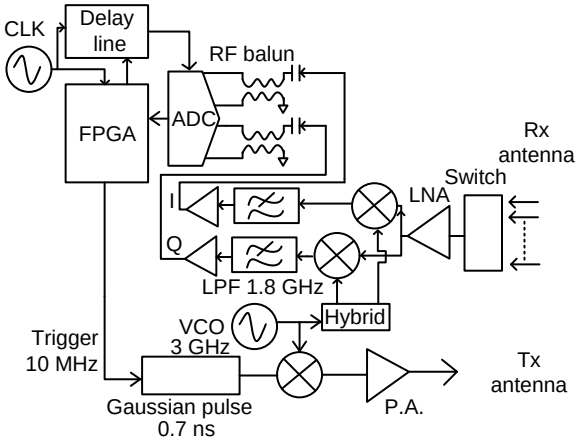


Fig. 15. Schematic of the radar presented in [49]. The radar is based on a coherent IQ demodulation scheme. The transmitting pulse has a pulse-width of 0.7 ns. The acquisition block is based on the sequential equivalent time algorithm.

The reader in [47] was used to read the same frequency-domain tag shown in Fig. 4 and introduced in [29]. The measurement bench is shown in Fig. 13. The reading was done in a practical environment where the tag was placed on top of a square wood surface of few millimeters thickness with the antenna below. This setup creates a reading process in a non-line-of-sight condition. However, the post processing was optimized with a short time Fourier transform (STFT) [48] to alleviate the effects of clutter and to manage the lower receive power with respect to a line-of-sight reading condition. The measurement was also performed with a DSO Agilent as reference system. The measurement results for the reader and the DSO are shown in Fig. 14. Both reading systems show the eight resonant frequencies of the tag.

To the best of our knowledge, the readers introduced in [46, 47] represent the only examples of custom chipless RFID reader based on the IR-UWB approach. In the literature, it is possible to find radar with similar hardware architectures of [46, 47], but designed for different applications. An imaging radar also working with sequential equivalent time is presented in [49]. A block diagram is shown in Fig. 15. The transmitter uses a pulse generator (Gaussian pulse) with a pulse-width of 0.7 ns, which is up-converted to approximately 3 GHz. For the receiver, a coherent IQ demodulation block is used. A FPGA (Virtex-5), in conjunction with a digitally controlled variable delay line, are employed to perform the sequential equivalent time algorithm (see Fig. 11). The input bandwidth of the system is limited to 3 GHz (7 GHz in [47]) and the overall jitter is of about 40 ps (2.3 ps in [47]). This difference in performance between [49] and [47] arises from the particular applications. The better performance of [47] underlines the difficulty behind the design of a reader for chipless technology. The characteristics of most of the proposed chipless tags in the literature are demonstrated with high performance test instruments. To help the deployment of chipless technology, the tag designs proposed in the literature should be read with low cost reader solutions. The main characteristics of [47, 49] are shown in Table 2. As previously explained, the sampling noise for an IR-UWB reader can be significant and will be discussed in the next section.

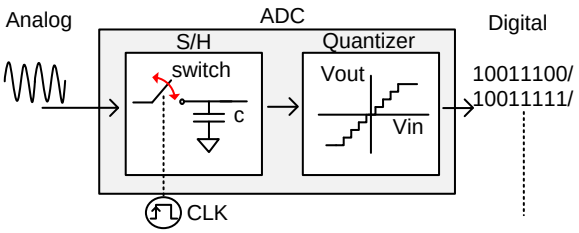


Fig. 16. ADC block schematic composed of a sample and hold block in series with a quantizer. The former is responsible for sampling noise and the latter for quantization noise.

XIII. Sampling Noise

All the analog to digital conversion processes degrade the SNR. There are different sources of noise that can play a major or minor role, depending of the ADC characteristics and the input signal in terms of voltage range and frequency contents.

An ADC can be modeled as a sample and hold (S/H) block in series with a quantizer as shown in Fig. 16. The S/H is responsible for the sampling the analog input; it is ideally composed of a switch controlled by a clock and a capacitor. The switch opens and closes according to the rising and falling clock edges, respectively. When the switch is closed, the capacitor tracks the analog input signal; when the switch opens the capacitor value is equal to the input at the rising clock event (sampling). This value is kept constant (holding) until the switch is closed again. During the holding period, the capacitor voltage is converted to digital symbols by the quantizer, whose input/output characteristic can be represented with a staircase function (see Fig. 16).

The degradation of SNR by an ADC is due to the error introduced by the sampling and quantization processes. The first is caused by the uncertainty of the sampling event, which is correlated with the sampling clock jitter and ADC aperture time uncertainty. The second is due to the input/output characteristic of the quantizer, which is a nonlinear function and therefore introduces higher order noise. These errors are sampling noise (S/H) and quantization noise (quantizer) respectively.

In case of SFCW and FMCW based chipless readers, the useful ADC input signal is low frequency, and the ADC degrades the SNR with quantization effects. An ideal ADC with a staircase quantizer has a maximum SNR output of,

$$SNR = 6.02\, N_{bit} + 1.76\, dB, \tag{4}$$

where N_{bit} is the number of bits of the ADC. This equation (4) assumes: 1) a sinusoidal input signal with an excursion equal to the ADC input full-scale, 2) the ratio between the ADC clock and the ADC input periods expressed with an irrational ratio, and 3) the clock frequency is of about the Nyquist rate [50]. From (4), the SNR can be improved by increasing N_{bit} and by exploiting techniques such as oversampling and digital filter implementations. For the SFCW and FMCW readers the ADC noise can be easily reduced. These readers are more affected by VCO phase noise, leakage, and pink noise.

The input of the ADC of an IR-UWB chipless reader is an UWB signal. Beside the quantization noise, the sampling noise is also significant. For IR-UWB equation (4) has to be reformulated. The reader ADC input is composed of the coupling between the transmitting and the receiving antennas, and the structural and the tag mode. The tag ID is encoded in the tag mode part of the ADC input signal (in the case of frequency-domain tag), the lowest energy part of the signal. The effective number of the ADC bits used for the tag mode will be lower than N_{bit}. To reduce the quantization noise, it is important to choose an ADC with a high number of bits, and to amplify the tag mode signal ideally to match the ADC input full scale range. Oversampling and the digital filtering implementations in post processing can also be useful to reduce the quantization noise. A logarithmic ADC can represent a good solution for the low tag mode power. This is employed in the Novelda IR-UWB NVA R640 radar development kit [51] used in [29, 38].

The sampling noise depends on the ADC characteristics, the ADC clock jitter, and the input frequency contents. For a low input frequency signal, it can be negligible, as in case of SFCW or FMCW based chipless readers. For the IR-UWB chipless reader approach, the noise contributions are more complicated. Sampling noise has to be taken into account and its effects can be notable. To study the sampling noise, a sinusoidal ADC input can be considered that is the result of the stationary process:

$$V_{in}(t) = \sin(\omega t + \varphi). \tag{5}$$

where φ is a random variable uniformly distributed between $[-\pi, \pi]$ (this process is parametric, stationary and ergodic).

This process, once through the S/H block of the ADC (see Fig. 16) becomes:

$$V(K) = \sin(\omega(TK + \gamma) + \varphi). \quad (6)$$

From the central limit theorem, γ is a Gaussian random variable with zero-mean that takes into account the jitter noise of the ADC clock, combined with the ADC aperture uncertainty that generally has a minimum influence. T is the ADC clock period. The introduced error by γ can be approximated with,

$$N(K) = cos(\omega(TK) + \phi)\,\omega\gamma. \quad (7)$$

As this process is stationary (the two random variables ϕ and γ are independent) it can be demonstrated that its mean value and autocorrelation are invariant with respect to timing translations. The ratio between the power of the process in (5) and (7) is equal to the SNR:

$$SNR = -10log_{10}(\omega^2\sigma_t^2), \quad (8)$$

where σ_t^2 is the variance of γ, which is approximated equal to the variance of ADC clock jitter. From (8) the SNR exhibits a decay of 20dB/dec with respect to input signal frequency. In the case of the UWB signal (IR-UWB chipless reader) the SNR has been calculated in [52] and is equal to,

$$SNR = -10log_{10}[4\pi^2\sigma_t^2(f_0^2 + \tfrac{BW}{12})], \quad (9)$$

where f_0 is the central frequency of the UWB signal and BW is its -3dB bandwidth. If f_0^2 > 10BW, the term BW/12 in (9) can be neglected. In this analysis only the jitter of the ADC clock has been considered, however in the case of an IR-UWB chipless reader, the pulse generator is triggered by a signal (such as a low frequency clock) which is also affected by jitter. Its variance can be added to σ_t^2 if both phenomenon are considered uncorrelated. Equation (9) is valid for both real time and equivalent time hardware implementations when is ensured the reproducibility of the transmitting signal.

The jitter that affects a signal is directly correlated with the signal integrity. Signal jitter is caused by different noise sources such as power supply variations, thermal noise, interference between nearby circuits and loading mismatching. Thus, in an IR-UWB chipless reader, the hardware architecture, the layout of the mixed-signal acquisition board and the choice of the components need to be optimized to reduce the jitter of the system. For the FCMW chipless reader, the error induced by the ADC can be neglected, since the VCO phase noise reduces the overall reader performance decreasing its frequency resolution.

The proposed noise analysis does not take into account additional disturbing signals at the input of the ADC. This may be the case of WiFi communications at 5 GHz. For real time implementations, this contribution may be filtered out with a digital notch filter in post processing. For a sequential equivalent time implementation, that source of noise is distributed in all the bandwidth of interest (3.1 – 10.6 GHz) and once acquired, cannot be filtered out. Thus, either a notch filter device can be inserted at the reader input port, or the reader averaging factor can be increased to reduce the effects of the disturbing signals.

XIV. CONCLUSION

A chipless RFID reader can be designed around different hardware architectures, in the frequency domain and time domain. In the frequency domain SFCW and FMCW architectures are widely employed. A SFCW reader allows for high frequency resolution and lower input noise bandwidth as a result of the IF bandwidth. However its read time may exceeds 1 s and its UWB emissions are strongly limited by FCC and ETSI regulations. An FMCW approach shows reduced read time, is less limited by UWB regulations, and its feasibility as a chipless reader has been demonstrated for time-based tags only. An IR-UWB approach is useful for a reduced read time and is less affected by UWB emission restrictions. The major drawbacks are represented by the sampling noise due to the high input noise bandwidth, and potentially low frequency resolution. Improving the performance and functionality of the reader helps to reduce the tag realization complexity; thereby low cost tags could be realized on substrates made of paper to compete with barcode based tags.

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