



HAL
open science

RF Power-Handling Performance for Direct Actuation of GeTe Switches

Alexandre Leon, Bruno Reig, Etienne Perret, Florence Podevin, Damien Saint-Patrice, Vincent Puyal, Jose Lugo-Alvarez, Philippe Ferrari

► **To cite this version:**

Alexandre Leon, Bruno Reig, Etienne Perret, Florence Podevin, Damien Saint-Patrice, et al.. RF Power-Handling Performance for Direct Actuation of GeTe Switches. *IEEE Transactions on Microwave Theory and Techniques*, 2019, pp.1-14. 10.1109/TMTT.2019.2946145 . hal-02429379

HAL Id: hal-02429379

<https://hal.science/hal-02429379v1>

Submitted on 8 Jul 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

RF Power-Handling Performance for Direct Actuation of GeTe Switches

A. Léon, *Member, IEEE*, B. Reig, E. Perret, *Senior Member, IEEE*, F. Podevin, *Member, IEEE*, D. Saint-Patrice, V. Puyal, J. Lugo-Alvarez, P. Ferrari, *Senior Member, IEEE*

Abstract—The study presented in this paper concerns Telluride Germanium Phase Change Material based switches, actuated via direct heating and arranged through two configurations: series or shunt. It is concluded that direct heating is a performing solution for amorphisation, preventing from heater ageing. Then, the switches configurations are compared in terms of RF performance, power handling and linearity. Some design rules are derived from empirical data, consolidated with thermal simulations. It is expected that either in series or shunt configuration, a large, thick and short GeTe in an optimized capacitive environment is preferable, for higher isolation in shunt configuration and for lower insertion loss in series one. The Figure-of-Merit, as cut-off frequency, is 11 and 21 THz for shunt and series configurations, respectively. In terms of power handling of amorphous GeTe, results confirm the existence of a threshold voltage leading to better handling for longer switches, in both configurations. For crystalline GeTe, design rules that link the maximum current through the switch before failure, to geometry, are derived for the very first time. Current is proportional to width, to the square root of thickness, and inversely proportional to length. The shunt configuration presented herein holds 31 dBm at ON-state and more than 35 dBm at OFF-state while the series configuration holds 27 dBm at ON-state and 32 dBm at OFF-state. For power handling, there exists a balance between series and shunt with a ratio of 4 in crystalline phase and of 0.25 in amorphous phase.

Index Terms—Direct heating, GeTe, phase-change material, power-handling, RF switches.

I. INTRODUCTION

WITH the evolution of communication means worldwide, it is necessary to develop applications, circuits and bottom level components that can address the future needs for the next generations of mobile networks. Within those networks, at the front-end modules (FEM) level, switches play a fundamental role for reconfigurability. This role is even strengthened with the incoming of massive multiple input multiple output (MIMO) systems and the principle of aggregation that appeared with 4G and that will be strengthened for next 5G. Switches will also be a must for low-consumption passive beam-forming systems based on phase shifters, for 5G but also for automotive radars and more generally for any point-

to-point communications.

In that context, Phase Change Material (PCM) switches constitute a recent and reliable approach to challenge MEMS, MOS transistors, PIN diodes or even a more recent technology that is based on Conductive-Bridge (CB). From a circuit point of view, performing switches need low insertion loss (IL), outlined by a low ON-state resistance R_{ON} , and high isolation, outlined by a low OFF-state capacitance C_{OFF} . As a trade-off, the cut-off frequency $1/(2\pi R_{ON}C_{OFF})$ is the major Figure-of-Merit (FoM) for switches:

$$FoM = 1/(2\pi R_{OFF}C_{ON}) \quad (1)$$

but switching time, power consumption, DC bias voltage, reliability, and cost also play a significant role.

CMOS and BiCMOS technologies are limited by their ON-state resistance R_{ON} , which leads to pretty high insertion loss. A switch achieving a cutoff frequency of 1.4 THz ($R_{ON} = 0.5 \Omega$) was presented in [1] in a SOI technology. However, the low R_{ON} value was achieved at the expense of the surface on the die, with a width equal to 1 mm, leading to high cost. JFET [2], MOSFET [3], HEMT [4] or SOS [5] lead to comparable performance. MEMS switches are very good candidates for low insertion loss with a value of 0.25 dB at 40 GHz [6] and OFF-state capacitance lower than 10 fF, but their reliability and packaging is time consuming as it had already been stated in 2003, [7]. CB technology, inspired from CBRAM, constitutes a promising technology as mentioned in [8]. For example, in [9], at low-RF, a very simple PCB-based process proved interesting performance at very low-cost. In [10], potentially integrated nanoscale memsresistive switches offered incredibly high electrical performance from RF to mm-waves, under low energy (\sim pJ) and reaching a FoM of 35 THz. However, the nanoscale filament was created through an air gap and the question of maintaining a reliable air-gap in an integrated silicon process still remains. Also, the presence of gold is up to now an issue. Nanoscale memsresistive switch constitutes a serious competitor to PCM but the technology easiness seems to be in favor of the latter.

PCM have been studied in many research groups, and several publications have already shown that their electrical performance compete and often overcome the current state-of-

Manuscript received ...

A. Leon, B. Reig, D. Saint-Patrice, V. Puyal, J. Lugo-Alvarez are with Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France. E. Perret is with Univ. Grenoble Alpes, Grenoble INP, LCIS, F-26000 Valence, France and Institut

Universitaire de France, 75005 Paris, France. F. Podevin is with Univ. Grenoble Alpes, Grenoble INP, RFIC-Lab, F-38031 Grenoble, France. P. Ferrari is with Univ. Grenoble Alpes, RFIC-Lab, F-38031 Grenoble, France.

the-art of the devices described above. Several PCM as Germanium Telluride (GeTe) [11]-[14], Germanium Antimony Telluride (GeSbTe) [15], and Germanium Antimonide (GeSb) [16] have been developed.

Basically, the electrical switching consists in a change of the structural phase of the material obtained through a gradient of temperature. Based on the structure represented in Fig. 1, heating may be induced by a direct contact to the RF paths, as in [12] where an electrical signal flows through the signal strip disrupted by the presence of the PCM. As a consequence, a DC current flow can be used to control the switch state.

Heating may also be indirect. In that case, electrical signal heats an intermediate highly resistive material that transfers its calorific energy to PCM via Joule effect [11]. In both cases, phase change induces an important resistive transition in the material. Its electric conductivity increases from less than 10 S/m, in its amorphous phase (high resistivity phase), to more than 100 kS/m in its crystalline phase (low resistivity phase). Usually, the resistance ratio between ON- and OFF- states ranges around 10^5 that is high enough to perform low insertion loss at ON-state and high isolation at OFF-state when PCM has been properly dimensioned.

From a technological point-of-view, there is more complexity in the design of indirectly heated PCMs as their implementation require an intermediate material and an extra metallic layer (heater) to convey electrical excitation. What's more an early ageing of the heater is usually observed, due to the high temperature necessary for changing PCM from one phase to another. Therefore, their reliability still has to be proven.

Direct heating is much simpler to implement but was not thoroughly studied up to know. In particular, a high RF power signal may have a negative impact on the physical PCM structure. This could be a limitation in some applications and power-handling as well as self-activation must be studied for direct heating. Works on direct heating PCM switches, [12], are not numerous and, to the authors' knowledge, power handling is never addressed. More generally, whatever heating is, no power handling study discusses about the influence of GeTe geometry (width, length and thickness of GeTe), and there is no comparison between series and shunt configurations. In that context, this paper claims, for the very first time, a geometrically based parametrical study on power handling confirmed by qualitative multi-physics thermal simulations, thus enabling to 1) propose design rules for PCM switches, 2) evaluate the performance of direct heating, 3) compare two different configurations of switches, series or shunt.

The paper is organized as follows. In part II, a brief technology description presents a new generation of GeTe switches, as compared to the previous ones presented by the authors in [17]. Two configurations are introduced, series and shunt. The direct electrical actuation is discussed. Then, in part III, RF small signal analysis compares the two configurations for both switching states, and in terms of FoM. Part IV is dedicated to large signal analysis. Power handling is studied, still for both configurations, with its parametrical analysis confirmed by thermal simulations. Linearity is also analyzed.

Part V compares results to the state-of-art before concluding in part VI with a discussion concerning design choices.

II. GERMANIUM TELLURIDE BASED SWITCH

A. Technology Description

The switch layout and process stack are described in Fig. 1. The flow developed so far fulfills two requirements: standard CMOS process compatibility and switching electrical performance. First, compatibility of the materials and techniques with a standard CMOS back-end-of-line (BEOL) has been considered for further integration. For instance, neither platinum, nor gold were used, but only aluminum and standard RF silicon materials. Second, different technological stacks were tested to enhance the PCM switching electrical performance. As shown in Fig. 1c, the PCM was contacted backside using metallic microstrip lines that optimize electrical contact. Following a strict process flow, aluminum feeding microstrip lines for backside contact were first patterned on a high-resistivity silicon (HR-silicon) wafer, after thermal oxidation. Next, GeTe was deposited in a co-pulverization step and patterned with dry etching (RIE). This process allows defining uniform patterns with widths as low as 250 nm. Then a 100-nm thick PECVD SiN dielectric was deposited to cover and protect the GeTe. A second level of metallic microstrip lines, etched with a standardized RIE process, was deposited to contact the first one. Finally, PECVD SiO₂ was deposited for passivation and test pads were opened by RIE.

Fig. 1 focuses on two configurations of the GeTe either in series (Fig. 1a) or in shunt with two devices in parallel (Fig. 1b). The close-up micrograph of the series switch in ON-state (Fig. 1a) shows the light color of the crystalline GeTe. Fig. 1c represents the technological stack.

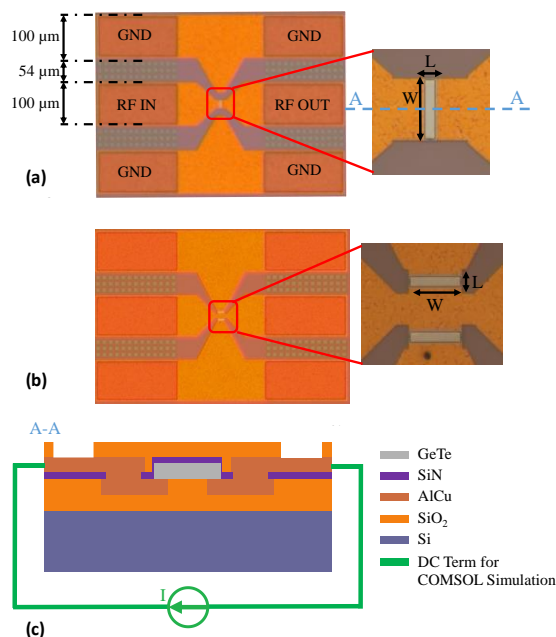


Fig. 1. Microscope image of the PCM switch. (a) Series configuration. $W = 19 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$. (b) Shunt configuration Two PCM in parallel, $W = 16 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$. (c) Technological stack.

B. Electrical Actuation

Direct heating can be performed very easily through this technological stack. A voltage pulse-shape signal is simply applied between the two ports RF IN and RF OUT (as defined in Fig. 1) to induce a change in the phase of the PCM.

In previous literature, different excitation shapes were used in order to get phase change, enabling freezing in a messy state for amorphization or re-arrangement and stabilization of the atomic crystal for crystallization, [11]. In this study, for the very first time, a unique pulse shape has been optimized to control both phase changes. Only the voltage level has been modified.

From a material point-of-view, a two-step process is needed to amorphize the crystalline phase: the PCM has first to be melt, and second to be tempered. The melting temperature to break connections between atoms is reached at 700°C. A 5-ns rise time, 50-ns duration time and 5-ns fall time pulse of tension is used for that purpose. Fig. 2, part A, shows that the melting point is reached in less than 20 ns. The first order response of the switch is due to the presence of parasitic capacitors in the circuit, so that the 20-ns duration time to amorphize the material is clearly overestimated. As GeTe electrical conductivity in the liquid melting phase is higher than in the crystalline one, voltage at the switch electrodes decreases until the steady state regime is reached (Fig 2, part B). Then, a thermal tempering occurs to freeze GeTe (Fig. 2, part C) into a messy state (Fig. 2, part D). Tempering is a fast operation but capacitive effect still implies an apparent 20-ns duration time.

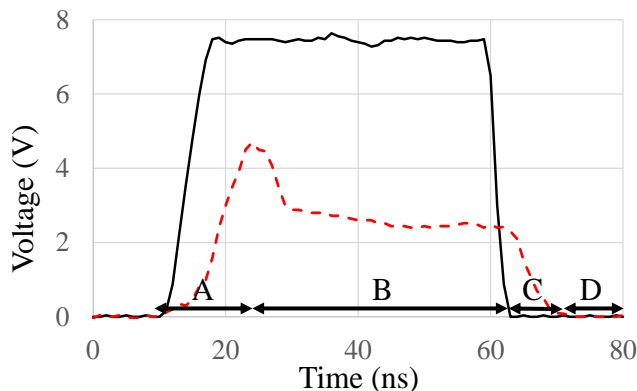


Fig. 2. Pulse generator voltage versus time for amorphization. Voltage at the pulse generator electrodes (solid line) and at the PCM switch electrodes (red dotted line). Part A: GeTe in crystalline phase. Part B: melting. Part C: tempering. Part D: GeTe is amorphized. Switch under test is the one of Fig. 1a, with $W = 19 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$.

Note that the DC current necessary to amorphize the PCM is 700 mA which is higher than for indirect systems: 60 mA in [11] or 9 mA in [12], but with a significantly lower voltage:

4.5 V whereas 8.5 V were needed in [12] and 20 V in [11], respectively.

Within indirect heating, crystallization is known to be the most energy consuming phase transition because of the time needed to re-arrange atoms in a periodic pattern [11]-[14]. Within direct heating, a different physical phenomenon occurs during PCM crystallization. The principle is based on the possibility to create a conductive filament through direct actuation, which for a given geometry is only depending on the level of the voltage applied via the RF IN and OUT ports, named as threshold voltage, V_{TH} , as in [18]. It is somewhat a misnomer in the literature that V_{TH} is given in V/ μm as any disruptive electric field. In this paper, the disruptive electric field will be written E_{TH} while V_{TH} equal $L \cdot E_{TH}$. Once threshold voltage has been reached, an almost instantaneous crystallization occurs. As aforementioned, the same pulse shape as applied for amorphization is used for crystallization, *i.e.* a waveform with 5-ns rise time, 50-ns duration time and 5-ns fall time. This is the reason why this technique can reduce significantly the switch power consumption as compared to indirect heating. Fig. 3 shows that the filament is created at 30 ns, for a voltage at the GeTe electrodes equal to 2.15 V. Then, a voltage drop occurs due to an evolution of the GeTe conductivity. Phase change is reached; material is in its crystalline phase (Fig. 3, part B). Threshold voltage is considered as an intrinsic limitation. Its impact has been discussed in [12] and [18] where a pondering between threshold voltage and breakdown RF power was proposed when dealing with RF power handling. A deep insight analysis concerning this phenomenon is proposed here with the introduction of analytical equations that could help for design by considering not only the FoM given by the cut-off frequency but also power handling. Notably, power handling should depend on the switch configuration series or shunt. These specific issues will be discussed in section IV.

To conclude about direct actuation, Table I compares direct and indirect heating in terms of the total consumed energy per PCM volume per cycle (corresponding to an ON-OFF transition followed by an OFF-ON transition). Direct heating is very efficient to reduce energy consumption. Particularly, the main advantage of direct heating is for crystallization, as the creation of a conductive filament is a shorter phenomenon than a long thermal re-arrangement approach. Here, series direct heating consumes 330 nJ/ μm^3 per cycle, mainly for amorphisation, whereas series indirect heating as presented in [11] and [12] consumes 2.5 times more. Shunt configuration, where two devices are in parallel, has not been measured but should obviously consume twice than the series one, due to

TABLE I.
SUMMARY OF MEASUREMENT RESULTS

Paper	Actuation	ON-state DC resistance (Ω)	Size : W^* (μm), L (μm), t (nm)	Insertion Loss (dB) @10 GHz/ @40 GHz	Isolation (dB) @10 GHz/ @40 GHz	Cut-Off Frequency (THz)	Switching time (ns) per cycle	P_{max} (dBm) OFF-state	P_{max} (dBm) ON-state	Energy consumption (nJ/ μm^3) per cycle
[11][18] - Series	Indirect	≈ 1	30, 0.9, 110	$\approx 0.1 / \approx 0.1$	$>20 / \approx 10$	≈ 11	$1.6 \cdot 10^3$	28.5	>28.5	820
[12] - Series	Indirect	3.9	12, 0.6, 250	$\approx 0.4 / < 0.5$	$\approx 22 / > 18$	≈ 4	$404 \cdot 10^3$	> 20	-	845
[14] - Series	Indirect	2.4	50, 2, -	$\approx 0.25 / 0.5$	$> 28 / > 15$	≈ 11		37.4	40	690
This - Series	Direct	1.1	19, 1, 300	$\approx 0.15 / \approx 0.15$	$>26 / > 12$	≈ 21	2 X 60	27	32	330
This - Shunt	Direct	5.0	2x16*, 1, 300	$\approx 0.4 / \approx 0.5$	$>30 / > 25$	$\approx 11^{**}$	2 X 60	31	> 35	660***

* 2xW in shunt

**see definition in section III, equation (2)

***estimated (as twice that in series configuration as W is almost doubled)

amorphization, as dimensions are almost doubled (19 μm series against 2X16 μm shunt) are compared in Table I).

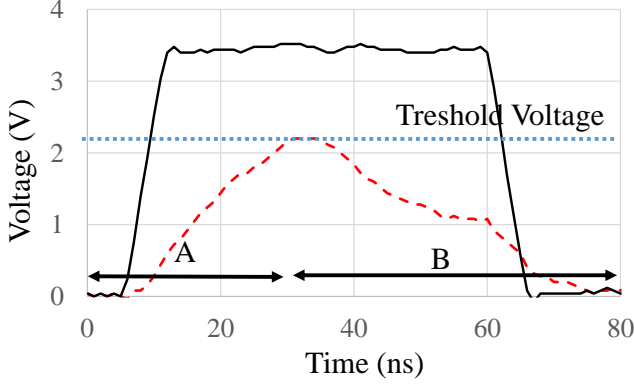


Fig. 3. Pulse generator voltage versus time for crystallization. Voltage at the pulse generator electrodes (solid line) and at the PCM switch electrodes (red dotted line). Part A: GeTe is still in amorphous state. Part B: GeTe crystallizes. Switch under test is the one of Fig. 1a, with $W = 19 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$.

III. SMALL SIGNAL ANALYSIS

In order to model the switch, either in a series or in a shunt mode, S-parameters measurements have been carried out from 40 MHz to 40 GHz using RF-probes (Z-probes) with a 150- μm pitch, on a measurement set-up composed of a semi-automatic probe station linked to a ANRITSU ME7808C vector network analyzer. SOLT (Short, Open, Load, Thru) calibration was performed. Prober shows termination loads of 50 Ω .

Fig. 4 gives the electrical equivalent circuit of the switch in series (Fig. 4.a) or in shunt (Fig. 4.b) configuration. Be careful that ON-state refers to the switch state while GeTe phase is described as amorphous or crystalline. As a general rule, R equals R_{ON} (R_{OFF} respectively) referring to the PCM resistance at the ON- (OFF- respectively) state of the switch. For series configuration, R_{ON} is the very low resistance obtained for crystalline GeTe whereas R_{OFF} is the five or six orders of magnitude higher resistance obtained for amorphous GeTe. C_{OFF} is the parallel capacitance, observable during OFF-state only. For shunt configuration, this is the contrary. R_{OFF} is the very low resistance of the crystal whereas R_{ON} is the five or six orders of magnitude higher resistance obtained for amorphous PCM. C_{ON} is the parallel capacitance, observable during ON-state only. $L_{||}$ models the inductive effect of the extra widths coming out from ground strips and necessary to contact the parallel PCMs, as in Fig. 1b. This model is somewhat similar to that proposed in [19] for parallel PCM with a slight change in the position of $L_{||}$, in series with the parallel R-C, much more suited to our devices.

The widths of the central and ground strips of the feeding lines on both sides of the PCM are 100 μm , with a gap separation equaling 54 μm . These dimensions correspond to a 50- Ω characteristic impedance Z_0 . As shown in the inset of Fig. 1a, the central strip reduces to 20 μm in the GeTe area; the gap reduces as well to maintain a 50- Ω characteristic impedance. For the shunt RF switch, the feeding lines stay the same but the central strip is simply not cut.

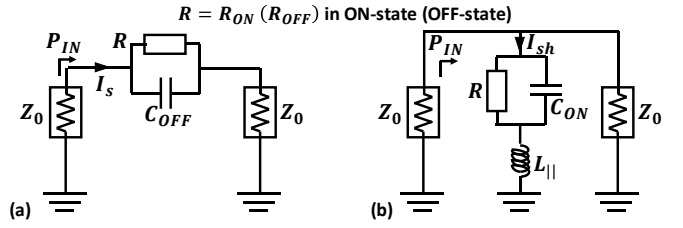


Fig. 4. Electrical equivalent circuit of the GeTe switch in its environment bench. The influence of GeTe is modeled with a variable resistor and a capacitor. The terms Z_0 represent the 50- Ω prober termination ports. a. Series GeTe switch. b. Shunt GeTe switch (in practice, two PCM in parallel).

Results up to 40 GHz are given in Fig. 5 for both configurations. Note that the loss due to the matched feeding lines has been de-embedded at any time.

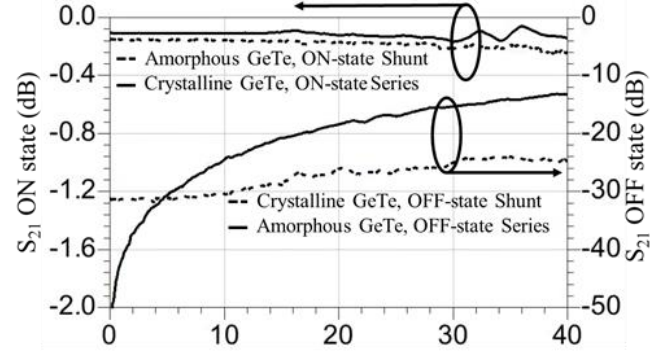


Fig. 5. Measured de-embedded switch performance for a 300-nm thick GeTe film. Insertion loss with switch in ON-state in series (solid line) and shunt (dash line) configurations. Isolation with switch in OFF-state in series (solid line) and shunt (dash line) configurations. Series configuration: $W = 19 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$. Shunt configuration: two PCM in parallel, $W = 16 \mu\text{m}$, $T = 300 \text{ nm}$, $L = 1 \mu\text{m}$.

For serial configuration, insertion loss at ON-state is lower than 0.15 dB up to 40 GHz and almost constant over the whole frequency band. A simple R_{ON} (ON-state resistance) with a value of 1.1 Ω can be used as an equivalent circuit. An isolation at OFF-state higher than 14 dB, up to 40 GHz is observed. The equivalent electrical model for the OFF-state corresponds to a parallel RC circuit with a resistance R_{OFF} of 100 k Ω and a capacitance C_{OFF} of 6.8 fF. This leads to a cut-off frequency equal to 21 THz, at the state-of-the-art to the authors' best knowledge, as shown in Table I.

For shunt configuration with two parallel shunt PCMs, performing results are also achieved up to 40 GHz with an isolation at OFF-state better than 24 dB corresponding to $R_{OFF} = 0,7 \Omega$ in series with $L_{||} \sim 7 \text{ fH}$. At ON-state, insertion loss varying between 0.4 and 0.5 dB over the whole band enable to evaluate the ON-capacitance as $C_{ON} = 20 \text{ fF}$. Meanwhile there is no sensitivity on the extraction of R_{ON} , that can be thus neglected in the model. An equivalent Figure-of-Merit dedicated to shunt configuration can be given as in equation (2):

$$FOM_{shunt} = 1/(2\pi R_{OFF} C_{ON}) \quad (2)$$

For the shunt switch of Fig. 1b, a Figure-of-Merit equal to 11 THz is obtained with (2). It is not surprising to get a value of $C_{ON-shunt}$ almost twice the one of $C_{OFF-series}$ as there are two PCMs in parallel in the shunt configuration. However, the triangular feeding lines to PCM are not exactly the same shape

in series or shunt configurations which explains why we observe practically $C_{ON-shunt} > 2C_{OFF-series}$. Concerning $R_{OFF-shunt}$, it should be equal to half of $R_{ON-series}$, if the widths, W , were the same. This is not totally true (19 μm in series and 16 μm in shunt) so that $R_{OFF-shunt} > R_{ON-series}/2$. This is the reason why the same FoM is not observed. It has to be noted that $L_{//}$ has no influence on FoM_{shunt} .

IV. LARGE SIGNAL ANALYSIS

A. Power Handling

Power handling is an important figure of merit to evaluate RF switch performance. Depending on the application, it can even be a core issue.

Power handling capability was tested for both ON- and OFF-states. Likewise, two configurations of switch were tested: serial switches as presented in Fig. 1a and shunt switches depicted in Fig.1b. As it will be discussed, the voltage and current flow through the devices are related to the configuration; so conclusions about power handling are also directly linked to the serial or shunt configuration. Finally, the influence of the switch geometry on the power handling is performed for each case (ON- / OFF-states, serial / shunt configurations). Indeed switches of various geometrical dimensions were characterized: GeTe width W was varied from 300 nm to 19 μm , and two GeTe lengths L were considered (0.5 μm and 1 μm). Likewise, samples with two different GeTe thicknesses T (100 nm and 300 nm) were fabricated and measured. The geometries of the different switches discussed below are given in Table II. For any switches up to 5 identical devices have been characterized to consider potential dispersion due to fabrication.

All power handling measurements presented below were carried out using RF-probes (Z-probes) with a 150- μm pitch on

the same measurement bench composed of a 100kHz – 20GHz signal generator (ROHDE & SCHWARZ SMB 100A) and of a broadband amplifier (ROHDE & SCHWARZ BBA150) allowing to deliver a maximum power of 40 dBm. A 20-dB coupler (MCLI HDL-33-20/200) separates signal between two paths. One is used to supply power to the device while the other one measures the latter by means of a power sensor (ROHDE & SCHWARZ NRP18S) connected to a power meter. A second power sensor is used for a similar measurement at the output of the device. SOLT calibration was performed. In practice, a 2.7 GHz CW signal was applied to the switches with a RF input power discretely ramped-up from -10 dBm to +40 dBm. For each step of 1 dB, both input power P_{IN} and output power P_{OUT} were measured. For reminding, Fig. 4 gives the electrical equivalent circuit of the switch in series configuration (Fig. 4a) and in shunt (Fig. 4b). R_{ON} (R_{OFF} respectively) is the switch resistance of the ON- (OFF-) state and C_{OFF} (C_{ON} respectively) the capacitance that can be determined only during OFF-state for the series configuration (ON-state for the shunt one respectively), as stated in part III. Probers present a 50- Ω load at each terminal, named Z_0 . For reminding, the characteristic impedance of the transmission lines also equals $Z_0=50 \Omega$.

To study the link between power handling and device geometry, it is interesting to consider the current flowing through the switch. This can be done for the series and shunt configurations as depicted in Fig. 4. Thus, analytical expressions which describe the relationship between the input power and the intensity of the current flow through the device for both configurations can be derived as below:

$$I^s = \sqrt{\frac{2}{Z_0} \cdot P_{IN}^s \cdot \frac{(2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2}{(R+2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2}} \quad (3)$$

$$I^{sh} = \frac{1}{|Z^{sh}|} \cdot \sqrt{2Z_0 \cdot P_{IN}^{sh} \cdot \frac{(2R)^2}{(2R+Z_0)^2 + (RC_{ON}\omega Z_0)^2}} \quad (4)$$

TABLE II
SUMMARY OF MEASUREMENT RESULTS OF ON-STATE SERIES SWITCHES, CRYSTALLINE GeTe

Device	Width W (μm)	Thickness T (μm)	Length L (μm)	Resistance R_{ON} (Ω)	Area $W \times T$ (μm^2)	$P_{max-dBm}^s$ (dBm)	P_{max}^s (mW)	Current I_{max}^s (mA)	Voltage V_{max}^s (V)
SE1-W1	0.58	0.1	1.0	155	0.06	5.58	3.61	4.790	0.72
SE1-W2	1.76	0.1	1.0	51.7	0.18	9.65	9.23	12.39	0.68
SE1-W3	7.62	0.1	1.0	11.9	0.76	18.8	75.9	47.90	0.72
SE1-W4	19	0.1	1.0	4.8	1.90	27.0	501.2	129.9	1.17
SE1-W5	31	0.1	1.0	2.9	3.10	31.2	1320	223.1	0.65
SE3-W1	0.58	0.3	1.0	51.5	0.18	6.4	4.36	8.75	0.45
SE3-W2	1.76	0.3	1.0	17	0.53	12.44	17.54	22.4	0.40
SE3-W3	7.62	0.3	1.0	3.9	2.29	23.7	234.4	92.0	0.48
SE3-W4	19	0.3	1.0	1.5	5.70	32	1580	245.6	0.61
SE1-W5-L2	31	0.1	1.5	4.4	3.10	30.2	1050	196	0.84
SE1-W5-L3	31	0.1	2.0	5.9	3.10	28.6	724	174	0.99
SE1-W5-L4	31	0.1	3.0	8.8	3.10	28	631	154	1.28

where I^s and I^{sh} correspond respectively to the current flow through the PCM, in series for the series switch and in shunt for the shunt one, expressed in Ampere. P_{IN}^s is the input power in the series configuration, P_{IN}^{sh} in the shunt one, both expressed in Watt. Z^{sh} , the impedance of the switch in shunt configuration, is equal to $\frac{R}{1+jRC_{ON}\omega}$. As a general rule, R value will depend on the switch configuration and state: $R = R_{ON/OFF}^{s/sh}$.

1) Crystalline GeTe characterization

The goal of this study is not only to define the limits of the device in terms of power handling, but to correlate power handling capability with the switch configuration (series / shunt) and the switch geometry. As the geometrical parameters W , T , and L are independent from each other, it will be assumed that the maximum input power before failure P_{max}^s is given by the following formula:

$$P_{max}^s(W, T, L) = f_W(W) \cdot f_T(T) \cdot f_L(L) \quad (5)$$

where $f_W(W)$ ($f_T(T)$ and $f_L(L)$ respectively) is a function of W (of T and L , respectively); and where these geometrical parameters are given in micrometer units. The objective here is to identify for the first time these unknown functions.

a) Series configuration of the switch

Firstly, the study is focused on series switch. The GeTe width, W , (see Fig. 1a) is varying between $0.58 \mu\text{m}$ and $31 \mu\text{m}$. Two different values of GeTe thickness T (100nm or 300nm) are considered. To begin with, length L is fixed to $1 \mu\text{m}$.

Fig. 6 presents the switch output power P_{OUT} versus input power P_{IN} for different GeTe widths W and thicknesses T . Open circuit and short circuit RF transmission lines, used for calibration, are also given for comparison. When the maximum RF power is reached, the GeTe is dramatically destroyed and the switch behaves like an open circuit. The 1-dB compression point does not occur before failure.

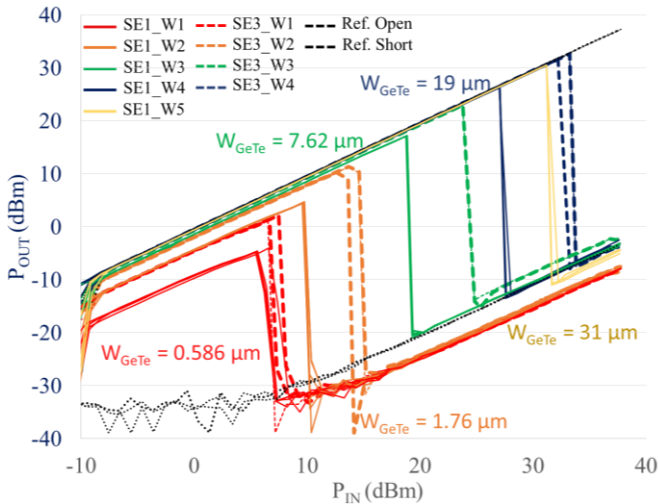


Fig. 6. Series GeTe switch in ON state versus W and T . $L=1 \mu\text{m}$. Output power versus input power when a 2.7-GHz CW signal is applied. Same switches (fabrication repeatability study) are superimposed on the plot (same trace, same color). Switches with different widths, W , are plotted with different color; 100nm thick GeTe are in solid line. 300nm thick GeTe are in dotted line.

The maximum input power before failure, P_{max}^s , measured with the bench, and the corresponding current flow through the

device, I_{max}^s , and voltage, V_{max}^s , are given in Table II and plotted in Fig. 7. Note the I_{max}^s is derived from P_{max}^s by using equation (1). In this figure, the maximum input power P_{max}^s is plotted versus the GeTe width W , for the two thickness values. Each point corresponds to an average value of the exactly same devices. A fitting curve is extracted from these results so that (5) can be re-written as follow, where P_{max}^s is given in mW:

$$P_{max}^s(W, 0.1, 1) = 1.375 \cdot W^2 \quad (6)$$

$$P_{max}^s(W, 0.3, 1) = 4.32 \cdot W^2 \quad (7)$$

So for the two thickness of GeTe under consideration, the maximum power P_{max}^s that can be handled by the device is a function of the square of W .

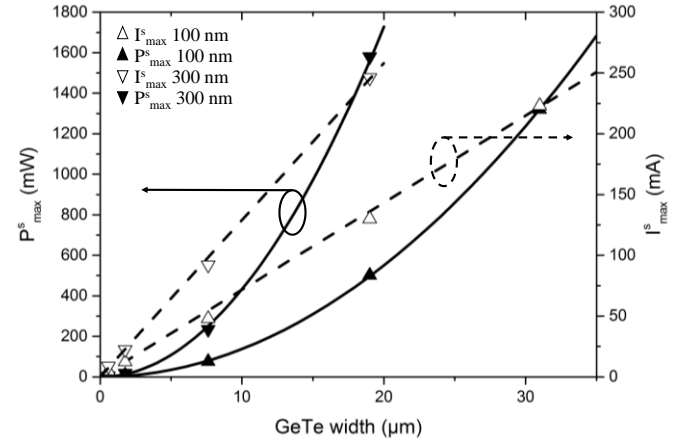


Fig. 7. Failure power P_{max}^s and current I_{max}^s of the series 1- μm length GeTe switch in ON state versus W for two values of the thickness: measurements are given by marker symbols (up triangle for 100 nm thick and down triangles for 300 nm thick), and the corresponding fitting curve (6), (7) in solid and dash lines respectively for power and current.

From (6) and (7) it is now possible to extract $f_T(T)$ for values of T between 100 nm and 300 nm. In that range $f_T(T)$ is proportional to T . Equation (5) can thus be rewritten as in (8):

$$P_{max}^s(W, T, 1) = 13.75 \cdot W^2 \cdot T \quad (8)$$

Hence, it can be seen that the maximum power handling of the series switch at OFF-state, corresponding to amorphous GeTe, is function of the square of its width and is proportional to its thickness. As in [20], when the cross sectional area of the GeTe is reduced, the maximum power handling is also reduced.

The variation of the maximum current I_{max}^s before failure is also plotted in Fig. 7. Same approach has been done; a linear curve can be used to fit the results. The following expression can be used to model the variation of I_{max}^s (expressed in Amperes) with the GeTe geometry:

$$I_{max}^s(W, T, 1) = 22.6 \cdot W \cdot T^{1/2} \quad (9)$$

The relative error (not shown here) between the measured values P_{max}^s (see table II) and the formula $P_{max}^s(W, T, L)$ in equation (6) is lower than 6% for W varying between $7.62 \mu\text{m}$ and $31 \mu\text{m}$ and T in the range of 100 – 300 nm.

A study on how P_{max}^s and I_{max}^s are affected by the GeTe length L was also performed. Output power P_{OUT} versus the input power P_{IN} for different GeTe lengths L are given in Fig. 8.

Contrarily to W and T , an increase in L will decrease P_{max}^S . As it will be confirmed in the next paragraph by a thermal analysis, the longer is the switch, the higher is the temperature at the middle of the GeTe.

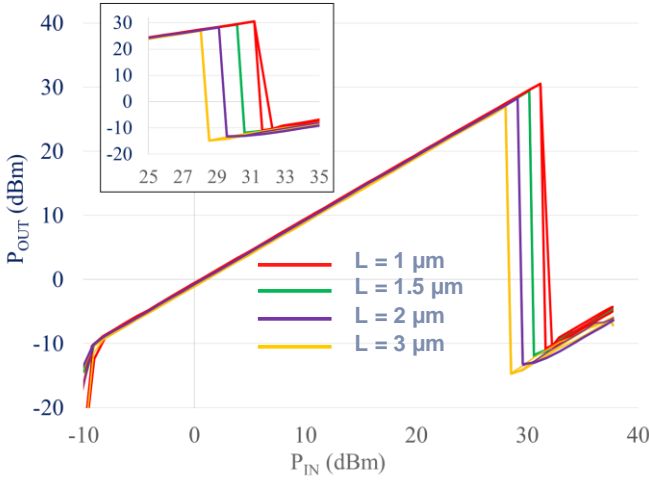


Fig. 8. Series GeTe switch in ON state versus L . $W=31 \mu\text{m}$. $T=0.1 \mu\text{m}$. Output power versus input power when a 2.7-GHz CW signal is applied. Same switches (fabrication repeatability study) are superimposed on the plot (same trace, same color).

The maximum input power before failure, P_{max}^S , measured with the bench, and the corresponding current flow through the device, I_{max}^S , are plotted in Fig. 9. The results can be fitted with a simple expression and the following formulas can finally be used to model the variation of P_{max}^S and I_{max}^S with W , T and L :

$$P_{max}^S(W, T, L) = 233.4 \cdot W^2 \cdot T / (L + 3.12)^2 \quad (10)$$

$$I_{max}^S(W, T, L) = 93.1 \cdot W \cdot T^{1/2} / (L + 3.12) \quad (11)$$

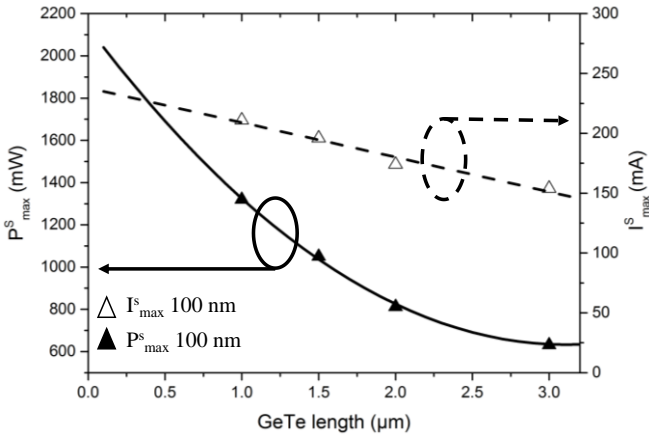


Fig. 9. Failure power P_{max}^S and current I_{max}^S of the series 31- μm wide and 100-nm thick GeTe switch in ON state versus L . Measurements are given by marker symbols. Corresponding fitting curve of equations (10) and (11) are in solid and dash lines respectively for power and current.

In the geometrical parameter range considered for the study, the maximum power is proportional to $W^2 \cdot T$ and inversely proportional to L . Note that $W^2 \cdot T$ does not correspond to the square of the transverse section of the GeTe $(W \cdot T)^2$. One explanation can be found from a thermoelectric modeling of the switch. Indeed, the influence of W and T in terms of heat transfer may differ. As it can be seen in Fig. 1, the main heat

spreader is the metallic line that contacts the GeTe backside. Hence, the way in which thermal dissipation occurs does not depend on the thickness of GeTe but mainly on its width. Anyway, even if W and T do not play the same role in terms of thermal dissipation: the thicker the GeTe is, the harder it is to dissipate heat.

It is clear that the GeTe geometry plays an important role on power handling for crystalline GeTe. A thermoelectric modeling of the proposed device has been performed to check by simulation the validity of (10) and (11) extracted from RF measurements based on a limited number of devices. As the failure is caused by too high a temperature in the GeTe [20], a thermoelectric modeling allows to connect RF excitation with the internal temperature of the structure. A 2D multi-physics simulator, COMSOL, has been used to simulate the GeTe switch. Electrical and thermal conductivity of the different materials that compose the switch are given in Table III, on the basis of data available in the literature. The phase change of the GeTe has been modeled as a variation versus temperature of its thermal conductivity. In this thermoelectric modelling, to simulate direct heating excitation, a current step comparable to the one that has been used during the measurements was set between the two RF lines. The same rise and fall time (respectively 5 ns, 50 ns and 5 ns) were considered in simulation.

TABLE III
ELECTRICAL AND THERMAL CONDUCTIVITY OF MATERIALS

Material	Electrical Conductivity (S/m)	Thermal Conductivity (W/m/K)
TiN	1 M	21.9
Amorphous GeTe	$\approx 5^*$	4
Crystalline GeTe	$\approx 100 \text{ k}^*$	7
SiN	1 p	30
AlCu	35 M	237
SiO ₂	1 f	1.4
Si	1	130

* extracted from 4-probes full sheet measurements

The device temperature profile is plotted in Fig. 10 after 55 ns, just before the pulse generator stops. The figure shows the spots where the temperature is higher than 1000°K, *i.e.* above melting temperature. It is clear that the highest temperature is reached in the center of the device, especially at the GeTe layer. Generally speaking, too much temperature rise will cause device failure. More precisely, the failure may come from several factors that are exacerbated with the increase in temperature, such as current crowding, phase change nucleation mechanisms, presence of defects, or even crystalline orientation. These phenomena consisting in considering the non-ideal nature of the switch are difficult to simulate accurately. Thus, to retrieve the measurement results, we followed a two-step approach. First a temperature t_0 (typically higher than melting temperature) is chosen. Then an observation point is chosen, numbered N°1, N°2 or N°3 as depicted on Fig. 10. Second, for each geometrical quantity (W , T or L), the current magnitude, I_{t_0} , that leads to temperature t_0 at point N°i, is derived from simulation. Results are summarized

in Fig. 11, where Fig. 11a plots the variation of I_{t_0} with W , Fig. 11b with T and Fig. 11c with L . For each case, an analytical expression as in (11) is used to model the observed variation. As for the empirical case, a very good match is obtained between simulation and analytical fit. Coefficients may be somewhat different between simulation fit and measurement fit. This is due to the observed currents which are not the same. I_{t_0} enables to reach t_0 at point $N^{\circ}i$ in simulation. I_{max}^s is the failure current across PCM in measurements.

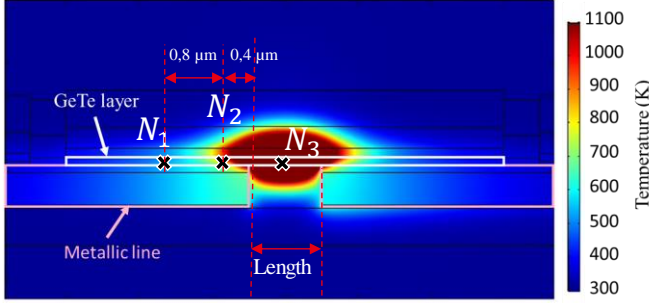


Fig. 10. Temperature profile in a 2D-COMSOL simulation.

b) *Shunt configuration of the switch*

Depending on the configuration (shunt or series), the switch will be affected differently by the RF power. Consequently, a similar work as previously was carried out in the case of the shunt switch.

Failure appears when temperature rise induced by the current flow through the PCM device (as described on Fig. 4 with I^s and I^{sh}) is too high. Hence, on the basis of similar PCM sizes either in shunt or in series configuration (which means $R = R_{ON}^s = R_{OFF}^{sh}$), failure corresponds to identical maximum current:

$$I_{max}^s = I_{max}^{sh} \quad (12)$$

I^s and I^{sh} are related to P_{IN}^s and P_{IN}^{sh} through (3) and (4) respectively. Moreover, in crystalline state, assumption (13) can be done:

$$RC_{OFF}\omega Z_0 \ll Z_0 \text{ and } RC_{ON}\omega Z_0 \ll Z_0 \quad (13)$$

On the basis of (3), (4) and (13), equation (12) can be rewritten as equation (14):

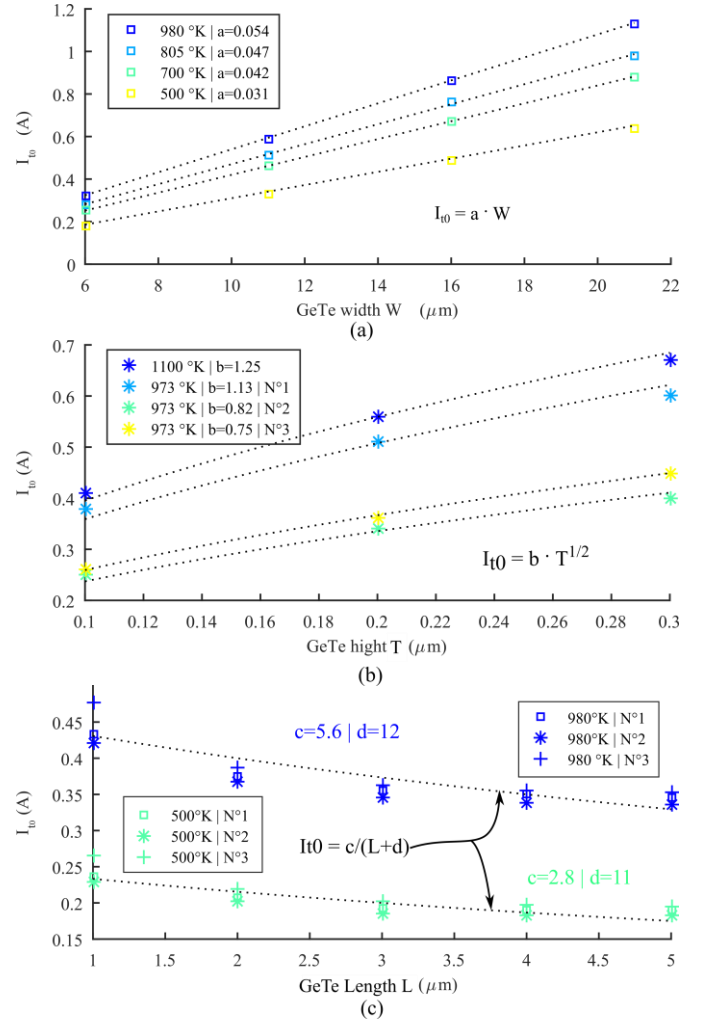


Fig. 11. Thermoelectric modeling of the GeTe. Input current I_{t_0} versus the GeTe geometrical parameters for a specific temperature t_0 . a) W is varying, $T=0.3 \mu\text{m}$, $L=1 \mu\text{m}$, b) T is varying, $W=20 \mu\text{m}$, $L=1 \mu\text{m}$, c) L is varying, $T=0.3 \mu\text{m}$, $W=20 \mu\text{m}$. $N^{\circ}i$ corresponds to various locations along the GeTe length at which the temperature t_0 is considered. When no location is precised, temperature is measured at the center of the GeTe. Dash line fits the data.

$$P_{max_cryst}^s = \frac{(R+2Z_0)^2}{(2R+Z_0)^2} \cdot P_{max_cryst}^{sh} \quad (14)$$

With (14), it is clear that for the same electrical power dissipated by the switch, the input power at which the failure occurs depends on the series or shunt configurations.

TABLE IV
SUMMARY OF MEASUREMENT RESULTS OF OFF-STATE SHUNT SWITCHES, CRYSTALLINE GeTe

Device	Width $2xW$ (μm)	Thickness T (μm)	Length L (μm)	Resistance R_{OFF} (Ω)	Area $W \times T$ (μm^2)	$P_{max_dBm}^{sh}$ (dBm)	P_{max}^{sh} (mW)	Current I_{max}^{sh} (mA)	Voltage V_{max}^{sh} (V)
SH1-W1	1.17	0.1	1.0	77.6	0.117	9.2	9.77	9.84	0.47
SH1-W2	3.52	0.1	1.0	26.0	0.352	12	15.85	24.0	0.42
SH1-W3	12.9	0.1	1.0	7.0	1.29	18.8	75.86	86.4	0.38
SH1-W4	32.0	0.1	1.0	2.8	3.20	27.0	501.2	240.0	0.69
SH3-W1	1.17	0.3	1.0	25.9	3.52	10.9	12.30	14.6	0.47
SH3-W2	3.52	0.3	1.0	8.6	1.05	14.9	30.90	40.9	0.47
SH3-W3	12.9	0.3	1.0	2.4	3.87	22.6	182.0	141	0.47
SH3-W4	32.0	0.3	1.0	1.0	9.60	31	1259	408	0.65

For $R < Z_0$, the allowable power in a series switch is greater than in a shunt switch presenting equal dimensions, and vice versa for $R > Z_0$. In order to have R as low as possible both in the series (for low insertion loss) and shunt (for high isolation) configurations (i.e. $R \ll Z_0$), a series device can handle four times more power than a shunt device. For practical consideration, smaller is the resistance (like for the switch with a thickness of 300 nm as compared to the one of 100 nm), better is the power handling during crystalline phase.

This result also explains why it is important in power handling study to consider these two configurations. It is why, like for the series switch configuration, power handling measurements have been performed on shunt configuration. Geometrical and electrical parameters of the measured devices are given in Table IV. As previously, a study on how P_{max}^{sh} and I_{max}^{sh} are affected by the GeTe geometrical parameters (W and T) was performed. Fig. 12 shows comparable results as exploited in the series case. After failure, we do not observe isolation anymore and the RF signal can flow back through the RF transmission lines.

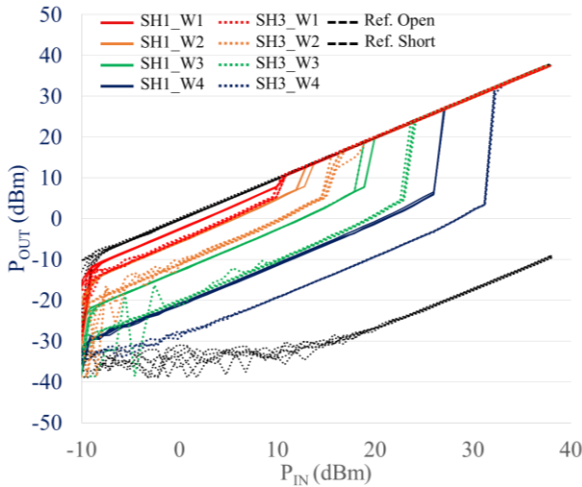


Fig. 12. Shunt GeTe switch in OFF state versus W and T . $L=1 \mu\text{m}$. Output power versus input power when a 2.7-GHz CW signal is applied. Same switches (fabrication repeatability study) are superimposed on the plot (same trace, same color). Switches with different widths, W , are plotted with different color; 100nm thick GeTe are in solid line. 300nm thick GeTe are in dotted line.

In Fig. 13 the same simple expressions can be used to fit the results and to model the variation of P_{max}^{sh} (in mW) and I_{max}^{sh} (in

A) with W (in μm) and T (in μm). No fit could be performed in terms of variation with L as only one length is available, i.e. $1 \mu\text{m}$. Also the analytical formula for shunt has not been confirmed with COMSOL multi-physics simulations but it can be assumed that conclusions would be similar. For measurements, fit gives:

$$P_{max}^{sh}(W, T, 1) = 4.0 \cdot W^2 \cdot T \quad (15)$$

$$I_{max}^{sh}(W, T, 1) = 23 \cdot W \cdot T^{1/2} \quad (16)$$

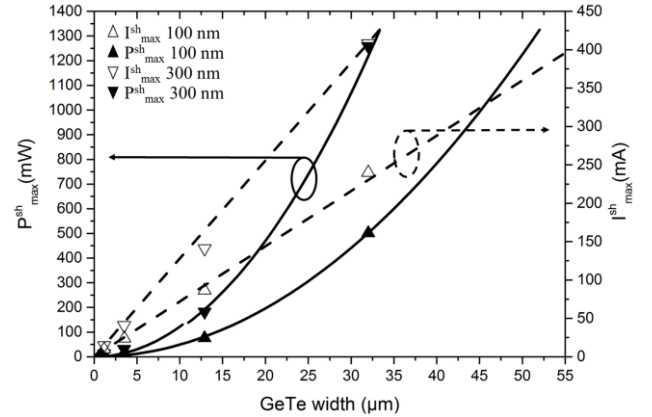


Fig. 13. Failure power P_{max}^s and current I_{max}^s of the shunt 1- μm length GeTe switch in OFF state versus W for two values of the thickness: measurements are given by marker symbols (up triangle for 100 nm thick and down triangles for 300 nm thick), and the corresponding fitting curve (15), (16) in solid and dash lines respectively for power and current.

By comparing (15), shunt configuration, with (8) (series configuration), it can be seen that $P_{max}^{sh}(W, T, 1) = 3.42 \cdot P_{max}^s(W, T, 1)$. This result is in excellent agreement with (14). As an example, for $W=31 \mu\text{m}$ in series and $W=32 \mu\text{m}$ in shunt, with $L=1 \mu\text{m}$ and $T=100 \text{ nm}$ for both, R_{ON}^s and R_{OFF}^s equal 2.9 and 2.8 Ω respectively. By taking $R_{ON}^s=R_{OFF}^s=2.85 \Omega$, mid value, a coefficient of 3.41 is expected with (14). This confirms that series configuration supports much more power in case of crystalline GeTe.

Anyway, before concluding in favor of one configuration or another (better isolation for shunt but better power handling for series when GeTe is crystalline), all cases have to be studied. In particular, what is power handling for amorphous GeTe, in both configurations?

TABLE V
SUMMARY OF MEASUREMENT RESULTS OF OFF-STATE SERIES SWITCHES, AMORPHOUS GeTe

Device	Thickness (μm)	Length (μm)	P_{max}^s (dBm)	P_{max}^s (mW)	$V_{max-RMS}^s$ (V)	$V_{max-ave}^s$ (V)	L_a^{RMS} (μm)	L_a^{ave} (μm)
SE3-W1 to SE3-W4	0.3	1	Min: 18.5 Mean: 20.0 Max: 21.5	Min: 70.8 Mean: 100 Max: 141	Min: 3.76 Mean: 4.47 Max: 5.31	Min: 3.39 Mean: 4.02 Max: 4.78	Min: 0.30 Mean: 0.35 Max: 0.42	Min: 0.27 Mean: 0.32 Max: 0.38
SE1-W1 to SE1-W4	0.1	1	Min: 23.5 Mean: 25.5 Max: 27.5	Min: 224 Mean: 355 Max: 562	Min: 6.69 Mean: 8.42 Max: 10.6	Min: 6.02 Mean: 7.58 Max: 9.54	Min: 0.53 Mean: 0.67 Max: 0.84	Min: 0.48 Mean: 0.60 Max: 0.75
SE1-W5	0.1	1	27.5	562	10.6	9.54	0.84	0.75
SE1-W5-L2	0.1	2	34.0	2510	22.4	20.2	1.80	1.60

2) Amorphous GeTe characterization

The study has been performed for GeTe in amorphous state after programming switches through the method described in section II. Switches in series and shunt configurations for thicknesses of 100 nm or 300 nm, lengths of 1 μm and 2 μm , and several widths, have been explored.

a) Series configuration of the switch

Results are exploited in Fig. 14 where output power versus input power evolutions are shown.

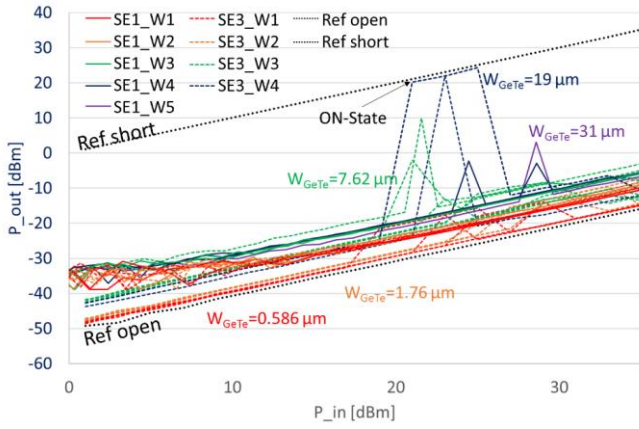


Fig. 14. Series GeTe switch in OFF state versus W and T . $L=1 \mu\text{m}$. Output power versus input power when a 2.7-GHz CW signal is applied. Same switches (fabrication repeatability study) are superimposed on the plot (same trace, same color). Switches with different widths, W , are plotted with different color; 100nm thick GeTe are in solid line. 300nm thick GeTe are in dotted line.

For amorphous state, failure corresponds to the maximum RF voltage that can be handled by the material. In fact, the switch failure is explained as a parasitic crystallization that occurs when the equivalent voltage at the GeTe edges should equal the threshold voltage, given by $V_{th} = E_{th} \cdot L$, as studied in [18]. This maximum voltage is thus proportional to the material length. A value of 12.6 V/ μm has been obtained for E_{th} in [18]. By using the model of Fig. 4a, for series switches, it is possible from (3) to calculate the RF magnitude voltage V_{max}^s across the switch before failure.

$$V_{max}^s = |Z^s| \cdot \sqrt{\frac{2}{Z_0} \cdot P_{max}^s \cdot \frac{(2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2}{(R+2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2}} \quad (13)$$

where Z^s , the impedance of the switch in series configuration, is equal to $\frac{R}{1+jRC_{OFF}\omega}$. By deriving RMS voltage, $V_{max-RMS}^s$, and average voltage, $V_{max-ave}^s$, as in [18], it comes:

$$V_{max-RMS}^s = \frac{V_{max}^s}{\sqrt{2}} \quad (14)$$

$$V_{max-ave}^s = \frac{V_{max}^s}{\pi} \quad (15)$$

RMS voltage ($V_{max-RMS}^s$) is equal to the value of the continuous voltage that would produce the same mean power dissipation than the RF voltage in a resistive load. Average voltage ($V_{max-ave}^s$) is equal to the average of the rectified voltage. By correlating either $V_{max-RMS}^s$ or $V_{max-ave}^s$ with E_{TH} , the length of the amorphous material L_a , (which is shorter than the total GeTe length L) can be calculated.

Switch dimensions, the maximum input power before failure P_{max}^s and the corresponding RMS and average RF voltage are given in Table V. The calculated length of amorphous GeTe L_a obtained by considering an E_{TH} of 12.6 V/ μm with either $V_{max-RMS}^s$ (noted L_a^{RMS}) or $V_{max-ave}^s$ (noted L_a^{ave}) are also shown in Table V. Results show that for switches with longer GeTe lengths, L , it is possible to obtain longer lengths of amorphous GeTe, L_a . This also means that power handling can be improved by using longer GeTe lengths. Note that in Table V, the length of amorphous GeTe is not a perfectly controlled parameter. This explains the dispersion observed in the power handling of devices showing same length and same thickness.

As aforementioned, when the maximum RF power is reached, the switch changes from OFF- to ON-state. This change is not destructive for the switch as it corresponds to a transition from amorphous to crystalline phase. It can be observed for some switches (SE3_W4 in blue curve in Fig. 14) that after failure the switch moves to ON-state. By pursuing the increase in input power, the switch is finally destroyed towards an open state, as previously observed for switches in crystalline phase. However, for other switches (SE3_W3 in green curve, SE1_W4 in blue curve and SE1_W5 in purple curve in Fig. 14), after failure, the switch changes toward an ON-state presenting extremely high insertion losses; it is immediately destroyed afterwards, thus leading to open state.

b) Shunt configuration of the switch

Regarding shunt switches, no failure could be detected by means of electrical measurements of the output power. However, a failure was observed by means of optical microscopy on most of the switches at about 30 dBm, Fig. 15. Note that this order of magnitude is in good agreement with the one that can be estimated with the introduced model. Indeed, from (4) it is possible to derive the relation between the maximum input power before failure P_{max}^{sh} and the voltage across the switch, V_{max}^{sh} :

$$V_{max}^{sh} = \sqrt{2Z_0 \cdot P_{max}^{sh} \cdot \frac{(2R)^2}{(2R+Z_0)^2 + (RC_{ON}\omega Z_0)^2}} \quad (16)$$

Let's consider $E_{th}=12.6 \text{ V}/\mu\text{m}$ as the limiting factor for power handling in amorphous phase, and an amorphized material mean length, L_a^{RMS} , of 350 nm for a GeTe thickness of 300 nm (respectively $L_a^{RMS}=670 \text{ nm}$ for $T=100 \text{ nm}$), as determined in the case of series switches in Table V. With these assumptions, and by using (16), it is possible to derive the maximum input power before failure P_{max}^{sh} . Thus, a maximum input power of 26 dBm has been obtained for switches with 300-nm thick GeTe and of 31.5 dBm for switches with a thickness of 100 nm. These results are in good agreement with the optical observation of the failure.

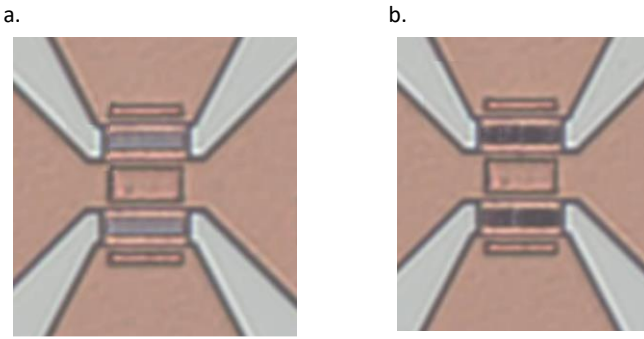


Fig. 15. a. Optical view of an amorphous GeTe switch in shunt before failure. b. Optical view of an amorphous GeTe switch in shunt after failure.

As previously, it is interesting now to compare power handling between the two configurations: shunt and series. For similar GeTe dimensions, leading to $R = R_{OFF}^s = R_{ON}^{sh}$, and identical values of the voltage across the switch, as voltage is the limiting factor for amorphous GeTe [18]), it is possible to derive the followings relationships:

$$V_{max}^{sh} = V_{max}^{sh} \quad (17)$$

$$P_{max}^s = \frac{1}{|Z^s|^2} \cdot \frac{(R+2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2}{(2Z_0)^2 + (2RC_{OFF}\omega Z_0)^2} \cdot \frac{(2Z_0R)^2}{(2R+Z_0)^2 + (RC_{ON}\omega Z_0)^2} \cdot P_{max}^{sh} \quad (18)$$

During amorphous state, it is assumed that:

$$\begin{aligned} R + Z_0 &\cong R \\ 2R + Z_0 &\cong 2R \\ R + 2Z_0 &\cong R \\ 2Z_0 C_{OFF} \omega \cdot R &\ll R \text{ and } 2Z_0 C_{ON} \omega \cdot R \ll R \end{aligned} \quad (19)$$

So, with these assumptions and from (18), it can be stated that:

$$P_{max_amorph}^s \cong \frac{1}{4} \cdot P_{max_amorph}^{sh} \quad (20)$$

Finally, for amorphous GeTe, the shunt switch at ON-state will hold about four times more power than the series one at OFF-state. Also, as a general conclusion for the amorphous phase, small thicknesses seem to be preferable rather than thick ones. The compromises between dimensions and configurations will be discussed in conclusion, after presenting some linearity aspects.

B. Linearity

The linearity of the GeTe switch is characterized at a fundamental frequency of 824 MHz, delivered by the RF power generator Agilent E4438C, and amplified through the amplifier system Ophir 5143. Two power sensors are used: before and after device. Fig. 16 shows the linearity measurement up to 35 dBm of a series device. The tested device is SE3-W4 (Table II), with $W=19 \mu\text{m}$, $L=1 \mu\text{m}$ and $T=300 \text{ nm}$. Rejection is about 100 dBc until destruction of the device at 33 dBm. This result is at the state of the art for PCM RF switches [14] and higher than CMOS [21].

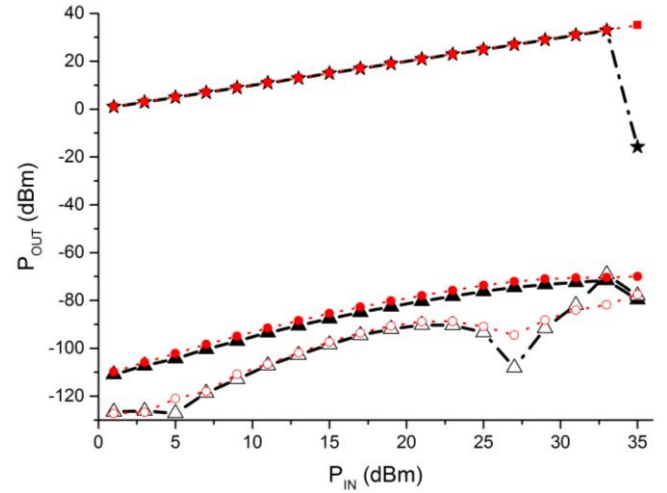


Fig. 16. Series device in ON-state (crystalline phase). Measurement of P_{OUT} versus P_{IN} at fundamental frequency f_0 (black dotted, dashed and star line), at $2f_0$ (black dotted, dashed and triangle line) and $3f_0$ (black dotted, dashed and empty triangle line). Reference thru line for f_0 , $2f_0$ and $3f_0$ (resp. in red dotted and square line, red dotted and circle line and red dotted and empty circle line). $f_0=824 \text{ MHz}$.

Same study has been carried out for the shunt devices in amorphous phase. Results are shown in Fig. 17. The tested shunt device is SH3-W4 (Table IV), with $W=2 \times 16 \mu\text{m}$, $L=1 \mu\text{m}$ and $T=300 \text{ nm}$. Rejection is about 95 dBc at the worst value of 31 dBm. No failure can be observed

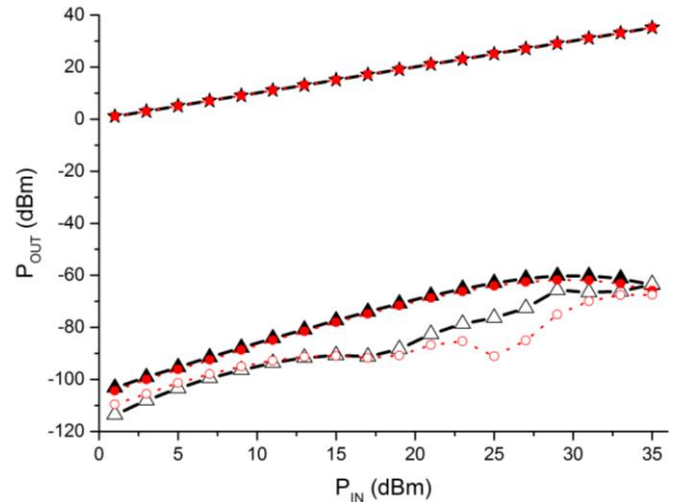


Fig. 17. Shunt device in ON-state (amorphous phase). Measurement of P_{OUT} versus P_{IN} at fundamental frequency f_0 (black dotted, dashed and star line), at $2f_0$ (black dotted, dashed and triangle line) and $3f_0$ (black dotted, dashed and empty triangle line). Reference thru line for f_0 , $2f_0$ and $3f_0$ (resp. in red dotted and square line, red dotted and circle line and red dotted and empty circle line). $f_0=824 \text{ MHz}$.

V. COMPARISON WITH THE STATE-OF-ART

The study presented so far in this paper was focused on giving general design rules for GeTe-based switches on the basis of empirical models confirmed through simulations. A compromise has to be made which will be discussed as a general conclusion. Never-the-less many devices were tested and Table I presents the more striking results relative to the state-of-the-art. Insertion loss and isolation are of major

importance leading to the presentation of large, thick but short devices as SE3-W4 and SH3-W4. Also the entire measurement campaign has been performed on those latter's which is not the case for others.

Our device benefits from direct heating: low capacitance due to the lack of heater leading to higher cut-off frequency, low DC programming cycle time leading to lower energy consumption. To the authors' mind, anyway, direct heating should be dedicated to move from crystalline to amorphous phase only, thus avoiding heater ageing but it may be not appropriate to move from amorphous to crystalline phase as the presence of one conductive nucleated filament may prevent from the crystallization of the whole device (only a small part of the PCM is crystallized). Also programming current may be high with direct heating. In the future, we will try to optimize programming current consumption and make cycling measurements.

VI. CONCLUSION

GeTe phase change material was used to realize RF switches with direct heating. Direct heating enables low energy consumption and prevents heater from ageing. However, a solution based on indirect heating for crystalline transition and direct heating for amorphization should be preferable.

The GeTe switches proposed here-in are categorized according to two configurations: shunt or series. In both cases, many designs were proposed with geometrical variations of the GeTe, in width, thickness and length. This large variety of devices enabled the authors to propose models in order to help future designers.

A small signal analysis from 40 MHz up to 50 GHz enabled, in both configurations, to draw the equivalent circuits, to derive insertion loss and isolation, and to estimate FoM, in terms of cut-off frequency, comparable or overpassing the state-of-the-art, depending on the configuration. Shunt configuration has to be favored for isolation while series one is more suited for extremely low insertion loss. As an example, measurement results confirm the small resistance due to the GeTe thickness (300 nm), with a R_{ON} resistance equal to 1.1 Ω while keeping good performance at the OFF-state with an equivalent capacitance of 6.8 fF, leading to a global FoM of 21 THz. The compromise concerning GeTe dimensions is well known for small signal analysis. It goes in favor of an optimized device for the switch ON-state, that is to say in series configuration a large, short and thick GeTe, while in shunt configuration, a minimized shunt parasitic capacitance is awaited. In OFF-state, in series configuration, the parasitic capacitance has to be minimized as well while in shunt configuration, a large, short and thick GeTe improves isolation without degrading the ON-state insertion loss.

Power-handling measurements were also carried out and confirmed that amorphous phase limitation is due to a threshold electric field of 12.6 V/ μm [18]. A very detailed approach was proposed concerning power handling of the crystalline phase. Some design laws were derived for the very first time, confirmed by thermal multi-physics simulations. It is

interesting to note that the maximum current before failure is proportional to the GeTe width, the square root of its thickness and inversely proportional to its length, in both configurations. A compromise has thus to be considered concerning the length, as a larger length enables more power handling during amorphous phase but a smaller length is preferable for power handling during crystalline phase. In accordance with small analysis conclusion, an advice would be not to shorten length anymore as long as insertion loss fits the specifications.

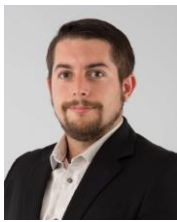
Moreover, a power handling balance is presented between series and shunt devices, showing that series configuration is preferred for crystalline phase and shunt configuration for amorphous phase.

Finally, no linearity constraint could be underlined for those passive devices.

REFERENCES

- [1] M. Jaffe et al, "Improvements in SOI Technology for RF Switches," in *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuit in RF Systems (SiRF)*, 26-28 Jan. 2015.
- [2] H. Mizutani et Y. Takayama, "DC-110-GHz MMIC travelling-wave switch," *IEEE Trans. on Microwave Theory and Techn.*, vol. 48, no 5, p. 840-845, May 2000.
- [3] Y. Jin et C. Nguyen, "Ultra-Compact High-Linearity High-Power Fully Integrated DC-20-GHz 0.18 μm CMOS T/R Switch," *IEEE Trans. on Microwave Theory and Techn.*, vol. 55, no 1, p. 30-36, Jan. 2007.
- [4] K. Y. Lin, W.-H. Tu, P.-Y. Chen, H.-Y. Chang, H. Wang, et R.-B. Wu, "Millimeter-wave MMIC passive HEMT switches using traveling-wave concept," *IEEE Trans. on Microwave Theory and Techn.*, vol. 52, no 8, p. 1798-1808, Aug. 2004
- [5] D. Kelly, C. Brindle, C. Kemerling, et M. Stuber, "The state-of-the-art of silicon-on-sapphire CMOS RF switches," in *IEEE Compound Semiconductor Integrated Circuit Symposium, CSIC '05*, 2005.
- [6] F. Souchon, et al., "Thin film Packaged Redundancy RF MEMS Switches for Space Applications," in *IEEE 19th International Conference on Solid-State Sensors, Actuators and Microsystems, Transducers*, Taiwan, 18-22 June 2017.
- [7] R. Chan, R. Lesnick, D. Becher, et M. Feng, "Low-actuation voltage RF MEMS shunt switch with cold switching lifetime of seven billion cycles," *Journal of Microelectromechanical Systems*, vol. 12, no 5, p. 713-719, Oct. 2003.
- [8] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Nanoscale memristive radiofrequency switches," *Nat. Commun.*, vol. 6, 2015.
- [9] M. Purushothama, A. Vena, B. Sorli, and E. Perret, "Nafion Based Fully Passive Solid State Conductive Bridging RF Switch," *IEEE Microw. Wireless Comp. Letters*, vol. 27, pp. 1104-1106, 2017.
- [10] J. A. Nessel, R. Q. Lee, C. H. Mueller, M. N. Kozicki, M. Ren, et J. Morse, "A novel nanoionics-based switch for microwave applications," in *2008 IEEE MTT-S International Microwave Symposium Digest*, 2008, p. 1051-1054.
- [11] P. Borodulin, et al., "Recent Advances in Fabrication and Characterization of GeTe-based Phase-change RF Switches and MMICs," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 4-9 June 2017.
- [12] M. Wang, and M. R. Rais-Zadeh, "Directly Heated Four-Terminal Phase Change Switches," in *2014 IEEE MTT-S International Microwave Symposium (IMS)*, 1-6 June 2014.
- [13] M. R. King, et al., "Morphological analysis of GeTe in inline phase change switches," *Journal of Applied Physics*, vol 118, issue 9, Sept. 2015.
- [14] J.-S. Moon, et al., "11 THz Figure-of-Merit Phase-change RF Switches for Reconfigurable Wireless Front-ends," in *2015 IEEE MTT-S International Microwave Symposium (IMS)*, 17-22 May 2015.
- [15] A. Mennai, et al., "Bistable RF Switches Using Ge₂Sb₂Te₅ Phase Change Material," in *2015 IEEE European Microwave Conference*, Paris, 6 - 11 Sept. 2015.

- [16] H. Lo, et al., "Three-Terminal Probe Reconfigurable Phase-Change Material Switches," *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 312–320, Jan. 2010.
- [17] A. Leon, et al., "In-depth characterization of the structural phase change of Germanium Telluride for RF switches," in *Advanced Materials and Process for RF and THz Applications (IMWS-AMP)*, Pavia, Italy, 20–22 Sept. 2017.
- [18] N. El-Hinnawy, et al., "Origin and Optimization of RF Power Handling Limitations in Inline Phase-Change Switches," in *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3934–3942, Sept. 2017.
- [19] J.-S. Moon, et al., "10.6 THz Figure-of-Merit Phase-change RF Switches with Embedded Micro-heater," in *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuit in RF Systems (SiRF)*, 26–28 Jan 2015.
- [20] S. H. Hawasli, et al., "Investigation of on-state power handling dependence on number of cycles for germanium telluride RF switches," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 292–295.
- [21] A. Botula, et al., "A Thin-film SOI 180nm CMOS RF Switch Technology," in *Silicon Monolithic Integrated Circuits in RF Systems*, San Diego, CA, USA, Jan 2009.



Alexandre Léon received the Eng. Dipl. degree in electrical engineering from the Ecole Nationale Supérieure d'Electronique, d'Electrotechnique, d'Informatique, d'Hydraulique, et des Télécommunications, Toulouse, France, he is currently PHD student in Université Grenoble Alpes and works with CEA-LETI, France.



Bruno REIG received his PhD degree in electronic from Pierre & Marie Curie university, Paris, France in 1999. From 1995 to 2004 he was involved in the development of advanced packaging solutions for microwave modules as a research engineer at Thales Research and Technology France. In 2004 he joined the MicroSystem Components Section at CEA-LETI, Grenoble, France where he was implied in the design, realization and characterization of RF MEMS switches and NEMS sensors. He also participated to the development of integrated mmW circuits design on advanced CMOS SOI technology. He is currently working on RF components and packaging solutions as a CEA expert and project manager.



Etienne Perret (S'02–M'06–SM'13) received the Eng. Dipl. degree in electrical engineering from the Ecole Nationale Supérieure d'Electronique, d'Electrotechnique, d'Informatique, d'Hydraulique, et des Télécommunications, Toulouse, France, 2002, and the M.Sc. and Ph.D. degrees in electrical engineering from the Toulouse Institute of Technology, Toulouse, in 2002 and 2005, respectively. From 2005 to 2006, he held a post-doctoral position with the Institute of Fundamental Electronics, Orsay, France. Since 2006, he has been an Associate Professor of electrical engineering with the University of Grenoble Alpes - Grenoble Institute of Technology, Grenoble, France. Since 2014, he has been a Junior Member with the Institut Universitaire de France, Paris, France, an institution that distinguishes professors for their research excellence, as evidenced by their international recognition. Since 2015, he has been an Appointed Member of the French National Council of Universities. He has authored or co-authored over 150 technical conferences, letters and journal papers, and books and book chapters. He holds several patents. His works have generated about 2000 citations. His current research interests include electromagnetic modeling of passive devices for millimeter and submillimeter-wave applications, and wireless communications, especially RFID and chipless RFID, and also include advanced computer-aided design techniques based on the development of an automated codesign synthesis computational approach. Dr. Perret is a Technical Program Committee member of the IEEE International Conference on RFID. He was a recipient of the French Innovative Techniques for the Environment Award in 2013, the SEE/IEEE Leon Brillouin Award for his outstanding achievement in the identification of an object in an unknown environment using a chipless label or tag in 2016 and the IEEE MTT-S 2019 Outstanding Young Engineer Award. He was a Keynote Speaker and the Chairman of several international symposiums. He was named one of the MIT

Technology Review's French Innovator's under 35 for his work on chipless RFID in 2013. Etienne Perret was awarded an ERC Consolidator Grant in 2017 for his project ScattererID.



Florence Podevin received the grade of engineer in electronics and microelectronics from the engineering school Centrale Lille in 1998, the M.Sc degree in electronics and microelectronics from the Université des Sciences et Technologies de Lille (USTL) in 1998 and the Ph.D. degree in microelectronics from USTL, in 2001. In 2001, she joined the Institute of Microelectronics, Electromagnetism and Photonics (IMEP, IMEP-LAHC) in Grenoble as an assistant professor. She is now associate professor at the Laboratory of RadioFrequency Integrated Circuits of the University Grenoble-Alpes. Her main research interest concerns tunable and miniaturized devices, such as phase shifters, power dividers, couplers, or co-design between passive and active devices with some interest on distributed amplifiers. She benefits from a great experience in terms of slow-wave transmission lines, at millimeter-wave frequencies, in CMOS and BiCMOS technologies or on advanced substrates dedicated to millimeter-waves. She authored or co-authored more than 100 papers published in international journals and national or international conferences, and co-holders 3 patents.



Damien Saint-Patrice received the M.S. degree in materials science from the Polytech'Clermont-Ferrand, Aubière, France, in 2006. He has been with CEA-LETI, Grenoble, France, since 2007. From 2007 to 2013, he worked on advanced packaging technologies as research engineer. Since 2014, he works as process integration engineer on MEMS devices.



Vincent Puyal received the B.S. degree in electronics engineering from Polytech'Montpellier, University of Montpellier II, France, in 2002, and the Ph.D. degree in microelectronics engineering from the University of Montpellier II, France, in 2007. From 2002 to 2006, he was involved with the design and testing of high-speed bipolar integrated circuits (ICs) for optical communication systems in collaboration with the LIRMM, Montpellier, France and Alcatel-Thales III-V Lab, Marcoussis, France. From 2007 to 2011, he was RF MEMS component and IC research engineer at the CNRS LAAS, University of Toulouse, France. In 2011, he joined the CEA LETI in Grenoble, France. His current research interests include RF and mmW Front-End Si ICs, EM and signal integrity modeling on SiP and high performance Back-End RF and mmW switches.



Jose Lugo-Alvarez received his PhD degree in Radiofrequency (RF) from the Université Grenoble-Alpes, Grenoble, France in 2015. Since 2016 he has been in the MicroElectronic Components Section at CEA-LETI, Grenoble, France as a RF Research Engineer. His current research interests include small- and large-signal characterization, modeling and optimization of active devices and semiconductor substrates toward RF applications in CMOS advanced technologies.



Philippe Ferrari received the Ph. D. degree from the "Institut National Polytechnique de Grenoble" (INPG), France, in 1992, with honors. Since 2004, he is a professor at the University Grenoble Alpes, Grenoble, France. His main research interest concerns tunable and miniaturized devices, such as filters, phase shifters, matching networks, couplers, power dividers and VCOs. These devices are developed in many technologies, PCB, CMOS/BiCMOS, and nanowires, at RF and mm-wave frequencies. He has worked towards the development of slow-wave CPW, and developed new topologies of slow-wave transmission lines, based on microstrip lines and SIWs, respectively. He is author or co-author of more than 200 papers published in international journals or conferences, and co-holder of six patents. He is an IEEE senior member, a member of the Editorial Board of the International Journal on RF and Microwave Computer-Aided Engineering (Wiley), and an Associate Editor of the International Journal of Microwave and Wireless Technologies (EuMA).