Subthreshold Drain current hysteresis of planar SiC MOSFETs

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4H-SiC MOSFETs are available in the market as discrete devices or power modules. These devices present many advantages for power conversion compared to Si IGBTs but still suffer from some (reliability) drawbacks [1-3]. The Vth instability of SiC MOSFETs is topic that mainly focuses on permanent drift of the Vth. Recoverable enhancement of the drain current in the subthreshold domain has been pointed out formerly for SiC MOSFETs [4] and is becoming a trending topic since it may affect the device stability. This phenomenon is not completely unknown since it affects Si devices as ell [5], but the Wide Band Gap of SiC enhances this effect and can produce a shift of the Vth up to several volts. As a matter of fact, hysteresis can make the devices switch faster, which could be an advantage to normal operation, but it can also make the devices switch on at lower gate bias, thus making them prone to undesired switching and leading to short circuit failure. Another problem can arise in the case of short-circuit, since the drain current will attain higher values and thus putting the device to higher thermal stress.

4H-SiC MOSFETs drain current subthreshold hysteresis can range from several tens of millivolts to several volts depending on the structure of the device. They are usually attributed to slow interface states that capture holes when the gate is negatively biased [4,6]. In this paper we will focus only on the Vth subthreshold Hysteresis of planar MOSFETs through measurements and TCAD simulation. This will give a better understanding of the role of the interface states in this phenomenon.

The subthreshold drain current depends strongly on the prior state of the device. In the subthreshlod domain, for same value of drain current we need higher gate bias when going from on-state to off-state than vice versa. Once the gate is biased above the Vth voltage, the drain current doesn't depend on the previous state anymore. This behaviour is illustrated in figure 1, where depending on the off-state starting voltage the subthreshold drain current can be almost 2 decades higher. The measurements in figure 1 were performed at room temperature, whereas figure 2 shows the hysteresis as a function of off-state starting gate bias voltage for several temperatures. The hysteresis decreases for higher temperature and is probably due to an acceleration of capture-emission mechanisms near the interface. To validate this hypothesis, the dependence of the surface potential on the gate bias voltage was extracted from C(V) measurements. C(V) measurement at different temperatures are shown in figure 3, where one can see that the Vfb is slightly shifted whereas the Vth stays the same. The extracted surface potential indicates a very low Vfb voltage which is certainly due to the difference of the workfunctions and probably the positive fixed charge in the oxide. The surface potential shows the band bending near the interface and can be related to the Fermi level near the interface. Since the occupancy of traps depends on the position of the Fermi level, one can predict the nature of the traps, donors or acceptors, and the capture/emission mechanisms happening at the interface. For a better assessment of the role of the interface states in the hysteresis phenomenon TCAD simulations have been performed. The simulated structure is shown in figure 5, whereas the simulated C(V) curves for different types of traps are shown in figure 6. The final paper will contain other measurements and will explain the dynamics of the phenomenon. All of these data may help manufacturers fine tune their device processing in order to avoid this undesired phenomenon.

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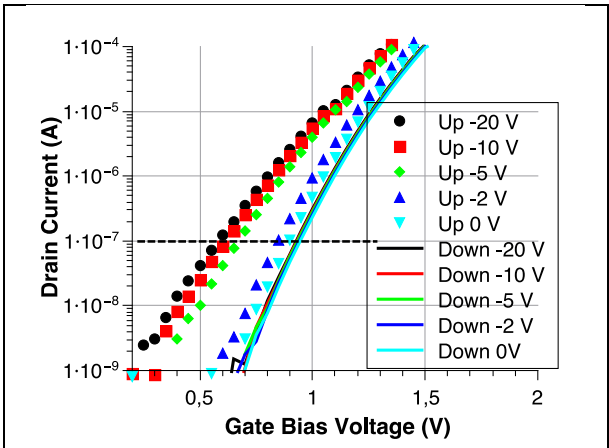

Fig. 1 – Drain current subthreshold hysteresis of commercial 900 V planar SiC MOSFET.

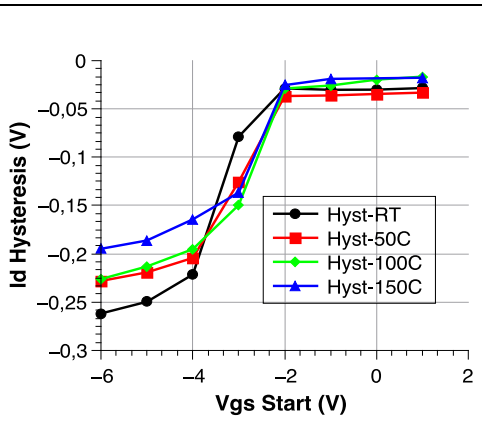

Fig. 2 – Temperature dependence of the drain current subthreshold hysteresis of 900 V SiC MOSFET extracted at 100 nA.

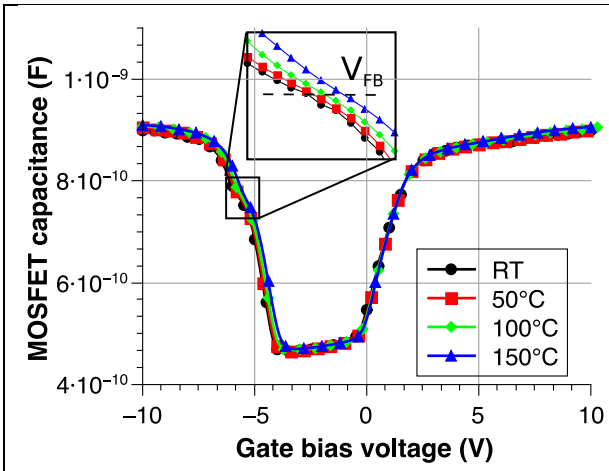

Fig. 3 – 4H-SiC planar MOSFET capacitance for different temperatures.

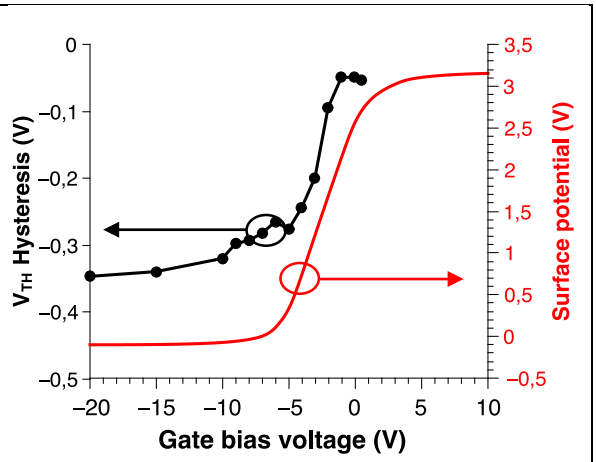

Fig. 4 – 4H-SiC planar MOSFET Vth Hysteresis and the corresponding surface potential as a function of the gate bias voltage.

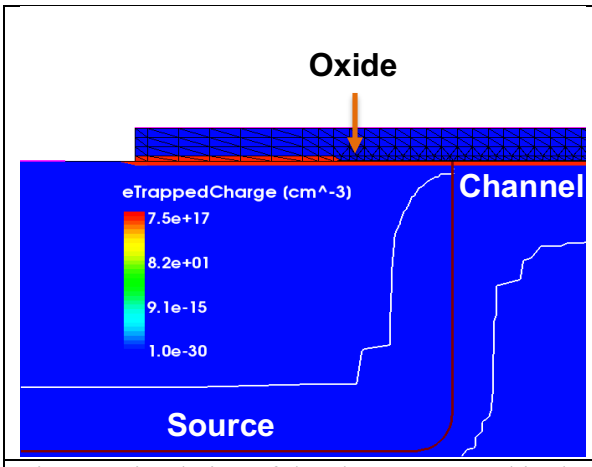

Fig. 5 – Simulation of the charge captured in the interface traps of a 4H-SiC planar MOSFET

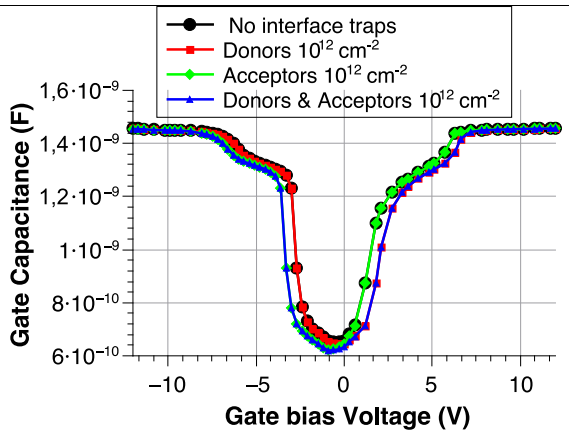

Fig. 6 – C(V) simulation of the effect of the interface traps in a planar 4H-SiC MOSFET.