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High-Voltage SiC-JFET Fabrication and Full Characterization

B. Asllani¹, P. Bevilacqua¹, A. Zaoui¹, G. Grosset², D. Planson¹ and H. Morel¹

¹) Univ Lyon, INSA Lyon, CNRS, AMPERE, F-69621 Villeurbanne, France

²) ION BEAM SERVICES, F-13790 PEYNIER, France

herve.morel@insa-lyon.fr

Silicon Carbide (SiC) enables to develop high-voltage devices. The present study focuses on JFETs. The targeted rating was 3300 V, 20 A.

To reach these characteristics a vertical structure with vertical and lateral channels was designed as shown in Fig. 1. The lateral channel enables an easy design with a low absolute value of the gate-source threshold voltage. It is easier to manufacture but yields a higher on-state resistance (R_{ON}) in comparison with a pure vertical channel.

Devices are fabricated on a n-type epitaxial layer (supplied by Showa Denko) with a thickness of 32.7 μm and a doping concentration of $9.7 \times 10^{14} \text{ cm}^{-3}$. 13 photolithography mask levels were used. A double gate structure one buried gate fabricated by ion implantation and a surface gate obtained by epitaxy regrowth. The edge termination of the JFETs includes a MESA structure and junction termination extension (JTE). The front side and back side metalizations are in Ag. The second passivation uses polyimide.

Electrical characteristics	Die dimensions (mm)	Source pad dimensions (mm)	Gate pad dimensions (mm)
3300V/20A	5,8 x 5,8	3,91x2,21	0,96x0,96

Best dies were diced and packaged to enable high current measurements. The packaging was an optimization of Iso4 standard package made by DeepConcept Company as shown in Fig. 2. The size is the same but the internal design is optimized for SiC and for 3300 V voltage. The package can operate up to 200°C. In this case, the support is a metal one: (Cu, Al + termination Ni, Au, Ag).

The electrical characterization includes: standard static characteristics as the output characteristic (Fig. 3), the transfer characteristic, dynamic characteristics like C_{rss} , C_{iss} . For such standard characterization a Keysight B1506A curve tracer was used. An IWATSU CS-5400 curve tracer was used for measuring the on-resistance versus the temperature. A specific test-bench for high voltage double pulsed test was used for the switching characterization (Fig. 4) and the associated turn-on and turn-off switching energy.

The final paper will present with further details, the main device characteristics for a datasheet like construction, the measurement protocols, and the associated test benches. Moreover turn-on and turn-off switching losses will be included in the range 500 V – 2000 V.

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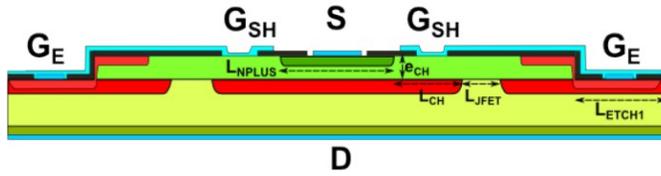


Fig. 1: Schematic of the designed JFET structure

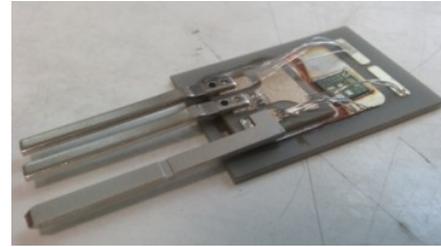


Fig. 2: A JFET die on its package

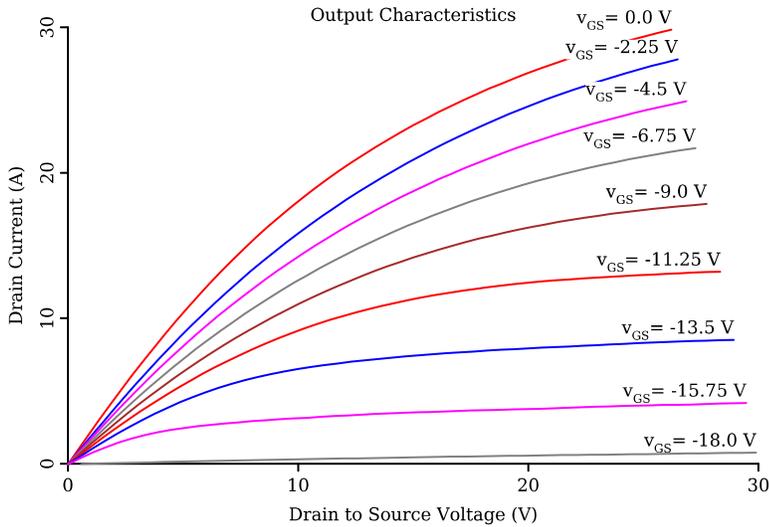


Fig. 3: Output Characteristics @ 25 °C – 32-J4 - B1506

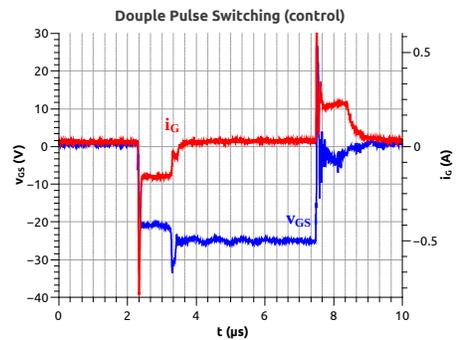
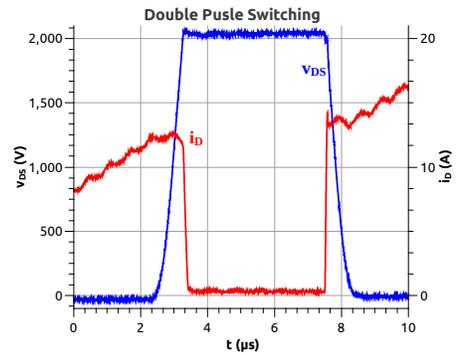


Fig. 4: Double pulse test measurements 2 kV, ~ 12 A

Parameter	Symbol	Conditions	Min	Avr	Max	Units
Drain-source voltage	V_{DS}			2000		V
Gate-Source voltage	V_{GS}			-20 to 2		V
Continuous drain current	i_D	$T_J=150\text{ }^\circ\text{C}$		13		A
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{ V}$, $T_J=25\text{ }^\circ\text{C}$, $i_D = 1\text{ mA}$	1950	2650	3300	V
Drain-source on-resistance	R_{DS}^{ON}	$V_{GS} = 0\text{ V}$, $T_J=25\text{ }^\circ\text{C}$, $i_D = 5\text{ A}$	0.49	0.52	0.58	Ω
Gate threshold voltage	V_{TH}	$V_{DS}=20\text{ V}$, $i_D = 100\text{ mA}$	-18.5	-18	-17.2	V
Input capacitance	C_{ISS}	$V_{GS} = -20\text{ V}$, $V_{DS} = 100\text{ V}$, $T_J=25\text{ }^\circ\text{C}$,		1470		pF
Output capacitance	C_{OSS}			170		pF
Reverse transfer capacitance	C_{RSS}			160		pF
Thermal resistance, junction-to-case	R_{TH}^{JC}		Estimated		0.26	