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# Extraction of the 4H-SiC/SiO<sub>2</sub> Barrier Height Over Temperature

O. Aviñó-Salvadó, *Member, IEEE*, B. Asllani, C. Buttay, *Senior Member, IEEE*, C. Raynaud, H. Morel, *Senior Member, IEEE*

**Abstract**—The behaviour of the barrier height of the SiC/SiO<sub>2</sub> interface has been investigated over a wide temperature range, from 173 to 523 K. These data complement literature, providing a better knowledge of this parameter, which was studied only over a more restricted temperature range, and never before for low temperatures. It is highlighted that measured samples exhibit a barrier height temperature dependence very near to the theoretical one ( $\approx -0.7$  meV K<sup>-1</sup>). Beyond 473 K the barrier height seems to drop faster for some samples, reaching  $\approx -1.4$  meV K<sup>-1</sup>. Should this faster decreasing rate be maintained for higher temperatures, it could limit 4H-SiC MOSFETs performances or reliability for high temperature applications.

It is expected that the data provided here will allow for a more accurate modelling of the gate current and of the charge injection in the oxide layer of power MOSFETs, leading to more reliable predictions of the oxide lifetime for 4H-SiC MOSFETs.

**Index Terms**—Barrier height, SiC/SiO<sub>2</sub>, Temperature, Fowler-Nordheim, Oxide, Robustness

## I. INTRODUCTION

THE study of the barrier height ( $\Phi_b$ ) at the SiC/SiO<sub>2</sub> interface of 4H-SiC MOSFETs over a wide temperature range is highly interesting from a double point of view: for a better modelling of  $\Phi_b(T)$ , but also regarding the reliability of the gate oxide. Indeed, the barrier height plays a major role in carrier transport mechanisms through the oxide, which cause the degradation of the dielectric and eventually its destruction [1]. The main electrode-limited conduction mechanisms are [2] i) Direct tunneling (DT), ii) Fowler-Nordheim (FN) tunnel injection, iii) Schottky emission.

If the electric field is large enough, the electron wave function may pass across the triangular barrier towards the conduction band of the dielectric (FN tunnel injection). Otherwise, carriers will cross the entire oxide thickness (DT injection). Both mechanisms are depicted in fig. 1, together with Schottky and Poole-Frenkel (PF, addressed later) phenomena. Schottky or thermionic conduction is a temperature enhanced mechanism, as can be deduced from eq. 1: with sufficient thermal energy, electrons can overcome the energy barrier between the semiconductor and the dielectric conduction bands. *Boige et al.* showed (in SiC power MOSFETs) that this carrier transport phenomenon only becomes predominant for temperatures above 700 K [3].

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$$I_{SCH} \propto T^2 e^{-\frac{c \sqrt{F_{ox}}}{T}} \quad (1)$$

Moreover, it is well known that for dielectrics (SiO<sub>2</sub>) thicker than 5 nm, Fowler-Nordheim tunnel injection is predominant over direct-tunneling [4]. This is the case for the oxide layer of SiC power MOSFETs. Therefore, FN tunneling is expected to be the main transport mechanism encountered in the present work. FN current density (eq. 2) can be calculated depending on the temperature ( $T$ , [K]) and the electric field in the oxide ( $F_{ox}$ , [V·m<sup>-1</sup>]), when a degenerate semiconductor is used as emitter electrode, using the tunnel transparency  $T(F_{ox}, E)$  and assuming that electron behaviour in the emitter can be described by a three-dimensional Fermi-gas [5, 6].

$$J_{FN}(F_{ox}, T) = \frac{4\pi m_{SiC} k T}{h^3} \int_0^\Phi T(F_{ox}, E) \cdot f(T, E) \cdot dE \quad (2)$$

$$f(T, E) = \ln \left[ 1 + \exp \left( \frac{E_F(T) - E}{kT} \right) \right]$$

$$T(F_{ox}, E) = \exp \left( -\frac{4\sqrt{2m_{ox}}(\Phi - E)^3}{3hqF_{ox}} \right)$$

where  $J_{FN}$  is the current density [A·m<sup>-2</sup>],  $q$  is the electron charge [C],  $E_F$  is the Fermi energy,  $\Phi$  is the electron affinity [eV] between the semiconductor and SiO<sub>2</sub>,  $m_{SiC}$  and  $m_{ox}$  are the effective electron mass in SiC and SiO<sub>2</sub> [kg] respectively and  $h$  and  $k$  are the Plank and Boltzmann constants. The 4H-SiC/SiO<sub>2</sub> barrier height can be defined [5] as follows:

$$\Phi_b = \Phi - E_F \quad (3)$$

*Lenzlinger and Snow* [7] introduced the zero temperature approximation of eq. 2 at 0 K, which is the most commonly used expression of  $J_{FN}$  in the literature. This yields:

$$J_{FN}^{0K} = A F_{ox}^2 e^{-\frac{B}{F_{ox}}}, \quad (4)$$

$$\text{with } A = \frac{q^3 m_{SiC}}{8\pi h m_{ox} \Phi_b}, \quad B = \frac{8\pi \sqrt{2m_{ox}} \Phi_b^3}{3qh},$$

The value of  $m_{ox}$  is  $m_{ox} = 0.42 \cdot m_0$  [7], where  $m_0$  is the free electron mass, and  $m_{SiC} = 0.29 \cdot m_0$  [8]. The barrier height  $\Phi_b$  is expressed in eV.

Other types of carrier transport have to be taken into account, in particular bulk-limited mechanisms. Recently,

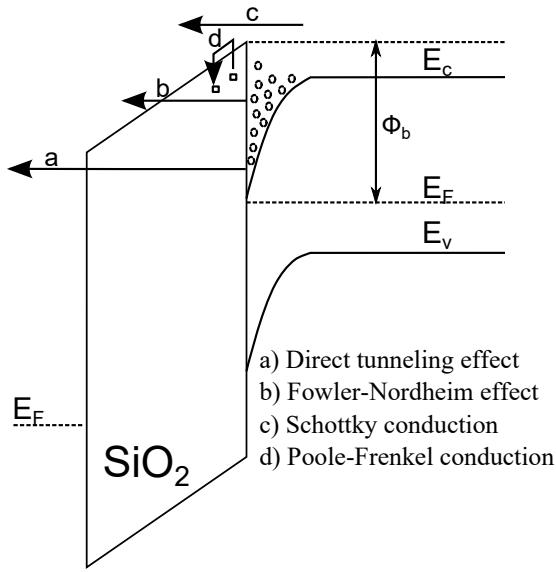


Fig. 1. Qualitative band diagram of a N-MOSFET (strong inversion) and the main injection phenomena to the oxide.

*Sometani et al.* stated that the Poole-Frenkel effect could become the governor transport mechanism for temperatures above 300 K due to "the existence of carbon-related defects and/or oxygen vacancy defects" [9]. PF is a trap-assisted mechanism (eq. 5, where  $\phi_t$  is the barrier height from the trap states and  $C$  is a constant) enhanced by temperature and electric field. This describes (see fig. 1) how trapped electrons can be detrapped by both thermal and electric field excitation, reaching the conduction band of the dielectric. In this work, the apparition of this phenomenon has been ruled out; further details are given in section III.

$$J_{PF} = C \cdot F_{ox} e \frac{q \cdot (\phi_t - \sqrt{qF_{ox}/(\pi \epsilon_0 \epsilon_{SiO_2})})}{kT} \quad (5)$$

Even if most publications [10, 11, 12, 13, 14] use eq. (4) to estimate the FN current, this model shows some limitations, as stated by *Pananakakis et al.* [5] for temperatures above 523 K in silicon devices. This is obvious because most of the parameters, such as the bandgap (and therefore the barrier height) or the SiO<sub>2</sub> and Si (SiC) effective masses are in reality temperature-dependent [15, 16]. For this reason, we limited our measurements to 523 K.

Si/SiO<sub>2</sub> interfaces have been largely studied and the barrier height dependence on temperature has been discussed in many papers [5, 17, 18]. Much fewer papers address the 4H-SiC/SiO<sub>2</sub> interfaces, and they only investigate it over a limited temperature range [14, 13, 12, 10, 19].

*Agarwal et al.* (1997) [14] extracted  $\Phi_b$  at 298, 423 and 598 K for MOS capacitors fabricated with 4H- and 6H-SiC polytypes from current-voltage (IV) measurements on the gate. These were then fitted by a classic Fowler-Nordheim current model [7, 6]. They reported that the SiC/SiO<sub>2</sub> barrier height is more dependent on temperature than the Si/SiO<sub>2</sub> interface, which shows more stable values. On the contrary, *Kimoto et al.* [20] reported a better thermal stability of the SiC/SiO<sub>2</sub>

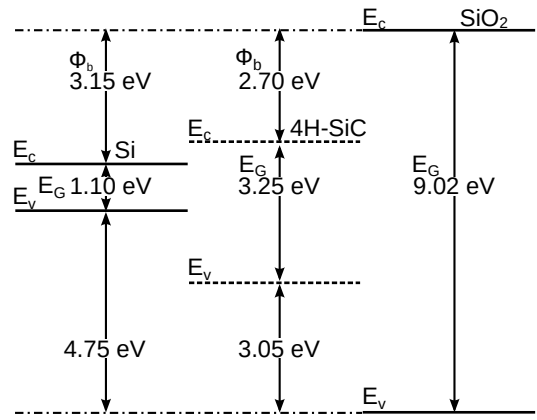


Fig. 2. Energy band diagrams for Si, 4H-SiC and SiO<sub>2</sub> and barrier heights from semiconductor to SiO<sub>2</sub> gate [22, 21].

interface. The value obtained [14] for the "effective" barrier height ( $\Phi_{eff}$ ) at 298 K (2.43 eV) was noticeably lower than the theoretical one (2.7 eV). Other authors such as *Waters* (2000) found even lower values [10] ( $\Phi_{eff}$ =1.92 eV at room temperature). The barrier height  $\Phi_b$  is often renamed  $\Phi_{eff}$ , the effective barrier height. However  $\Phi_{eff}$  can be different from the theoretical  $\Phi_b$  due to uncertainties on effective masses of carriers, presence of interface traps, or other factors such as oxide non-homogeneities.

In 2010, *Yu et al.* [11] extracted  $\Phi_{eff}$ =2.57 eV at 296 K and 2.36 eV at 473 K in MOS capacitors. In 2011, *Le-Huu et al.* published, to our knowledge, the most complete study on the SiC/SiO<sub>2</sub> barrier height so far. They estimated barrier height values ranging from  $\Phi_{eff}$ =2.68 eV at 298 K to  $\Phi_{eff}$ =2.42 eV at 523 K (see table I). More recently (2018), a study [13] on Wolfspeed's 4H-SiC, 1200V, Gen3 N-MOSFETs reported a  $\Phi_{eff}$ =2.83 eV at 423 K.

The noticeable differences between the reported barrier height values can in particular be explained by the presence of trapped charges at the interface (interface states) or in the vicinity of the interface in the oxide (oxide border traps or near interface traps) [21]. Thus, values closer to the theoretical one (2.7 eV) suggest an improvement in the oxide interface quality.

Regarding reliability, the higher bandgap of SiC (compared to Si, see fig. 2), instead of being an advantage can paradoxically become one of its main drawbacks [23]. Indeed, a greater bandgap allows to block higher voltages. But at the same time FN tunnel injection in the oxide of SiC MOSFETs is stronger due to the lower barrier height between SiC and SiO<sub>2</sub>. As it is well known [24], FN tunnel injection is one of the main reliability issues in SiC MOSFETs, and this phenomenon becomes more intense as the temperature increases, because the barrier height decreases [14]. Moreover, the presence of occupied interface states might also contribute to decreasing the barrier height further. Therefore, the reliability of the oxide may be seriously compromised [23]. This is especially important regarding the high temperature use of SiC MOSFETs [24], contrarily to what many authors initially expected [25]. However, this topic is not closed. Recent improvements [26, 27] in the manufacturing process of SiC MOSFETs have lead to an important reduction in the density of defects at the SiC/SiO<sub>2</sub>

interface. For example, *Yu et al.* [11] estimated lifetimes of up to 100 years at  $4 \text{ MV cm}^{-1}$  on SiC MOS capacitors, for temperatures up to 648 K.

Other operating conditions, in particular short-circuit and avalanche operation modes [28], may involve FN tunnel injection or Schottky emission. Indeed, when operating under these conditions, a lot of energy is dissipated in the device over a short period of time, causing a great increase of temperature in the oxide, favouring gate current increase. This is evidenced by *Chen et al.* [29], who observed an increase in the gate-source current before failure happened during a short-circuit test and relate this with tunneling current. However, a recent study [3] suggests that Schottky emission may be the predominant phenomenon in this gate current increase.

This paper provides the evolution of  $\Phi_{eff}$  over a large temperature range (from 173 K to 523 K, with 25 K steps). This has not been studied before (only a few values were reported – see table I –, with larger steps), and it is expected that these data will be helpful for a better modelling of the FN current, and thus, for a more reliable oxide lifetime prediction.

## II. METHODOLOGY AND RESULTS

All tests presented in this paper have been performed on commercial 4H-SiC N-MOSFETs C2M008012D [30] from Wolfspeed, based on planar technology [31].  $\Phi_b$  has been calculated using the model of the FN current density described in eq. 4. As introduced in section I, it is expected that FN tunnel injection will be the governor mechanism [4, 3] because of the oxide thickness and temperature range of this experiment.

Two sets of measurements have been run:  $C_{iss}$  (input capacitance) and  $I_G$  (gate current). In both cases, three pristine samples have been characterized (with drain and source terminals short-circuited) using a Keysight B1505A curve tracer.  $C_{iss}$  characterization allows to obtain the main flat-band voltage depending on the temperature. This is used to extract the  $\Phi_{eff}$  in the other three samples. To ensure a good control of the temperature, the experiment has been performed in a cryostat, after a 10 minutes delay once the desired temperature has been reached.

Fig. 3 shows the measured  $I_G$  current over the temperature range. As expected,  $I_G$  increases with temperature. This behaviour is caused by a decrease of the SiC/SiO<sub>2</sub> barrier height, in agreement with the FN current expression (eq. 2).

The measured capacitance  $C_{iss}$  is depicted in fig. 4. As temperature increases, the threshold voltage of the transistors is lowered and the input capacitance  $C_{iss}$  reaches the oxide capacitance  $C_{ox}$  (inversion regime) value for a lower voltage. Also noticeable is the shape of the curve near the flatband voltage ( $\approx -6$  V), which exhibits a "kink" that disappears as temperature increases. These features ("kink" and plateau) may be related to the geometrical structure of the vertical power MOSFET, which differs from the lateral MOSFET considered in microelectronics. However, the most important characteristic for this study is the shift of the capacitance curve between the accumulation and depletion regions, ie. the shift of the flat-band voltage  $V_{fb}$ .

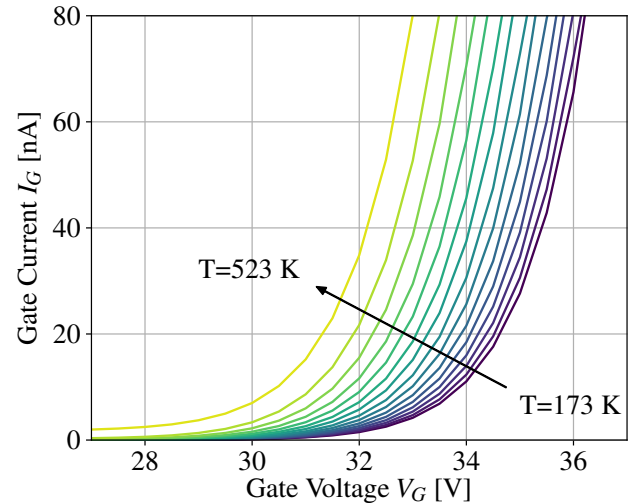


Fig. 3. Characterization of the C2M008012D MOSFET current  $I_G$  over temperature, from 173 K to 523 K. Measurement realized from -5 to 40 V. The current is limited to 100 nA.

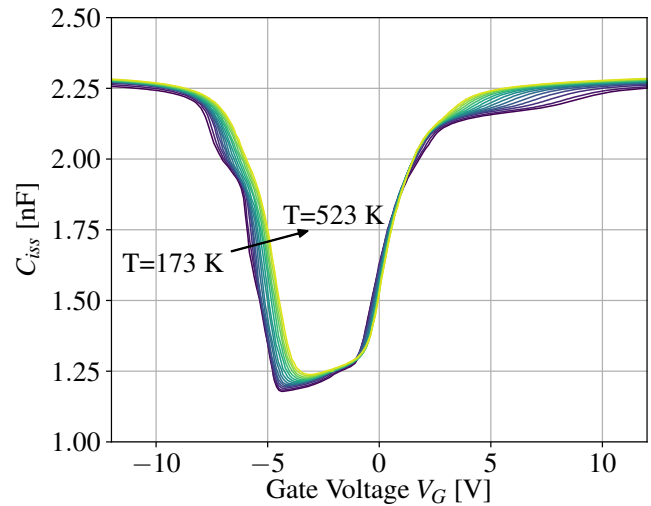


Fig. 4. Characterization of a C2M008012D MOSFET capacitance  $C_{iss}$  over temperature, from 173 K to 523 K. Measurement realized from -12 to 12 V.

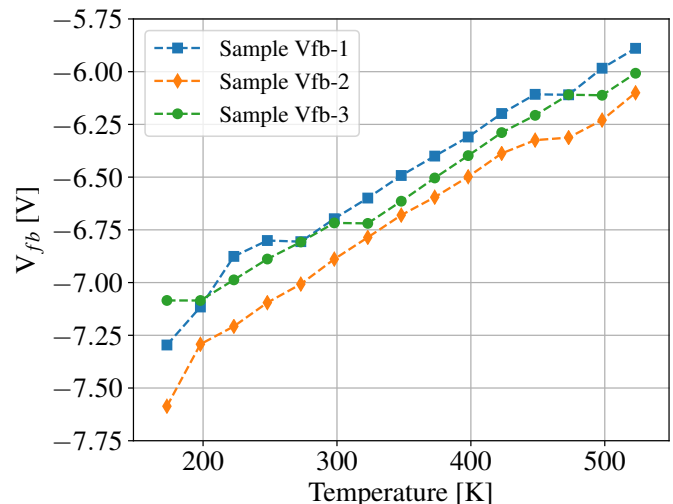


Fig. 5. Evolution of the flat-band voltage over temperature, from 173 K to 523 K, for three C2M008012D MOSFETs.

This feature is important because a change in  $V_{fb}$  results in a change in the oxide electric field (eq. 6) [32, Ch. 5, p. 166]:

$$F_{ox} \approx \frac{V_G - V_{fb} - \psi_s}{t_{ox}} \quad (6)$$

where  $F_{ox}$  is the oxide electric field and  $\psi_s$  is the surface potential. The surface potential has been assumed to be equal to the band gap of the SiC (3.25 eV) since for high inversion conditions the Fermi level at the interface reaches the conduction band. Once it reaches the conduction band, no matter how much we increase the gate bias, the surface potential changes very slowly as any additional charge in the channel has little effect on the Fermi level. Increasing the bias voltage will thus only increase the electric field in the oxide until it breaks down.

Fig. 5 shows the evolution of  $V_{fb}$  vs. temperature, as extracted from the capacitance curves. The extraction methods to obtain the flat-band voltage are largely described in the literature [4, 33]. In the present study, the method described in *Saks et al.* [33] was employed as some device parameters are not given by its manufacturer. The value of the flatband voltage has been extracted at 2 nF (constant capacitance method), which corresponds to the capacitance value at the threshold voltage at room temperature.

To calculate the FN current density ( $J_{FN}$ ), only the oxide thickness  $t_{ox}$  is unknown. However, to obtain the FN current ( $I_{FN} = J_{FN} \cdot S$ ), the gate oxide surface is also required. For an ideal, parallel-plate, MOS capacitor, the relation between the surface (S) and the oxide capacity ( $C_{ox}$ ) is the following:

$$S = \frac{C_{ox} \cdot t_{ox}}{\epsilon \cdot \epsilon_0} \quad (7)$$

where  $\epsilon$  and  $\epsilon_0$  are the relative permittivity (3.9 for SiO<sub>2</sub>) and the vacuum permittivity ( $8.8541 \times 10^{-12}$  F m<sup>-1</sup>), respectively. As it is known [30] that  $C_{rss}$  (reverse transfer capacitance) is about 100 times lower than  $C_{iss}$  (input capacitance) at 30 V, we can assume the following for conditions of strong inversion:

$$C_{iss} \gg C_{rss} \rightarrow C_{ox} \approx C_{gs} \approx C_{iss} \quad (8)$$

Then, eq. 4 to 8 can be recombined, leading to:

$$I_{FN} \approx A \cdot \frac{C_{iss} \cdot t_{ox}}{\epsilon \cdot \epsilon_0} \cdot F_{ox}^2 e^{-\frac{B}{F_{ox}}} \quad (9)$$

with at strong inversion  $C_{iss} \approx 2.3$  nF. At this point, all the parameters involved in  $I_{FN}$  have been extracted or are known, except  $t_{ox}$ , which can then be estimated by matching the theoretical FN current with the measured current  $I_G$ . This has been realized with the measurement of "Sample  $\Phi_1$ " at 423 K, assuming a  $\Phi_{eff} = 2.83$  eV, as reported by Wolfsped researchers on similar devices [13]. A good fitting is obtained for  $t_{ox} = 53.2$  nm, as can be observed in Fig. 6. It is noticeable that  $t_{ox}$  value is consistent with the typical gate oxide thickness reported in the literature [23, 34, 35] for 1200 V SiC MOSFETs ( $\approx 50$  nm).

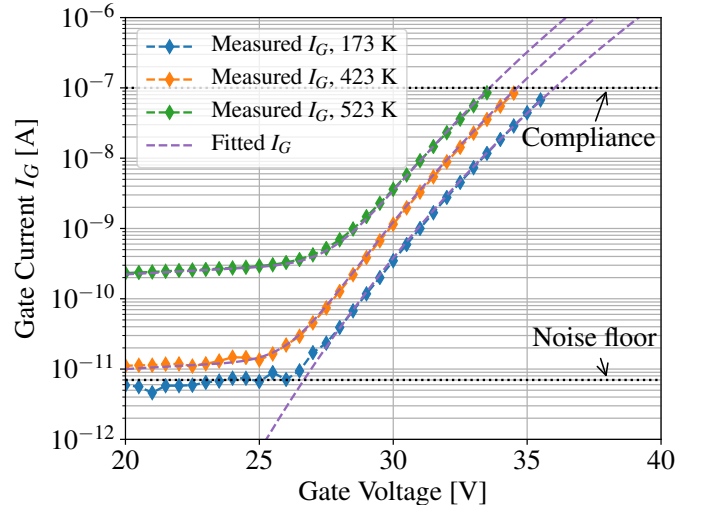


Fig. 6. Measured current  $I_G$  (Sample  $\Phi_1$ ) at 173 K, 423 K and 523 K, fitted with the FN model (eq. 4). A good fit is achieved for an oxide thickness of 53.2 nm. NB: a 100 nA current compliance was set to limit aging of the device and a parallel leakage resistance was considered to model leakage current at the lower electric fields.

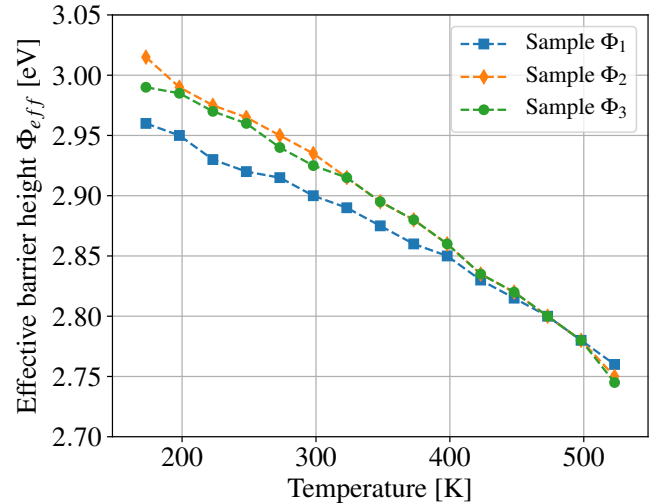


Fig. 7. Extraction of  $\Phi_{eff}$  over temperature, from 173 to 523 K, for three MOSFET samples (Sample  $\Phi_1$ , Sample  $\Phi_2$  and Sample  $\Phi_3$  of table I).

The determination of  $t_{ox}$  from the measurements at 423 K then allows to estimate the effective barrier height evolution with temperature  $\Phi_{eff}(T)$ , fitting the different measurements with the FN current calculation, as all other parameters are known. The resulting values are presented in fig. 7, which highlights the temperature dependence of  $\Phi_{eff}$  vs. temperature for three different samples. The data are summarized in Table I, together with the main values presented in the literature [14, 11, 19, 13]. Obtained results shows a low dispersion. The most plausible explanation is related to errors/uncertainties in the oxide thickness and surface estimation, as well as deviation of these parameters among samples.

### III. DISCUSSION

It can be observed that  $\Phi_{eff}$  values are slightly above the theoretical ones. As this agrees with the reference paper from

TABLE I  
EXTRACTED AND AVERAGE VALUE OF  $\Phi_{eff}$  FOR THE DIFFERENT SAMPLES IN THE TEMPERATURE RANGE 173 K TO 523 K. COMPARISON WITH LITERATURE VALUES [14, 13, 11, 19].

Temperature [K]	173	198	223	248	273	298	323	348	373	398	423	448	473	498	523
Sample $\Phi_1$	2.96	2.95	2.93	2.92	2.92	2.9	2.89	2.88	2.86	2.85	2.83	2.82	2.80	2.78	2.76
Sample $\Phi_2$	3.02	2.99	2.98	2.97	2.95	2.94	2.92	2.90	2.88	2.86	2.84	2.82	2.80	2.78	2.75
Sample $\Phi_3$	2.99	2.99	2.97	2.96	2.94	2.93	2.92	2.90	2.88	2.86	2.84	2.82	2.80	2.78	2.75
Average	2.99	2.98	2.96	2.95	2.94	2.92	2.91	2.89	2.87	2.86	2.83	2.82	2.80	2.78	2.75
Agarwal (1997) [14]						2.43					2.11				
Yu (2010) [11]						2.57							2.36		
Le-Huu (2011) [19]						2.68			2.65		2.59		2.51		2.42
Lichtenwalner (2018) [13]											2.83				

Wolfspeed [13], in which the thickness and the surface area of the samples are known to the authors, the most plausible explanation for these higher  $\Phi_{eff}$  values are uncertainties on many parameters such as: surface area, oxide thickness or on effective mass of the oxide. Notice that other authors have also reported [12, 36] higher  $\Phi_{eff}$  ( $\approx 2.79$  eV) than the theoretical one.

The existence of Poole-Frenkel conduction has been investigated since other groups [9] have reported that for temperatures above 300 K this phenomenon becomes the predominant conduction mechanism. In the case where PF would dominate current transport, one can deduce from eq. 5 that  $\ln(J_{PF}/F_{ox})$ , would be a linear function of  $\sqrt{F_{ox}}$  [37]:

$$\ln(J_{PF}/F_{ox}) = m(T) \cdot \sqrt{F_{ox}} + b(T) \quad (10)$$

Upon verification, the slope parameter  $m(T)$  of eq. 10 extracted from measurements (not presented here for the sake of brevity) does not fit the theoretical values in the range of 173 K to 523 K. Thus PF conduction has been ruled out in the present study. Please note that this finding is not in contradiction with [9], for which no post oxidation annealing is mentioned. On the contrary, with commercial devices, Nitric Oxide Post Oxidation Annealing (NO-POA) is standard procedure in order to lower the density of defects in the oxide near the SiC/SiO<sub>2</sub> interface and enhance the channel mobility [38]. This may increase the distance of the nearest traps from the interface and make it less probable for the electrons to tunnel into and cause Poole-Frenkel conduction.

The behaviour of  $\Phi_{eff}$  shows an almost constant decrease rate for temperatures comprised between 323 and 473 K ( $\approx -0.72$  meV K<sup>-1</sup>). This temperature dependence increases for higher temperatures, with rates ( $\approx -1.13$  meV K<sup>-1</sup>) above 473 K. For lower temperatures,  $\Phi_{eff}$  temperature dependence is slightly weaker, ( $\approx -0.55$  meV K<sup>-1</sup>).

These variations are consistent with the theoretical value ( $-0.7$  meV K<sup>-1</sup>) calculated in ref. [39]. Furthermore, *Fiorenza et al.* [40] calculated the temperature dependence of  $\Phi_{eff}$  using a deposited oxide and compared it to published results obtained on thermal oxides. Their results show that thermal oxides usually exhibit a higher decrease rate of  $\Phi_{eff}(T)$ . This indicates that the devices under study here have a good quality deposited oxide.

The faster decrease of  $\Phi_{eff}$  above 473 K, remains qualitatively consistent with results presented in another publication [19], which indicate a larger decrease of the barrier

height at high temperature ( $\approx -2$  meV K<sup>-1</sup> above 473 K). It has been largely discussed [14, 10, 19], that this can limit the use of SiC at high temperature, as it would require to limit the oxide electric field to ensure reliability. As a result, the on-state resistance of the MOSFET [14] would increase. However, it is noticeable that since the publication of previous studies [14, 10] in 1997 and 2000, the quality of the oxide interface has improved significantly, minimizing interface states and leading to  $\Phi_{eff}$  values much closer to the theoretical ones. Now, we can state that oxide quality continues to improve, minimizing this ratio and getting closer to the theoretical one. For better confidence, the error introduced by the temperature dependence of the effective masses should be studied further, as it has not been taken into account here.

#### IV. CONCLUSIONS

This paper provides  $\Phi_{eff}$  (effective barrier height) values for a wide temperature range, from 173 K to 523 K, for the 4H-SiC/SiO<sub>2</sub> interface (using Wolfspeed C2M008012D MOSFETs).

These values are close to the theoretical ones, indicating that the oxide layer in these devices is of good quality, with few interface defects. A decrease rate of  $\approx -0.7$  meV K<sup>-1</sup> has been observed up to 473 K. Above this temperature  $\Phi_{eff}$  tends to decrease faster, up to  $\approx -1.4$  meV K<sup>-1</sup>. This phenomenon requires further analysis (including effective masses temperature dependence) because may cause an acceleration of the oxide degradation, affecting the expected lifetime of the oxide.

Regarding SiC power MOSFET devices, these values will allow a better modelling of their gate current with respect to temperature, as well as of the charge injected into the oxide. Next studies should focus on i) the evolution of  $\Phi_{eff}$  for higher temperatures and if this could affect reliability models and ii) on Fowler-Nordheim tunneling and Schottky emission in the cases where a high amount of power is dissipated in MOSFET devices (such as short-circuit or avalanche events).

These data can be valuable for power electronics applications, especially on the aeronautic and spatial domains, where devices can operate in a wide temperature range.

#### REFERENCES

- [1] K. Okada, M. Kamei, and S. Ohno, "Reconsideration of dielectric breakdown mechanism of gate dielectrics on basis of dominant carrier change model," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4386–4392, 2017, doi:10.1109/TED.2017.2747580.

- [2] H. Bentarzi, *Transport in Metal-Oxide-Semiconductor Structures: Mobile Ions Effects on the Oxide Properties*. Springer Science & Business Media, 2011, doi:10.1007/978-3-642-16304-3\_7.
- [3] F. Boige, D. Trémouilles, and F. Richardeau, "Physical origin of the gate current surge during short-circuit operation of sic mosfet," *IEEE Electron Device Lett.*, vol. 40, pp. 666–669, 2019, doi:10.1109/LED.2019.2896939.
- [4] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John Wiley & sons, 2006, doi:10.1002/0470068329.
- [5] G. Pananakakis, G. Ghibaudo, R. Kies, and C. Papadas, "Temperature dependence of the fowler–nordheim current in metal-oxide-degenerate semiconductor structures," *J. Appl. Phys.*, vol. 78, pp. 2635–2641, 1995, doi:10.1063/1.360124.
- [6] J. J. O'Dwyer, *The theory of electrical conduction and breakdown in solid dielectrics*. Clarendon Press, 1973.
- [7] M. Lenlinger and E. H. Snow, "Fowler-nordheim tunneling into thermally grown sio<sub>2</sub>," *J. Appl. Phys.*, vol. 40, pp. 278–283, 1969, doi:10.1063/1.1657043.
- [8] N. Son, W. Chen, O. Kordina, A. Konstantinov, B. Monemar, E. Janzén, D. Hofman, D. Volm, M. Drechsler, and B. Meyer, "Electron effective masses in 4h sic," *Appl. Phys. Lett.*, vol. 66, pp. 1074–1076, 1995, doi:10.1063/1.113576.
- [9] M. Sometani, D. Okamoto, S. Harada, H. Ishimori, S. Takasu, T. Hatakeyama, M. Takei, Y. Yonezawa, K. Fukuda, and H. Okumura, "Temperature-dependent analysis of conduction mechanism of leakage current in thermally grown oxide on 4h-sic," *Journal of Applied Physics*, vol. 117, no. 2, p. 024505, 2015, doi:10.1063/1.4905916.
- [10] R. Waters and B. V. Zeghbroeck, "Temperature-dependent tunneling through thermally grown sio<sub>2</sub> on n-type 4h- and 6h-sic," *Appl. Phys. Lett.*, vol. 76, p. 1039, 2000, doi:10.1063/1.125931.
- [11] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of sic mosfets: A technology for high-temperature environments," *IEEE Trans. Device Mater. Rel.*, vol. 10, pp. 418–426, 2010, doi:10.1109/TDMR.2010.2077295.
- [12] P. Fiorenza, A. Frazzetto, A. Guarnera, M. Saggio, and F. Roccaforte, "Fowler-nordheim tunneling at sio<sub>2</sub>/4h-sic interfaces in metal-oxide-semiconductor field effect transistors," *Appl. Phys. Lett.*, vol. 105, p. 142108, 2014, doi:10.1063/1.4898009.
- [13] D. J. Lichtenwalner, S. Sabri, E. V. Brunt, B. Hull, S. Ganguly, D. A. Gajewski, S. Allen, and J. W. Palmour, "Gate oxide reliability of sic mosfets and capacitors fabricated on 150mm wafers," in *Proceedings of the 12th European Conference on Silicon Carbide and Related Materials*, Birmingham, UK, 2–6 Sep 2018, doi:10.4028/www.scientific.net/MSF.963.745.
- [14] A. K. Agarwal, S. Seshadri, and L. B. Rowland, "Temperature dependence of fowler-nordheim current in 6h- and 4h-sic mos capacitors," *IEEE Electron Device Lett.*, vol. 18, pp. 592–594, 1997, doi:10.1109/55.644081.
- [15] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *J. Appl. Phys.*, vol. 67, pp. 2944–2954, 1990, doi:10.1063/1.345414.
- [16] R. H. Good and E. W. Müller, "Field emission," in *Electron-Emission Gas Discharges I/Elektronen-Emission Gasentladungen I*. Springer, 1956, p. 176, doi:10.1007/978-3-642-45844-6.
- [17] A. Hadjadj, G. Salace, and C. Petit, "Fowler–nordheim conduction in polysilicon (n+)–oxide–silicon (p) structures: Limit of the classical treatment in the barrier height determination," *J. Appl. Phys.*, vol. 89, pp. 7994–8001, 2001, doi:10.1063/1.1374479.
- [18] A. Hadjadj, O. Simonetti, T. Maurel, G. Salace, and C. Petit, "Si-sio<sub>2</sub> barrier height and its temperature dependence in metal-oxide-semiconductor structures with ultrathin gate oxide," *Appl. Phys. Lett.*, vol. 80, pp. 3334–3336, 2002, doi:10.1063/1.1476709.
- [19] M. Le-Huu, H. Schmitt, S. Noll, M. Grieb, F. Schrey, A. J. Bauer, L. Frey, and H. Ryssel, "Investigation of the reliability of 4h-sic mos devices for high temperature applications," *Microelectron. Reliab.*, vol. 51, pp. 1345–1350, 2011, doi:10.1016/j.microrel.2011.03.015.
- [20] T. Kimoto and J. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. John Wiley & Sons, 2014, doi:10.1002/9781118313534.
- [21] V. Afanas'ev, M. Bassler, G. Pensl, M. Schulz, and E. V. Kamienski, "Band offsets and electronic structure of sic/sio<sub>2</sub> interfaces," *J. Appl. Phys.*, vol. 79, pp. 3108–3114, 1996, doi:10.1063/1.361254.
- [22] P. Friedrichs, E. Burte, and R. Schörner, "Dielectric strength of thermal oxides on 6h-sic and 4h-sic," *Appl. Phys. Lett.*, vol. 65, pp. 1665–1667, 1994, doi:10.1063/1.112904.
- [23] R. Singh and A. R. Hefner, "Reliability of sic mos devices," *Solid-State Electron.*, vol. 48, pp. 1717–1720, 2004, doi:10.1016/j.sse.2004.05.005.
- [24] R. Singh, "Reliability and performance limitations in sic power devices," *Microelectron. Reliab.*, vol. 46, pp. 713–730, 2006, doi:10.1016/j.microrel.2005.10.013.
- [25] W. Weicheng, X. Zhong, and K. Sheng, "High temperature stability and the performance degradation of sic mosfets," *IEEE Trans. on Power Electron.*, vol. 29, pp. 2329–2337, 2014, doi:10.1109/TPEL.2013.2283509.
- [26] K. Fukuda, S. Suzuki, T. Tanaka, and K. Arai, "Reduction of interface-state density in 4 h-sic n-type metal-oxide-semiconductor structures using high-temperature hydrogen annealing," *Appl. Phys. Lett.*, vol. 76, pp. 1585–1587, 2000, doi:10.1063/1.126103.
- [27] T. Kobayashi, J. Suda, and T. Kimoto, "Reduction of interface state density in sic (0001) mos structures by post-oxidation annealing at high temperature," *AIP Advances*, vol. 7, p. 045008, 2017, doi:10.1063/1.4980024.
- [28] A. Fayyaz, L. Yang, and A. Castellazzi, "Transient robustness testing of silicon carbide (sic) power mosfets," in *15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, 3–5 Sep 2013, pp. 1–10, doi:10.1109/EPE.2013.6634645.

- [29] C. Chen, D. Labrousse, S. Lefebvre, M. Petit, C. Buttay, and H. Morel, "Study of short-circuit robustness of sic mosfets, analysis of the failure modes and comparison with bjts," *Microelectron. Reliab.*, vol. 55, pp. 1708–1713, 2015, doi:10.1016/j.microrel.2015.06.097.
- [30] Cree, *C2M0080120D Silicon Carbide Power Mosfet Datasheet, Rev. C*, Durham, NC, USA, Oct. 2015.
- [31] O. Aviño-Salvado, H. Morel, C. Buttay, D. Labrousse, and S. Lefebvre, "Threshold voltage instability in sic mosfets as a consequence of current conduction in their body diode," *Microelectronics Reliability*, vol. 88, pp. 636–640, 2018, doi:10.1016/j.microrel.2018.06.033.
- [32] C. Hu, *Modern semiconductor devices for integrated circuits*. Prentice Hall Upper Saddle River, NJ, 2010, vol. 2, doi:10.3403/BSIEC60748.
- [33] N. Saks, S. Mani, and A. Agarwal, "Interface trap profile near the band edges at the 4h-sic/sio<sub>2</sub> interface," *Appl. Phys. Lett.*, vol. 76, no. 16, pp. 2250–2252, 2000, doi:10.1063/1.126311.
- [34] R. Ouaida, M. Berthou, J. León, X. Perpiñà, S. Oge, P. Brosselard, and C. Joubert, "Gate oxide degradation of sic mosfet in switching conditions," *Electron Device Lett.*, vol. 35, pp. 1284–1286, 2014, doi:10.1109/LED.2014.2361674.
- [35] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, and Y. Yokotsuji, *High performance SiC trench devices with ultra-low ron*, Washington, USA, 5-7 Dec 2011, doi:10.1109/IEDM.2011.6131619.
- [36] R. Kumar Chanana, "Determination of hole effective mass in sio<sub>2</sub> and sic conduction band offset using fowler-nordheim tunneling characteristics across metal-oxide-semiconductor structures after applying oxide field corrections," *Journal of Applied Physics*, vol. 109, no. 10, p. 104508, 2011, doi:10.1063/1.3587185.
- [37] P. Fiorenza, G. Greco, F. Giannazzo, R. Lo Nigro, and F. Roccaforte, "Poole-frenkel emission in epitaxial nickel oxide on algan/gan heterostructures," *Applied Physics Letters*, vol. 101, no. 17, p. 172901, 2012, doi:10.1063/1.4761961.
- [38] J. Berens, G. Pobegen, G. Rescher, T. Aichinger, and T. Grasser, "NH<sub>3</sub> and no+nh<sub>3</sub> annealing of 4h-sic trench mosfets: Device performance and reliability," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4692–4697, 2019, doi:10.1109/TED.2019.2941723.
- [39] P. Samanta and K. C. Mandal, "Leakage current conduction, hole injection, and time-dependent dielectric breakdown of n-4h-sic mos capacitors during positive bias temperature stress," *J. Appl. Phys.*, vol. 121, no. 3, p. 034501, 2017, doi:10.1063/1.4973674.
- [40] P. Fiorenza, M. Vivona, F. Iucolano, A. Severino, S. Lorenti, G. Nicotra, C. Bongiorno, F. Giannazzo, and F. Roccaforte, "Temperature-dependent fowler-nordheim electron barrier height in sio<sub>2</sub>/4h-sic mos capacitors," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 38–42, 2018, doi:10.1016/j.mssp.2017.11.024.