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High-efficiency cooling system for highly integrated power electronics for hybrid propulsion aircraft

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Abstract— A study of high-performance power electronics and their associated high efficiency cooling system is proposed in this work. The purpose of the research is to find, design, study and optimize high-efficiency power electronics cooling system for a hybrid propulsion aircraft. The purpose is to find the most performing and efficient cooling system to allow power electronic converters to operate with the highest performances possible. After a study focused on the most suitable solutions, a passive capillary pumped system was retained because of its performances and energetic efficiency. Here, a study of this particular system is presented. The Capillary Pumped Loop for Integrated Power (CPLIP) or CPLTA (Capillary Pumped Loop for Terrestrial Applications) is introduced: numerical and experimental results are proposed to show the performances of this loop. It will be also shown that the loop is able to ensure the temperature requirements for power modules. After an introduction on this kind of cooling system and its working principles, the loop behavior will be experimentally studied while a finite volume solver will be used to obtain 3D temperature map of power converter modules. Other than the capability to ensure the temperature controllability, it will be shown how this loop is able to ensure and go beyond the required power coefficient to allow these systems to fly.

Keywords—Power electronics, cooling, temperature, capillary pumped loop, hybrid aircraft

I. INTRODUCTION

The subject of the present research is part of the European project Cleansky2. It is managed by HASTECS consortium (Hybrid Aircraft Academic reSearch on Thermal and Electrical Components and Systems). Five different teams work on the project, each one with a different task. Power electronics and power electronics cooling teams (WP2 and WP4, respectively) collaborate to research, design and optimize highly integrated power electronic systems and their associated high-efficiency cooling system to be used for the hybrid propulsion aircraft of 2035. For the research, two different targets have been imposed

to allow these systems to fly. The first objective, referred to the year 2025, is to design and optimize power electronics and their associated cooling system with the purpose to obtain an overall power coefficient of $15 \text{ kW} \cdot \text{kg}^{-1}$. A power coefficient of $25 \text{ kW} \cdot \text{kg}^{-1}$ has to be reached for 2035.

Power electronics, multilevel converters are more and more used for high-power medium-voltage applications. Actually, this is the best option to reduce converters' weight while maintaining a high efficiency. However, adapted control strategy and semiconductors should be used with, to reduce power losses due to high switching frequencies.

The increasing power and the miniaturization of electronic components make the classical cooling solutions inadequate to evacuate the thermal load generated by chips. It is thus necessary to find and use more efficient and easy-to-integrate solutions. During the latest twenty years, many researchers worked on the issue: different technologies have been continuously compared and studied to find the most performing one, as reported by Agostini et al. in 2007 [1]. Energetic efficiency and thermal performances, unfortunately, do not always go in the same direction. In fact, most of the best nowadays performing technologies are able to ensure the adequate cooling with high heat transfer coefficients. On the contrary, these solutions sometimes require very high pumping power (e.g. mini or microchannels, porous media and metal foams [1]). The higher the pumping power, the lower the power coefficient. In general, the choice of a cooling technology depends on efficiency and performance requirements. New kinds of technologies have been used since the latest thirty years in space applications [2], e.g. satellite data transmission equipment cooling: heat pipes, Capillary Pumped Loop (CPL) and Loop Heat Pipes (LHP). The main advantages of these systems are passivity, adaptability and efficiency [3]. Since a few years they have been also used for power electronics cooling in terrestrial applications [4], e.g.

railway [5-7] and automotive fields. One of the main issues, related to the use of capillary pumped technologies in terrestrial applications, is their sensitivity to the gravity field. To avoid problems related to LHPs or CPLs [8], in particular during transient stages, a new kind of loop was developed in 2004 by Euro Heat Pipes™. The Capillary Pumped Loop for Terrestrial Applications (CPLTA) or CPLIP (Capillary Pumped Loop for Integrated Power), as it is also called (see Fig. 9), allows a temperature range controllability, like a classical CPL, without all the instabilities.

High heat flux removing capability is undeniable for this kind of loop! Since 2012, it is experimented and used in a metropolitan cycle in the RATP line in Paris for IGBTs cooling with a theoretical thermal evacuation capability up to $40 \text{ W} \cdot \text{cm}^{-2}$, as reported by Dupont et al. [5]. Ayel et al. [8] and Accorinti et al. [9] have deeply explained the ability to maintain a constant operating temperature on the evaporator walls, where electronics power modules are installed, for any cold source temperature variation and for power cycle with large amplitude heat load steps [10]. In particular, Accorinti et al. [9] showed, changing cold source temperature from 5 to 40°C , at constant applied thermal power, that the evaporator wall temperature change was negligible. Moreover, it was demonstrated, parametrizing the reservoir temperature, at constant cold source temperature and heat power, that it is possible to control the evaporator wall temperature and so to fix the junction temperature.

After an introduction on which are the most suitable strategies to apply to power electronics to maximize the power coefficient ($\text{kW} \cdot \text{kg}^{-1}$), in this paper, power electronics technologies are introduced to explain their influence on power coefficient and which are the strategies to control it. Particular attention will be paid to the cooling system. Its working principle and the main thermal characteristics will be presented. It will be also shown how it is able to satisfy the efficiency and temperature requirements in this particular application field. Analytic, experimental and numerical methods are used to demonstrate the capability of this kind of cooling system to keep temperature controlled, for the presented high efficiency and performing electronic components, in presence of high heat flux densities.

II. TECHNOLOGIES

A. Power electronics

Converter losses have a great impact on cooling system design and its transient capacity influences converter-sizing point. It is so necessary to maintain them as low as possible.

To get an idea of the value of the specific power ($\text{kW} \cdot \text{kg}^{-1}$) obtained using a simple solution, a 3-level NPC inverter with a regular PWM was sized for the maximal power point. A cooling system power coefficient of $0.34 \text{ kW} \cdot \text{kg}^{-1}$ and 6th generation semiconductor silicon components were considered. For the latter case, the converter weight repartition is shown in Fig. 1. In this particular case, the specific power coefficient of the inverter and its adjoined cooling system is equal to $9.77 \text{ kW} \cdot \text{kg}^{-1}$, which is small when compared to the 2025 target of $15 \text{ kW} \cdot \text{kg}^{-1}$. Therefore, from this example, it can be noticed that the main factor to increase power density is to decrease the cooling system mass (heat exchanger in Fig. 1): by reducing the power losses

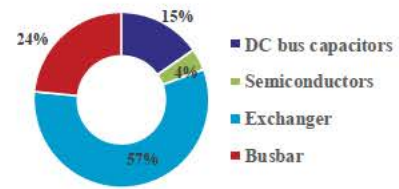


Fig. 1. 3-level PWM NPC weight distribution (using 6th Gen. 1700V IGBT).

sses and/or optimizing the cooling system itself. As far as power electronics is concerned, the power losses could be reduced by playing on three main areas (see Fig. 2).

1) Topology choice

The first option to reduce power losses concerns the use of small voltage rating components, by using multilevel topologies to avoid the direct series association. The selected topologies are 3-level topologies such as NPC and FC [11]. The FC topology has an additional capacitor but, unlike NPC, switching frequency is divided by two. 5-level topologies were considered and studied, but the used voltage level does not require more than 3-level topologies in order to fully use the installed silicon of the IGBT modules.

2) Control strategy

The second option to reduce power losses is related to control or modulation strategy (see Fig. 3). This may reduce the switching losses if a discontinuous pulse width modulation is used instead of a sine PWM, for example. Here, only the sine and discontinuous PWM strategies results will be presented.

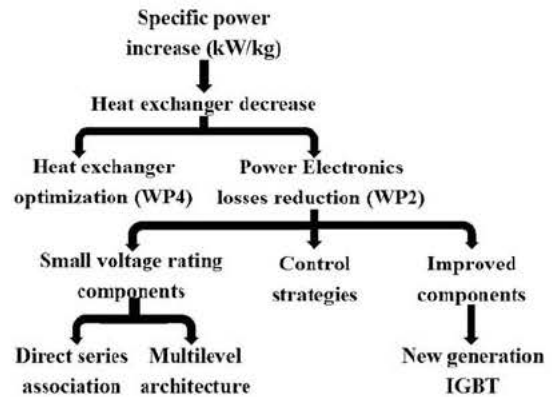


Fig. 2. Specific power increasing study line.

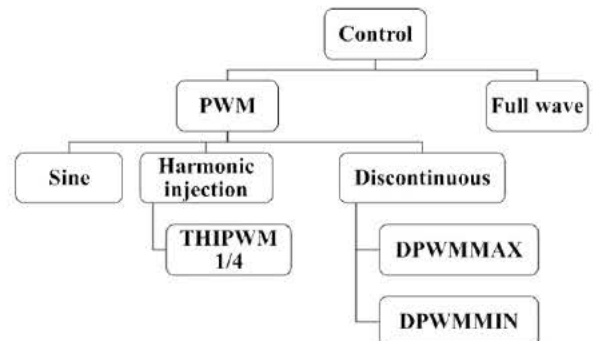


Fig. 3. Analyzed control strategies.

2.1) PWM

Sinusoidal PWM is the most used method: a high-frequency triangular carrier wave is compared with a sinusoidal reference of desired frequency (see Fig. 4). So, the intersection of both waves defines the switching or commutation instants. For this modulation, the harmonics are around the switching frequency.

2.2) Discontinuous PWM

Discontinuous PWM method is an effective strategy to reduce switching losses. The easiest approach for discontinuous modulation of a multilevel inverter is to simply lock particular phase legs to the upper or lower voltage rails for fractions of the fundamental cycle [12]. To do so, a signal is added to the sinusoidal reference and it is compared to the triangular carrier, as in Fig. 5, in which the switching cell does not switch for a third of the modulation period.

3) Used semiconductors and power losses model

The use of new generation IGBTs, better performing than old generation ones, is the third solution to reduce power losses. These new silicon components have new compact and light-weight package with 50% reduction of internal thermal resistance and 15% reduction of total losses in inverter operation as shown in Fig. 6 [13, 14].

Concerning the power losses model, the current and voltage characteristics of a transistor during a switching period are represented in Fig. 7. There are two types of power losses: switching and conduction losses. Switching losses for the IGBT are represented by the turn-on and off energies (E_{on} , E_{off}) as second-order polynomial as a function of the current with three parameters A, B and C (given by the manufacturer), as in (1):

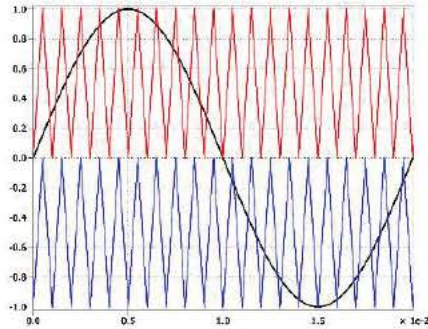


Fig. 4. PWM triangular carrier and sine reference.

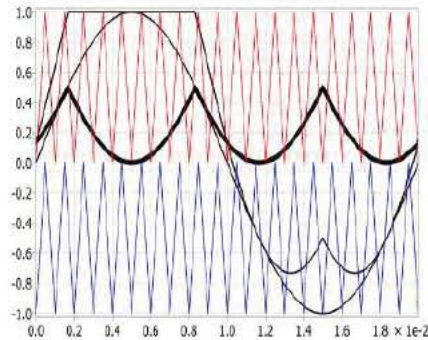


Fig. 5. DPWMMAX triangular carrier and sine reference.

$$E_{V_{def}}(I) = E_{on} + E_{off} = (A + B \times I + C \times I^2) \quad (1)$$

Using the integral of $E_{V_{def}}$, for a modulation period, the switching power losses, P_{sw} , can be computed as in (2):

$$P_{sw} = \frac{1}{T_{mod}} \frac{1}{T_{sw}} \int_{t_1}^{t_2} \frac{v_{sw}}{v_{def}} E_{V_{def}}(I) dt \quad (2)$$

With T_{sw} the switching period, T_{mod} the modulation period and v_{sw} the switching voltage. v_{def} is determined from the datasheet ($v_{def} = \frac{v_{max}}{2}$). A more detailed description of the losses calculation method is available in [15]. Otherwise, conduction losses are calculated using the following model, see (3) and (4):

$$P_{condIGBT} = \frac{1}{T_{mod}} \int V_{ce}(t) \times I_c(t) dt \quad (3)$$

$$P_{condIGBT} = V_{ce0} \cdot I_{avg} + R_{ce} \cdot I_{rms}^2 \quad (4)$$

With V_{ce0} and R_{ce} the conduction parameters given by the manufacturer (see Table I). Similar equations are used for the diode. The switching and conduction parameters, reported in Table I for the 1700V 7th generation Mitsubishi's component, are selected from the datasheet and integrated into the developed simulation tool. In this particular architecture, a single power switch contains a transistor with an antiparallel diode that ensures a path for the reverse current.

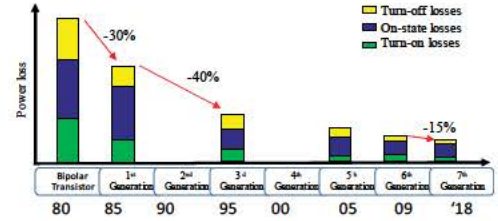


Fig. 6. IGBT's power losses evolution [14].

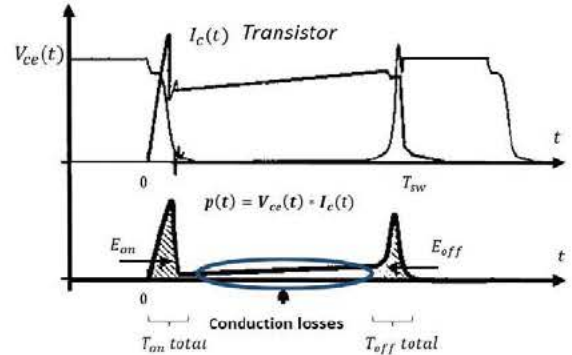


Fig. 7. IGBT current and voltage waveforms during switching.

TABLE I. Switching and conduction IGBT parameters.

	A	B	C	V_{ce0} (V)	R_{ce} (mΩ)
On	9.5E-3	8.52E-5	1.28E-7	1.13	1.36E-3
Off	2.21E-2	1.36E-4	8.35E-8		

The thermal model circuit will include two thermal resistors: $R_{th_{jc}}$ and $R_{th_{ch}}$ (see Fig. 8), in which the thermal flow is caused by the losses of each component. The temperatures of the different points in the switch package can be determined using (5), (6) and (7):

$$T_{Transistor} = P_{losses} R_{th_{jc}T} + T_{case} \quad (5)$$

$$T_{Diode} = P_{losses_{Diode}} R_{th_{jc}D} + T_{case} \quad (6)$$

$$T_{case} = (P_{losses} + P_{losses_{Diode}})(R_{th_{ch}} + R_{th_{ha}}) + T_{ambient} \quad (7)$$

Where $R_{th_{jc}}$ is the junction to case thermal resistance, for transistor and diode respectively (T and D); $R_{th_{ch}}$ is the case to heatsink thermal resistance and $R_{th_{ha}}$ is the heatsink to ambient thermal resistance (all resistances are expressed in $K \cdot W^{-1}$).

The case of the chips package is directly connected to the ambient, corresponding to the imposed reservoir temperature (see sec. IV) in this particular study case. So the heatsink to ambient thermal resistance ($R_{th_{ha}}$) is forced to zero. The assembly is cooled down by the CPLIP's evaporator, as it will be better explained in the following, whose specifications are modeled using the experimental evaporator-to-reservoir thermal conductance [9], in order to fix the case temperature to the ambient ($70^\circ C$ in our example).

B. CPLIP working and theoretical principles

Theoretical thermodynamic cycle and operating principle of the CPLIP have been deeply explained in previous works [8-10,16,17]. High simplicity characterizes the Capillary Pumped Loop for Integrated Power. The primary circuit is composed by an evaporator (or more in parallel as in the case of this study), a vapor line, a condenser (oversized to ensure the necessary subcooling), a liquid line and a reservoir (see Fig. 9). Here, a quick and simplified explanation is reported to focus the attention on the thermodynamic states of interest: evaporator wall temperature (where power electronics modules are installed), secondary side temperatures (where heat is definitively evacuated) and reservoir temperature (also called ambient temperature, see Fig. 9), used to fix the operating pressure and temperature level of the whole system.

In the diagram reported in Fig. 10, with reference to the loop scheme of Fig. 9, the theoretical thermodynamic cycle is reported.

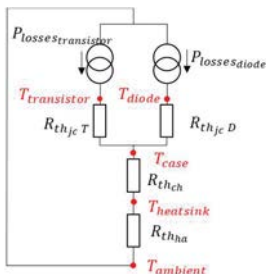


Fig. 8. Equivalent thermal model of an IGBT component with antiparallel diode [15].

Starting from point V , corresponding to the saturation evaporating conditions in the porous wick, the vapor flows in the evaporator grooves where, subject to viscous pressure losses, it is superheated (point V_i). In the vapor lines, the vapor is slightly cooled (heat losses to the ambient) until the inlet of the condenser: condition V_o . In the condenser, vapor is cooled until saturation state at condensation front C . Then, the liquid is subcooled until point l_i (the point C corresponds to the condensation front). The slight pressure increase, between the states C and l_i , is due to a difference of height, so to gravity force, between the condenser inlet and outlet respectively (almost 10 cm in this case). From the outlet of the condenser, subcooled liquid flows through the liquid line (supposed to be well insulated) to the reservoir inlet (point l_o). In the liquid line, the liquid is obviously subjected to viscous losses and gravity pressure drop due to the difference of height between the condenser outlet and the reservoir inlet. The liquid leaves the reservoir, slightly heated, in the condition RE , corresponding to the liquid condition in the lower part of the reservoir. Flowing through the reservoir-evaporator tube, the liquid enters the evaporator (condition E_i). The liquid that flows in the porous wick is subjected to a pressure drop. Here it is heated, until condition E_o is reached: evaporation temperature in the wick. In the evaporator, capillary forces take place and compensate for all pressure drops in the loop between E_o and V .

Calculating the total amount of pressure drop in the loop, corresponding to the pressure difference between the states E_o and V (see Fig. 10), it is possible to calculate the vaporization temperature T_V , corresponding to the saturation pressure P_V .

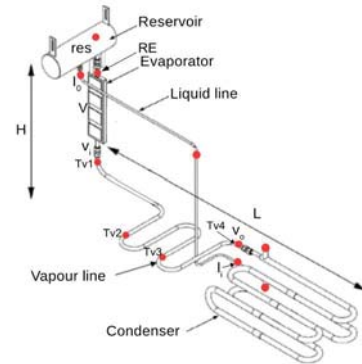


Fig. 9. CPLIP concept scheme [8, 10, 17].

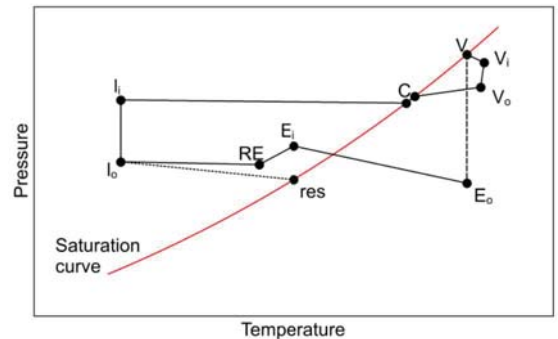


Fig. 10. Theoretical CPLIP thermodynamic cycle [8,12].

The pressure difference that the capillary wick is able to provide, allows the fluid to flow in the loop and is equivalent to the accumulated pressure drop in the whole loop (until the capillary limit ΔP_c):

$$\Delta P_c = \Sigma \Delta P_{tot} = P_V - P_{E0} \quad (8)$$

A more accurate explanation of working principle and the method to calculate the value of the evaporation temperature in the wick, with good approximation in steady state conditions, is reported in [9].

III. PROBLEM SPECIFICATIONS

From a thermal point of view, the cooling system has to be able to limit the temperature of electronic components and to ensure a constant operating temperature during the entire mission of the aircraft. Otherwise, climb and descent stages can represent a detrimental condition for the power electronics lifetime. In fact, ground and flight altitude temperature conditions are much different. A temperature difference of about 40 K exists between these two conditions. The cooling system has to be also able to ensure the highest thermal performances possible, in terms of heat transfer coefficient, and the adequate temperature on the base of the power modules. To respect the targets of 2025 and 2035, the system has to be characterized by the lowest mass possible to increase the power to mass ratio (power coefficient) and to respect the energy-efficiency-condition: the system has to be able to absorb the lowest amount of energy to operate. Moreover, from a thermodynamic point of view, the lowest the irreversibility, due to the presence of mobile parts and valves in the circuit, the highest the thermodynamic efficiency.

As a function of the chosen electronic topology, a heat power up to 18 kW has to be evacuated with the lowest encumber possible. In this study, it will be considered that the power electronics and its adjoined cooling system are installed in the nacelle.

IV. COOLING SYSTEM DESIGN AND OPTIMISATION

A. Preliminary analysis

The choice of the design point is a critical issue. This influences the mass of the cooling system and so the power coefficient. An analysis based on the amount of energy to be evacuated from electronic components during the entire mission profile is thus necessary. Observing the electronic losses mission profile as a function of time (Fig. 11 reports as an example the thermal losses for an NPC-DPWMMAX configuration; there, for confidentiality issues the thermal losses are reported as the ratio Q/Q_{max} , where Q_{max} is higher than 15 kW), five different stages can be identified. Each stage of the mission profile is related to a different behavior of electronic components and so to a different amount of thermal energy to be evacuated: taxi out (I), take-off and climb (II), cruise (III), descent and landing (IV), taxi in (V). During stage I, IV and V, the quantity of thermal energy to be evacuated is lower than the energy to be evacuated during the take-off or cruise stages (II and III respectively). The design point choice is so impacted by these two flight phases. In particular, at the beginning of stage II, a power peak (red circle in Fig. 11), which is very limited in time (abo-

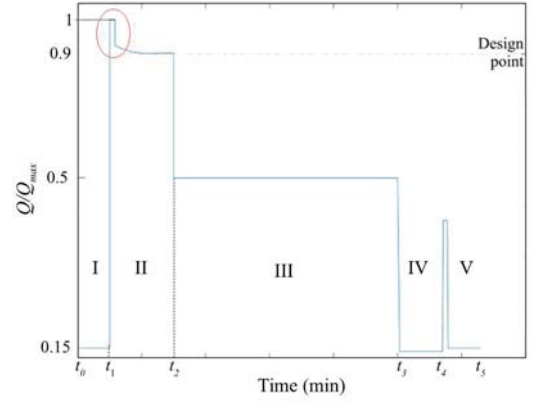


Fig. 11. Example of total thermal losses as a function of time (NPC-DPWMMAX configuration).

ut 1.5 min) is noticeable. During the cruise stage, the thermal losses are almost one-half of the power peak value. A cooling system design based on the power peak value can lead to a large over-sizing of the cooling system, while an under-sizing is evident if the cruise stage is chosen to fix the design point. In this last case a coupling with a different technology should be considered to damp the lack of not treated energy but reducing the power coefficient. The point corresponding to thermal losses at the end of the take-off stage is chosen as trade-off for the design point. Loop thermal and hydraulic inertia will be used to damp the thermal power peak at the beginning of stage II. In table II, a synthesis of the amounts of energy is reported for the take-off (II) and cruise (III), according to the electronic topology.

There, the ratios of energy to be evacuated during those stages and the quantity of neglected energy are also reported. Moreover, it can be observed that the energy evacuated during stage II is between 44 and 45% of that of stage III, whatever the electronic topology. Moreover, one can observe that the neglected amount of energy, for the specified design points, is lower than 3% of the energy to be evacuated during stage II.

In the following, it will be experimentally shown that the thermal and hydraulic inertia of the loop can be used to damp the energy lack ($E_{neglected}$).

B. Loop design

During the optimization process of the CPLIP, particular attention was paid to the condenser: the heaviest component in the whole cooling system. In this particular application it is assumed that the condenser is installed in the nacelle, where a secondary air flow (external air) is always available when power converters operate.

TABLE II. Thermal energy ratios during take-off and cruise.

Power electronics topology	E_{II} (MJ)	E_{III} (MJ)	E_{II}/E_{III}	$E_{neglected}$
FC_DPWMMAX	16.20	36.12	44.85%	2.23%
FC_PWM	19.42	44.10	44.03%	1.99%
NPC_DPWMMAX	16.86	38.22	44.11%	1.56%
NPC_PWM	18.75	42.00	44.63%	1.86%

Titanium was chosen as material for loop components and aluminum for condenser fins. The secondary side air velocity was considered equal to the aircraft velocity during the taxi out-and-in stages (10 m/s) at 33°C (on the ground according to the 98% of the airports in the world). Methanol was considered as working fluid [8-10,16,17]. In Fig. 12 a simplified schematic of a three parallel heads CPLIP is reported. No thermal diffusers are considered. Starting from the design point, the necessary coolant mass flow rate, \dot{m}_{meth} , is calculated by considering latent and sensible heats; referring to Fig. 12:

$$\dot{m}_{meth} = \frac{\sum_n Q_{ext,n}}{h_{l,v} + c_{p,l}(T_V - T_{RE})} \quad (9)$$

Where, in (9), $Q_{ext,n}$ is the electronic loss to the n -th evaporator (design point), $h_{l,v}$ the latent heat of vaporization and $c_{p,l}$ the specific heat, while T_V and T_{RE} are the vaporization and reservoir temperatures, respectively.

With reference to the NPC-DPWMMAX configuration (in bold in Table II), in the following, the dimensions of the components of the loop are reported to give to reader an idea of the cooling system overall dimensions. To reduce the mass of the transport lines, their internal diameters were calculated on the basis of an imposed velocity of 50 and 2 m/s in vapor and liquid lines respectively. So, the 0.2-meter-long titanium vapor and liquid lines are characterized by an internal diameter of 15 mm and 3 mm respectively and a wall thickness of 0.6 mm. A continued smooth finned condenser (overall dimensions: $0.8 \times 0.05 \times 0.35$ m³), with internal tubes' diameter of 8 mm, was chosen for any case. To reduce the pressure drop in this component, a two-ranks (thirty tubes per rank), parallel fed configuration was chosen. The 0.1-millimeters-thick rectangular fins are made of aluminum and are spaced of 2 mm the one from the other. An overall thermal conductance of $760 \text{ W} \cdot \text{K}^{-1}$ characterizes the condenser in this particular case.

In Fig. 13, an example of power modules/evaporator assembly is reported. The evaporator dimensions are related to power modules dimensions: evaporator frontal surface area is equal to the total surface of modules to be cooled. Following the latter dimensions (*Mitsubishi 7th generation IGBT modules NC-Type*), the evaporator is characterized by a height (\vec{g} direction) of 26 cm, a width of 6.2 cm and a thickness of 1.8 cm, as in [8]. A nickel porous wick, with a porosity of 73%, an average pore diameter of $6.3 \mu\text{m}$ and a thickness of 14 mm, is contained in the evaporator case as in [8, 9]. Power modules are installed on the one millimeter-thick-nickel evaporator walls.

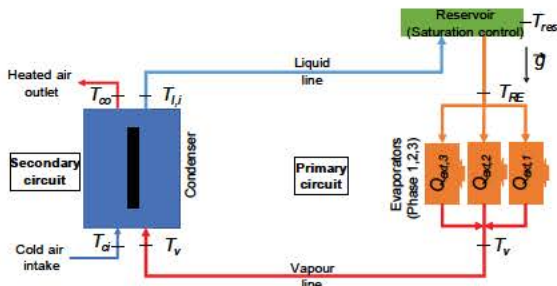


Fig. 12. Three parallel heads CPLIP configuration.

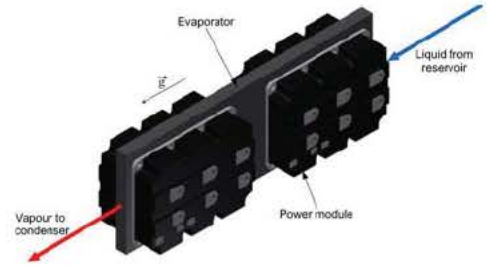


Fig. 13. Module/evaporator assembly.

Finally, the reservoir total volume, assumed to be rectangular, is calculated to compensate for the volume of fluid contained in the vapor line and the condenser during operations. A two-millimeters-thick wall was considered, for any case, to obtain its mass and encumber. Further studies have to be done to decrease the reservoir wall thickness by ensuring the adequate mechanical resistance to reservoir internal pressure.

C. Results

The results of the optimization process are reported in Table III for any electronic topology. The highest power coefficient (about $19 \text{ kW} \cdot \text{kg}^{-1}$) was reached for the NPC-DPWMMAX configuration, characterized by the lowest mass. This value is higher than that required for the target 2025 ($15 \text{ kW} \cdot \text{kg}^{-1}$), but more researches have to be done to optimize the cooling system to reach the power coefficient requirements of 2035.

In the case of this application, the ability of the cooling system to evacuate the highest heat power with the lower cooling system mass is a necessary but not sufficient condition. It has to be also verified that the system is able to ensure the component temperature requirements. In particular, for power modules in use (*Mitsubishi 7th generation IGBT modules – NC-Type*), the junction temperature is limited to 150°C. The temperature distribution on the power module can be obtained by executing 3D-conduction simulations using the finite volume solver of StarCCM+™. High frequency switching of electronic components is largely smoothed by the high time constant of thermal system. So, steady-state condition was used in the model. Following the scheme reported in Fig. 14, the thermal power evacuated by the IGBT or diode was applied on the junction, following the case. The experimentally obtained thermal conductance ($G_{ev,res}$), reported in [9], was used as convection boundary condition on the opposite side with a reference (ambient) temperature at the reservoir, $T_{res}=70^\circ\text{C}$. As indicated in the Mitsubishi's datasheet for this particular module, the materials indicated in Fig. 14 were used. As it will be seen in the

TABLE III. Optimization results for each electronic topology: cooling system mass and thermal power coefficient.

Topology	Cooling system mass (kg)	Thermal power coefficient ($\text{kW} \cdot \text{kg}^{-1}$)
FC_DPWMMAX	10.5	1.29
FC_PWM	14.0	1.16
NPC_DPWMMAX	11.1	1.26
NPC_PWM	12.3	1.27

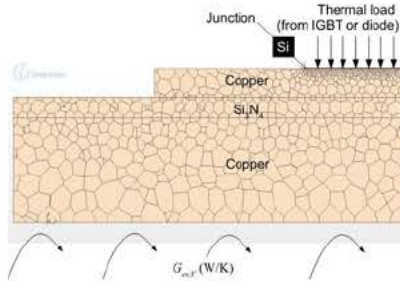


Fig. 14. Model boundary conditions section scheme.

following, the particular assembly of the module allows, because of the presence of the resin layer (Si_3N_4), a spreading of the heat evacuated by components. No thermal diffusers are needed in this case. In Fig. 15 and 18, numerical results are reported for the two worst conditions: only diodes, or only IGBTs, operate. In the first case (Fig. 15), due to high component losses on a small surface, the heat flux density is higher than that of the second case (Fig. 16). The worst condition, in which only diodes dissipate 155 W each, the heat flux density is obviously the highest one: a heat flux density of about $242 \text{ W}\cdot\text{cm}^{-2}$ is applied on each diode in this case. It can be observed that, despite this very high value, the maximum junction temperature is about 127°C : lower than the maximum admissible temperature value. In the second case (Fig. 16), because of the lowest heat flux density applied on the IGBTs (about $92 \text{ W}\cdot\text{cm}^{-2}$), lower temperature values are registered. In both cases the minimum temperature is obviously fixed by the saturation condition in the reservoir ($T_{\text{res}} = 70^\circ\text{C}$ in these examples). Observing both Fig. 15 and 18, in which the junction-side view is reported, hot spots are noticeable in correspondence of the junction both for IGBTs and diodes. However, the maximum temperature value does not cross-over the admissible temperature value (150°C). Despite

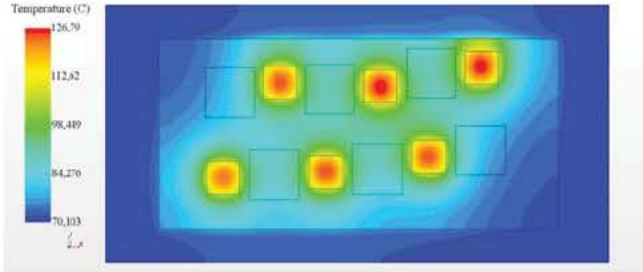


Fig. 15. Temperature map: Diode losses 155 W, each; IGBT losses 0 W each ($T_{\text{res}} = 70^\circ\text{C}$).

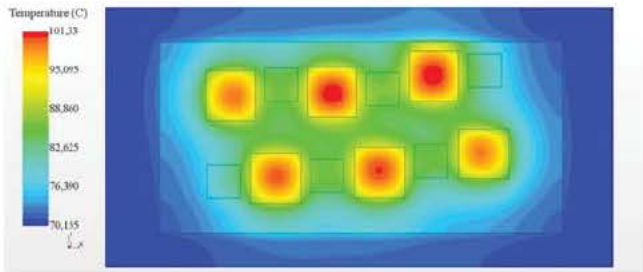


Fig. 16. Temperature map: Diode losses 13 W, each; IGBT losses 133 W each ($T_{\text{res}} = 70^\circ\text{C}$).

the very high heat flux densities dissipated by components, the spreader behavior of the module allows a more uniform temperature field distribution in correspondence of the module base (interface between the module and the evaporator). No hot-spot are so noticeable there and so, an equivalent heat flux density of about $12.2 \text{ W}\cdot\text{cm}^{-2}$ and $11.6 \text{ W}\cdot\text{cm}^{-2}$ is dissipated by each module in the first and in the second case respectively.

Fig. 17 depicts the experimental results for a one-phase thermal losses mission profile. The same experimental facility as in Ayel et al. [8] and Accorinti et al. [9] was used. There, the characteristics of the experimental apparatus are deeply explained. The loop used for the tests has a maximum heat evacuation capability higher than 5 kW with a single evaporator. This allowed to test the losses of one electrical phase, $Q_{\text{ext},n}$ (even in this case for confidentiality issues only the ratio between the thermal power to be evacuated and the maximal, one-electrical phase thermal power, $Q_{\text{ext},n}$, is reported). The hypothesis about the use of the loop thermal inertia during severe transient phases (take-off stage) can be so verified. Some differences could exist between the experimental behavior, here presented, and the real one. They should be especially due to a length difference of the transport lines and/or a different nature of condensers.

With reference to Fig. 17, as the power is applied to the evaporator (about 15% of $Q_{\text{ext},n}$, at time $t=0$) during taxi-out stage, the loop starts to operate (before the power peak of stage II).

The presence of temperature overshoot and the start-up behavior has been deeply explained in [17]. As the sudden and violent thermal power peak is applied to the evaporator (100% of $Q_{\text{ext},n}$ at the beginning of the take-off stage, II), the evaporator wall temperature (indicated as “base” temperatures in the curves of Fig. 17) increases. Because of the thermal inertia of the evaporator, the temperature peak is reached only at the end of the power peak. Despite the heat power applied to the evaporator decreases, the temperature continues to slightly increase, but with a lower slope. This phenomenon could be due to assessment phenomena in the reservoir due to the violent increase of thermal power applied to the evaporator (from about 15% to 100% of $Q_{\text{ext},n}$). When reservoir conditions are stabilized, one more time, the evaporator temperature decreases following the same shape

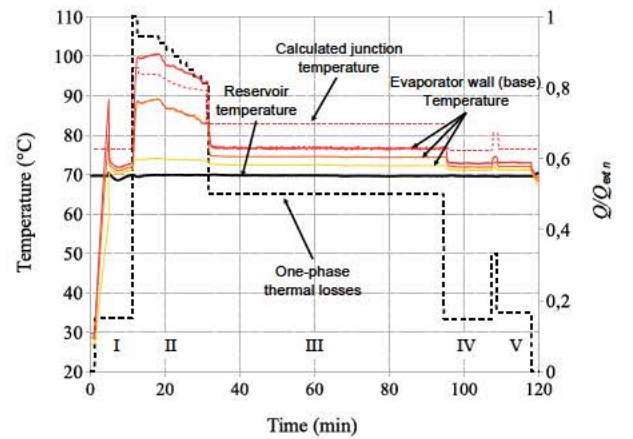


Fig. 17. Diagram resulting from an experimental test on a mission profile of a single-phase alimanted power converter.

of the thermal-power-load until cruise stage (III) begins. Here, all temperature values are stabilized. The loop operates in steady-state conditions. During this stage, because of a pressure difference between the evaporator inlet and outlet [17], a temperature difference in correspondence of the evaporator wall, and so in correspondence of the electronic modules base can be observed (red, orange and yellow curves). On the same diagram (Fig. 17), the value of the junction temperature, obtained by the numerical model described in sec. II, has been superimposed (red dotted line). The electronic numerical model uses the evaporator conductance curves [9]. The model tends to slightly overestimate the temperature values. This could be due to a “shift” between the wall and wick temperature. Otherwise, during the cruise stage (steady-state) the junction temperature prediction agrees with a difference lower than 10%. It can be also noticed that the temperature values are much lower than the admissible value, even during the harsh transient stage.

V. CONCLUSION

In this work, a high efficient and high performing cooling system for power electronic modules, for hybrid propulsion aircraft, has been presented with the purpose to find a solution to cool them in the most efficient way and to allow them to operate as close as possible to their limit by not caring about thermal issues. The problem to solve is not only related to thermal power to evacuate (up to 18 kW) and the high heat flux densities, but also to system mass and encumber. In fact, very high specific power values have to be reached to allow this system to be used in aeronautical field. After a discussion on the strategies to reduce power electronics thermal losses, the associated cooling system has been introduced with a quick explanation of its theoretical and working principle. A preliminary analysis was presented to explain how its design point was chosen. A three-parallel-evaporator capillary pumped loop was chosen to be used in this application because of its lower volume encumber. The coupling of power electronics technology and its adjoined cooling solution is able to ensure a power coefficient ($19 \text{ kW} \cdot \text{kg}^{-1}$) higher than the required for the Cleansky-HASTECS project target 2025 ($15 \text{ kW} \cdot \text{kg}^{-1}$). More studies have to be done to reach the target of 2035, but the results are absolutely encouraging. Using experimentally obtained conductance values as boundary condition in 3D-finite-volume-simulations, it was obtained that despite the very high heat flux densities, up to $242 \text{ W} \cdot \text{cm}^{-2}$, the junction temperature never cross over the maximal admissible value suggested by constructor. Experimental results showed that, in a real application case, CPLIP behaves well ensuring the base and, consequently, the junction temperature requirements.

Further studies are required to refine the results. The impact of the condenser and the transport line lengths on the dynamic of the loop have to be more accurately studied. It was also observed that this kind of loop has the capacity to “adapt” its behavior and evacuate the required thermal power even in the case of slight under-sizing and in presence of sudden and violent heat power increases (see take-off stage: II). Pushing it until its limits, higher power coefficient than those presented in this work can be reached to go over the requirements of 2035. The CPLIP

is able to ensure the temperature requirements with very high power to mass ratios.

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