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An investigation of current distribution over four GaN HEMTs in parallel configurations

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Abstract—GaN HEMTs are desirable for parallel configurations due to (i) relatively steady threshold voltage over a wide temperature range and (ii) the positive temperature coefficient of their on-resistances. However, their operations are sensitive to the circuit parasitics and dissimilarities between devices.

This paper investigates the current distribution among four parallel GaN HEMTs, considering two symmetrical circuit layouts of a power cell. For switching experiments, 25 V input voltage and a maximum load current of 7 A are considered. Current through each GaN HEMT is measured using stud-type, high bandwidth, coaxial shunt current sensors (CSs). The same circuit is further investigated by removing the current sensors. A second circuit is built by eliminating the CSs as to achieve high current. The circuit is tested up to 27 A/ 80 V. Here, only the voltage measurements and thermal images are obtained. Thermal images are used to evaluate the power dissipation between the four HEMTs and to correlate them with the current measurements. Further, the current waveforms are simulated using a SPICE model. The parasitic elements of the layout are calculated by ANSYS Q3D.

Index Terms—current balancing, GaN HEMT, parallel, high frequency, CVR

I. INTRODUCTION

In recent years, Gallium Nitride-based high electron mobility transistors (GaN HEMTs) have been widely studied due to their high power density capability as well as the fast switching operation (allowing them to operate beyond 100 kHz [1]). The current-carrying capability of these devices can be increased by paralleling the transistors [2].

Two main characteristics of these transistors contribute to promote power sharing among transistors and thermal stability [3]: as seen in Fig. 1, the GaN transistors have a positive temperature coefficient of on-resistance and a relatively steady threshold voltage over a wide temperature range. The drain current and on-resistance versus gate-source voltage from 25° to 150° C are illustrated in Fig. 1(a) and 1(b) respectively for a GS66516T (GaN Systems inc.). The characterization of five different samples shown in Fig.1(c) demonstrates that the difference between resistor values at a given temperature is insignificant.

The normalized on-state resistance of GS66516T in response to temperature is illustrated in Fig. 2. As per the normalized on-resistance ($R_{DS(on),norm}(T)$) versus temperature graph in the datasheet. Here, the nominal on-resistance at ambient temperature (i.e. $R_{DS(on),(T_a)}$ at 25°C) is 27 mΩ.

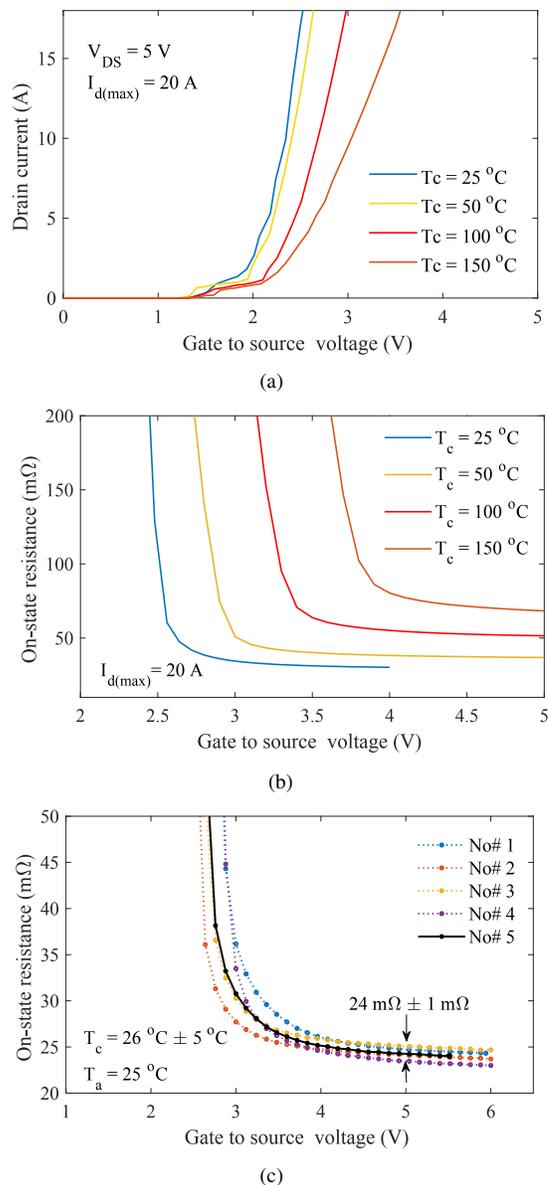


Fig. 1. GS66516T characteristics measured with Keysight B1505A power device analyzer: (a) typical drain current vs. gate voltage at different temperatures, (b) on-state resistance of a sample of 5 GaN HEMTs and (c) on-state resistance at different temperatures

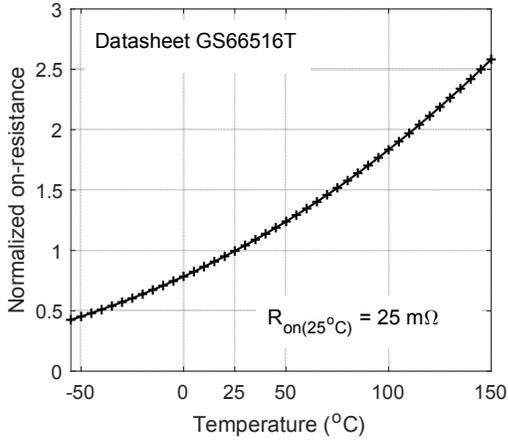


Fig. 2. Normalized on-state resistance versus temperature of GS66516T as per the datasheet.

The increase in normalized on-state resistance of the GS66516T can be express as in

$$R_{DS(on)_norm}(T_j) = \frac{R_{DS(on)_278K}}{R_{DS(on)_Ta}} \left[\frac{T_j}{278K} \right]^{2.72} \quad (1)$$

where T_j is the absolute junction temperature and 2.72 is fitting parameter of the graph. The approximate heat dissipation via a GaN HEMT P_{max} is given by

$$P_{max} = R_{DS(on)}(T_j) I_{D-}(T_j)^2 \quad (2)$$

where on-resistance is $R_{DS(on)_norm}(T_j)$ and the drain current $I_{D-}(T_j)$. Voltage drop across the drain and the source of a GaN HEMT is given by

$$V_{DS} = \frac{P_{max}}{I_{D-}(T_j)} \quad (3)$$

For few identical GaN devices in parallel, the drain-to-source voltages are uniform and they dissipate equal power. However, these values are difficult to measure accurately.

The ideal method to evaluate the current distribution in parallel transistors is by measuring it in the individual device. However, obtaining these waveforms in very high frequency applications is particularly difficult without disturbing the behaviour of the circuit. It requires low noise current sensors with very high bandwidth. Circuit modeling is another approach to estimate undisturbed current waveforms, providing a reasonably accurate model. Since measuring voltage signals causes less disturbance to the circuit, a possible method to validate the accuracy of the model is by comparing experimental and simulation results of the voltage waveforms.

To measure current in high speed applications, the most commonly used transducer are the shunt resistors [6]–[9]. They are simple, highly linear and cost effective. Coaxial shunts (current viewing resistors—CVR) are suitable for high-frequency measurements despite the constraints in continuous operations and the physical dimensions. They have extremely flat frequency response from DC to 2 GHz. In general, the

CVRs are noise immune and have fast response to the high current measurements up to 5 kA with a 20 ns rise time.

The work presented in this paper investigates two different circuits layouts for the parallel connection of GaN HEMTs. Two configurations are considered for four GaN in parallel experiments (i.e. based on the inclusion/exclusion of current sensing resistors). CVRs are utilized in one of the circuit for the measurement of current through individual transistor. Thermal images and a simulation model are also used to verify the experiment results.

In this paper, section II describes the current measurement of the four paralleled GaN HEMTs followed by an introduction to the basic configuration of the test prototypes. Section III details experiment setup and the test conditions. The experimental results are in Section IV. An analysis of the experiment and the simulation results are also detailed in Section IV. Practical issues of mounting CVRs and suggestions to address those issues are described in Section V with a conclusion.

II. AN APPROACH TO CURRENT MEASUREMENTS

The main objective of this paper is to investigate current distribution of four GaN HEMTs in parallel in two different layouts. Moreover, the consequences of adding CVRs in the power path are to be identified.

In order to compare the dispersion of current among transistors, the primary approach is to measure them using CVRs. An experiment prototype with four GaN HEMTs in parallel in a line configuration has been selected for this experiment. To identify the consequences of adding CVRs, the gate-to-source and the drain-to-source voltages of the same circuit can be compared with and without mounting CVRs on the circuit.

The second approach is to measure the gate-to-source and drain-to-source voltages of a new board with four GaN HEMTs mounted in two sides (i.e. two GaN HEMTs in each side of the PCB). A simulation model that moderately replicates the experiment results can be used to estimate the current waveforms of a circuit with no CVR mounted on. Further, by obtaining the thermal images of the second circuit, the current distribution among four transistors can be correlated.

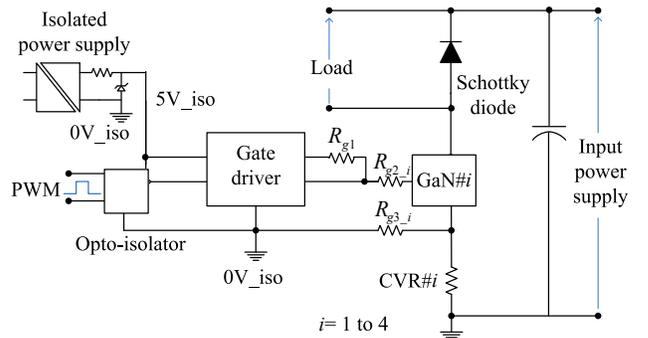


Fig. 3. Schematic diagram of the switching circuit with a clamp inductor as the load.

The best practice when designing GaN-based high frequency converters is to minimize the parasitics in both power and gate control loops. Compact prototypes can eliminate parasitic components in the circuit. Multi-layered circuits were used reduce length of routing and therefore minimize parasitic inductance losses [4]. However, to evaluate the current distribution among transistors and identify the impact of the layout, basic PCBs with two copper layer were considered to be sufficient [5].

A. Design of the prototypes

For the basic experimental prototype, a high frequency power cell (i.e. a half-bridge converter) was designed as the schematic illustrated in Fig. 3. The device under test (i.e. four GaN HEMTs in parallel) constituted the low-side switch. A high frequency Silicon Carbide Schottky diode is utilized for the high-side.

Since the gate driver reference connects directly to the source terminals of the GaN transistors the CVRs had to be kept outside of the control loop to prevent coupling the power and control loops. Moreover, connecting all sources directly would lead to un-controlled current circulation between the transistors as only one gate driver is used to drive multiple transistors in this design. To address this issue, the total gate-to-source resistance split appropriately between the connections of the driver and the gate, and the driver and the source as seen in Fig. 3 (i.e. R_{g2-i} and R_{g3-i} ; see the values in Table I). An opto-isolator and an isolated power supply provide the isolation between the gate driver input-output signals.

TABLE I
RESISTOR VALUES FOR THE TWO CASES

	Case 1	Case 2
Layout of the GaN HEMTs on PCB	Single side	Double side
Gate resistor 1 ($R_{g1}-\Omega$)	5.1	3
Gate resistor 2 ($R_{g2}-\Omega$)	0	8.1
Gate resistor 3 ($R_{g3}-\Omega$)	5.1	0

The PCB, shown in Fig. 4 (Case 1) was designed for four CVRs to measure current through each GaN transistor. The arrangement of the GaN HEMTs in this design follow a line layout on the top layer of the PCB and the CVRs are on the bottom layer. The gate control circuit is located on an extensions connected vertically to the main board.

The circuit in Fig. 5 (Case 2) has more symmetrical arrangement of GaN HEMTs. Here, two GaN devices are laying on each side. The top and the bottom devices occupy in the same area. This arraignment is feasible as the GaN devices used in this prototype are top-side cooled transistors. There are no CVRs included in this design and therefore, reduced the parasitics between source-to-ground power path.

Both Case 1 and Case 2 were built using standard double sided PCBs. The key components of the experimental prototype are listed in Table II. For the experiments, CVRs with a 25 m Ω resistance [10] shown in Fig. II-A were used. They have a lower parasitic inductance in the connection than lead-types.

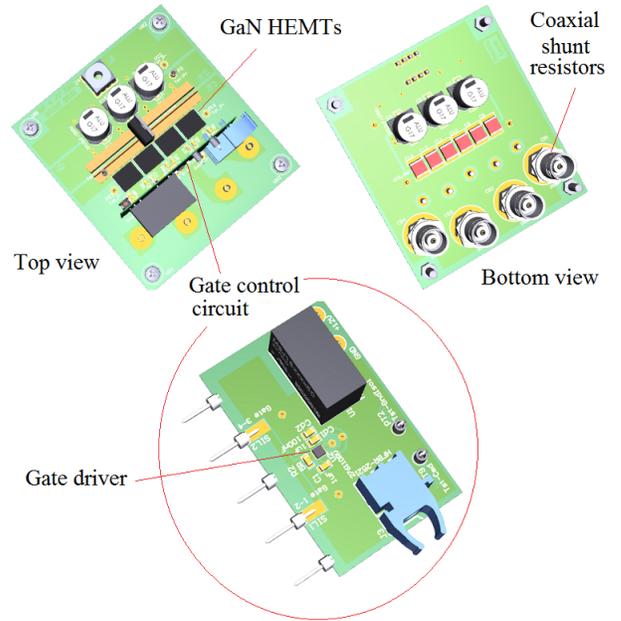


Fig. 4. Case 1: Four GaN HEMTs in line laid configuration. The gate control circuit is an extension to the main power board which fixed vertically. Provision for CVR-based current measurement are included in the design.

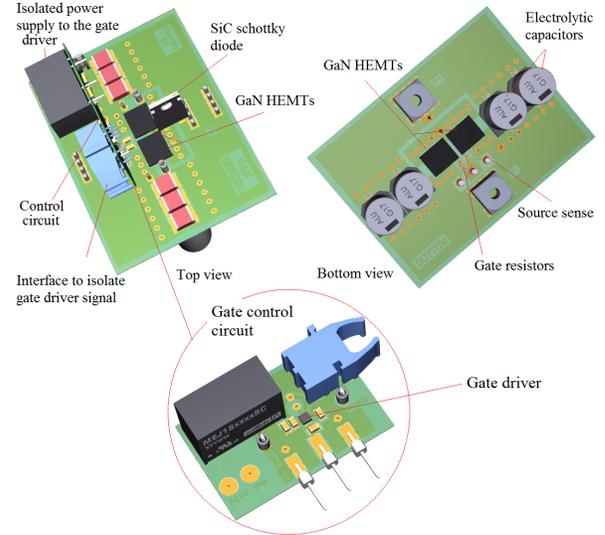


Fig. 5. Case 2: Four GaN in parallel in double side on PCB. The gate control circuit is an extension to the main power board which fixed vertically. No current measurement facilities included in the design.

III. TEST SETUP AND CONDITIONS

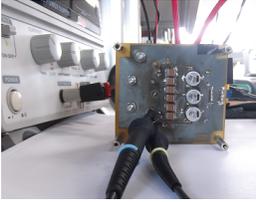
For the experiments, two oscilloscopes were utilized to observe the $V-I$ characteristics simultaneously. The shunts were measured using a digital phosphor oscilloscope (Tektronix DPO4034B, 4-Channel, 350 MHz, 2.5 GS/s) while the input voltage, load current and gate input voltages were measured using a mixed domain oscilloscopes (Tektronix MDO3024, 4-Channel, 200 MHz, 2.5 GS/s). The other accessories were high bandwidth passive probes for voltage measurements (Tektronix P6139B—500 Mhz, 10 M Ω , 8 pF) and a current probe for

TABLE II
LIST OF MAIN COMPONENTS

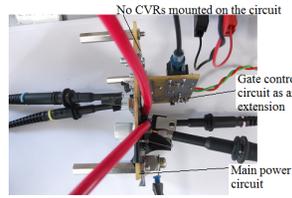
Function	Component	Manufacturer	Description	Qty
Low side switch	GS66516T	GaN Systems inc.	650 V, 60 A, 27 m Ω	4
High side sw.	IDH16G120CS	Infineon	40 A, 80 V/ns	1
Gate driver	UCC27611DRV	Texas Instruments	5 V _{out} , 4–6 A	1
Iso. power supply of the gate driver	MEJ1S1205SC	Murata	5 V, 200 mA, 1 W, 5.2 kVdc isolation	1
Fiber optics receiver	HFBR-2521Z1	BROADCOM	Links dc-5 MBd	1
Bulk capacitors	EEVEB2C100Q	Panasonic	10 μ F \pm 20%, 160Vdc, Al. Elect.	4 to 6
Filter capacitors	CKG57NX7T2W225M500JH	TDK Multilayer	2.2 μ F \pm 20% X7T 450Vdc, Ceramic	6
Current sensor (optional)	SDN-414-025	T&M Research	25 m Ω \pm 4%, 2 W, 1200 Mhz	4



(a)



(b)



(c)

Fig. 6. GaN HEMTs in line laid configuration (*Case 1*): (a) and (b) top side and bottom views of the PCB with detached CVR, (c) CVR mounted circuit.

load measurements (Tektronix TCP0030A—DC to >120MHz, 30 A—maximum range).

TABLE III
TEST CONDITIONS

Parameter	Case 1	Case 2
Input voltage (V)	25	25, 80
Load	9 μ H, \sim 100 m Ω	
Switching frequency (kHz)		200
Pulse width (ns)		500
No. of bursts		10
Pulse frequency (kHz)		1

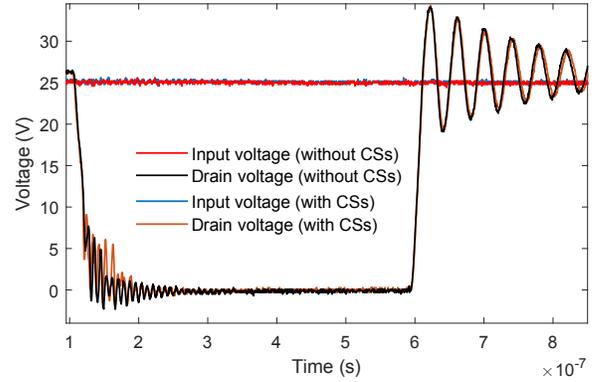
A summary of the test conditions with their nominal values are listed in Table III. The load is a solenoid with 9 μ H, 100 m Ω , 42.5 MHz bandwidth. For the *Case 1*, the input voltage limits to 25 V due to the circuit and CVRs parasitic inductances. As the CVRs were removed for the *Case 2*, it was possible to increase the voltage safely up to 80 V.

To limit self heating of the GaN devices, a digital delay/pulse generator was set to generate a pulse burst triggered at repetition rate of 1 kHz. There were 10 pulses per burst, each with 500 ns pulse width and 5 μ s pulse period. This corresponds to a 200 kHz switching frequency.

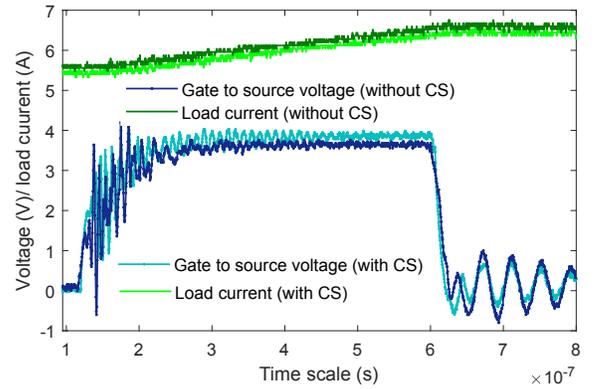
IV. EXPERIMENTAL RESULTS

A. Experimental results of Case 1 circuit

First, *Case 1* with CVRs in Fig. 6(a) was tested. Then, the CVRs were removed from the circuit as illustrated in Fig 6(b) in order to obtain measurements without connecting them. The figure shows the bottom layer of the circuit connected to the test setup and Fig. 6(c) is a side view of the circuit. The two sets of results are compared in Fig. 7 (with and without connecting CVRs: (a) drain and input voltages, (b) load current and gate, source voltages).



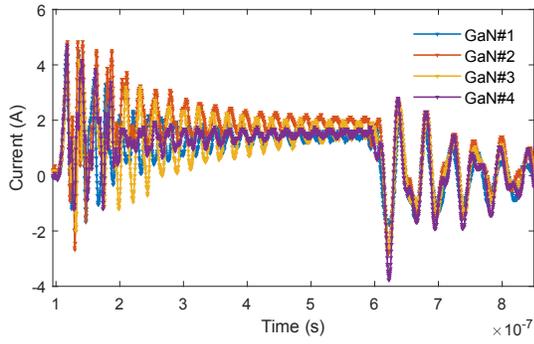
(a)



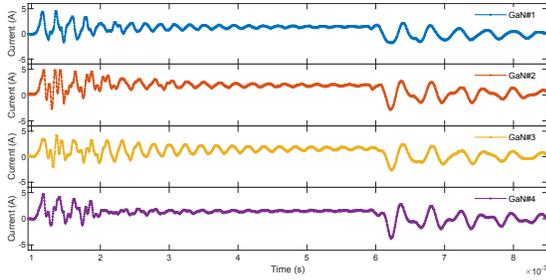
(b)

Fig. 7. A comparison of results with and without connecting CVRs: (a) drain and input voltages, (b) load current and gate, source voltages

As seen in Fig. 8, CVR-based current measurements of each GaN HEMT were obtained and the drain current distribution of four GaN HEMTs in *Case 1* are balanced. The ringing in



(a)



(b)

Fig. 8. Coaxial shunt based current measurement of circuit in Fig. 6

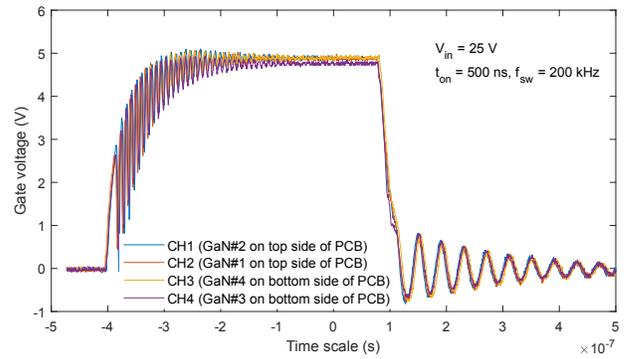
the switch-off state was caused due to the parasitics in the common-source path.

B. Experiment results of Case 2 circuit

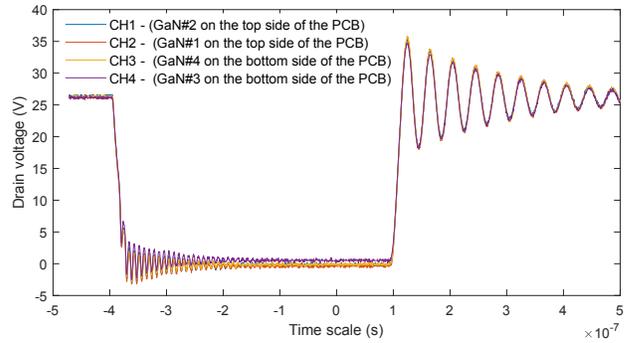
The *Case 2* circuit is more symmetrical and it does not include CVRs for current measurements. For the *Case 2* experiments, both 25 V, 7 A and 80 V, 27 A conditions were applied. Figure. 9 illustrates the gate and drain voltages under 25 V, 7 A condition. The waveforms are uniform can render equal distribution of drain current via each GaN device. Alternatively, these results are verified with thermal images (see Fig. 10(a)). Prior to obtain thermal images, a high emissivity black coating was sprayed over the shiny GaN surfaces and the PCB traces. Emissivity of the camera was set to 82% to match the ambient temperature which was about 19°C.

Figure 10(a) and (b) are illustrated the thermal images obtained at 25 V and 80 V respectively. No heat sinks were utilized in the circuit. The photos were taken after keeping 2 minutes in the operation. The estimated heat dissipation (junction to case) via a GaN HEMT at 25 V is approximately 75 mW and the junction to ambient heat dissipation is about 1.6 W. For 80 V input voltage, the estimated junction to case heat dissipation via the GaN HEMT is approximately 1.2 W and the junction to ambient heat dissipation is about 9 W. As per the results, it can be concluded that the current distribution of the GaN HEMT devices is well balanced.

A simulation model of *Case 2* was built to understand the causes of the oscillations in the current waveform. It was built with circuit parasitics and the manufacturer defined component models. The PCB parasitic components were extracted using

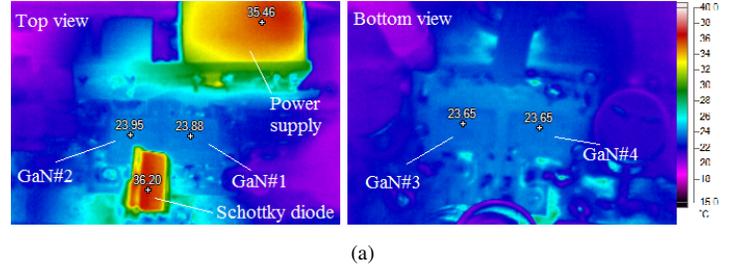


(a)

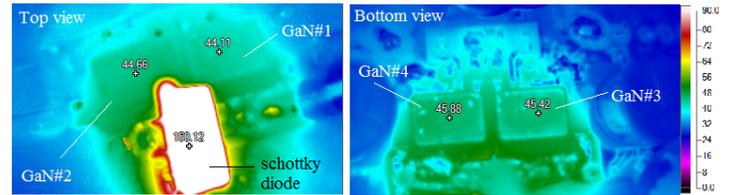


(b)

Fig. 9. Case 2: (a) Experimental prototype with current sensing via coaxial shunt resistor. (b) CVR-based measurements during transients. Input voltage is at 25 V.



(a)



(b)

Fig. 10. Thermographic images captured at different load currents the room temperature around 19°C of the *Case 2* board: (a) load current 7 A and input 25 V, (b) load current of 27 A and input at 80 V.

ANSYS-Q3D software. The aim was to reproduce experiment results using large signal modeling technique using LTSpice.

A simplified circuit with PCB parasitic components as in Fig. 11 was used to define the simulation model. Further, the control circuit parasitic components were also included.

As seen in the results comparison in Fig. 12, the simulation

Device	Case temperature ($^{\circ}$ C)	Normalized on resistance	On resistance ($m\Omega$)
25 V / \sim7 A			
GaN#1	23.88	0.9862	24.66
GaN#2	23.95	0.9868	24.67
GaN#3	23.65	0.9841	24.60
GaN#4	23.65	0.9841	24.60
80 V / \sim27 A			
GaN#1	44.11	1.1798	29.49
GaN#2	44.66	1.1853	29.63
GaN#3	45.42	1.1931	29.83
GaN#4	45.88	1.1978	29.94

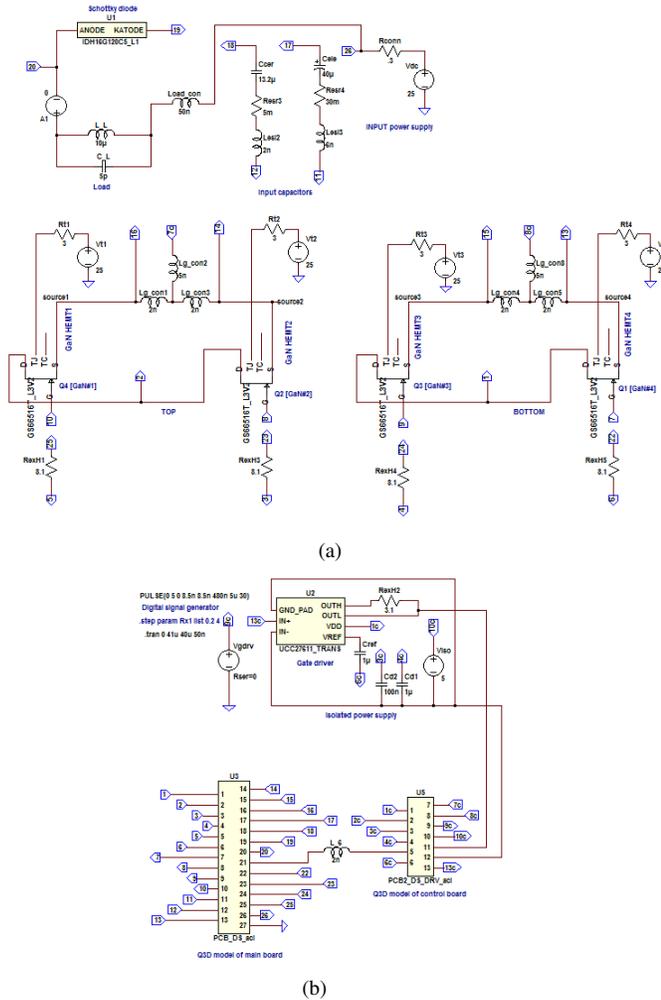


Fig. 11. Parasitic components of the circuit model: (a) power loop and (b) control loop and the Q3D parasitic models

model can be improved to obtain more accurate current waveforms. Since the gate and drain voltage waveforms in *Case 2* are comparably with lower to *Case 1* with CSs, low noise drain current waveforms can be expected.

V. CONCLUSION

A fairly equal current distribution is observed among the components in both circuits during the switching operations, resulting in a stable thermal equilibrium. However, the insertion of large CSs has a negative impact on the dynamic

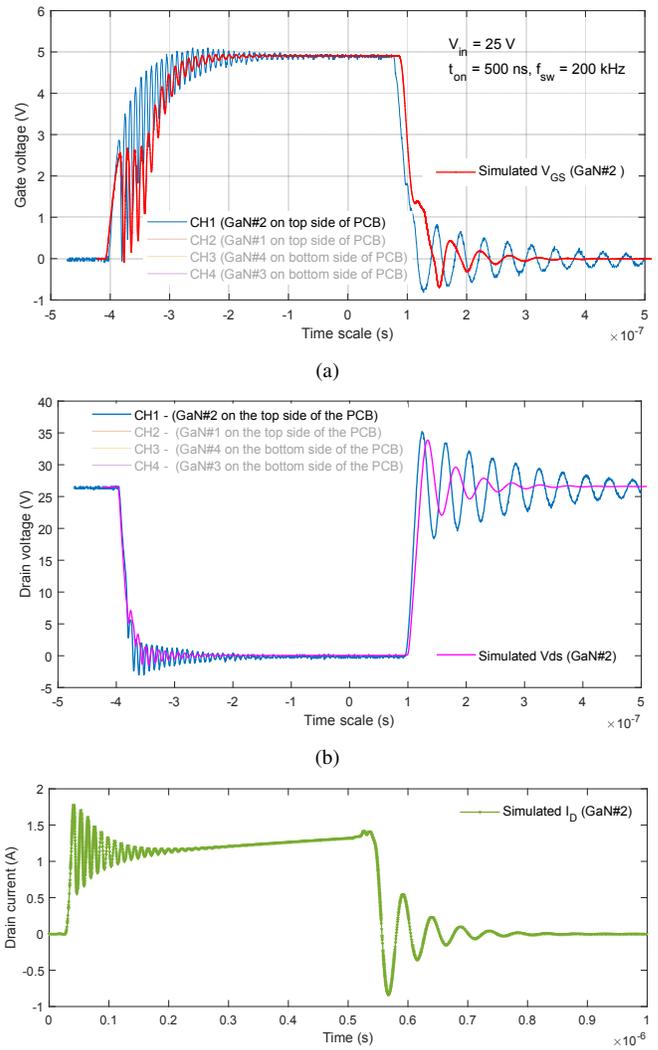


Fig. 12. Experiment results validated with a SPICE simulation: *Case 2* circuit and simulated drain current waveform

performance of the transistors that limits the current/voltage range during experiments. Circuits without CSs perform well in higher voltages. By using the waveforms acquired from these prototypes, we showed that the simulation provides a satisfying accuracy. Hence, it can be used to calculate current sharing for the board without CSs. Regarding the effect of the layout; the double-side layout leads to a more symmetrical design which can be a viable solution for current balancing in the devices.

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