

Die Interconnection for Power Module 3.0

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Needs for Interconnections

Passives and active components need “multi functional” interconnections :

Electrical - Thermal – Mechanical (ETM)

One, two or three functions associated to perform solutions for 3D integrated modules

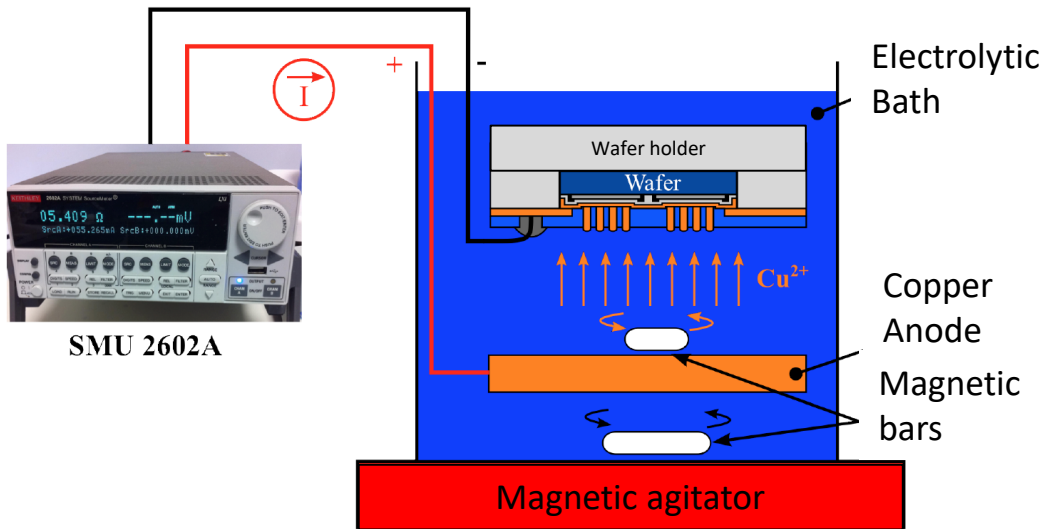
High performance is required for each physical domain and high reliability (critical)

Several ways

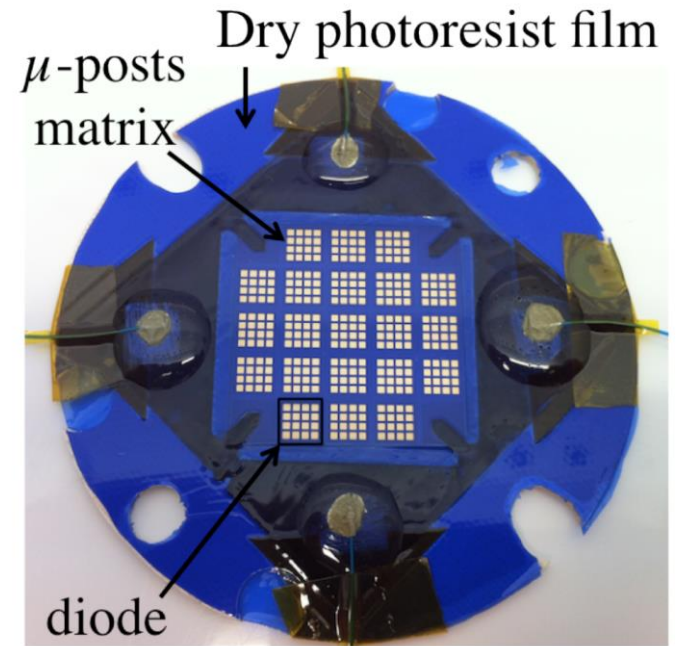
- Conventional :
 - Brazing, bonding, sintering, electroplated via... → not addressed here
- Non conventional :
 - Diffusion bonding, pressed nano post, pressed foam, electroplated via...

- Copper to copper “direct bonding”
- Copper nano post (ETM)
- Copper nano post in PCB environment (ET)
- Foams in PCB environment
- Conclusion

Example “direct copper to copper bonding”



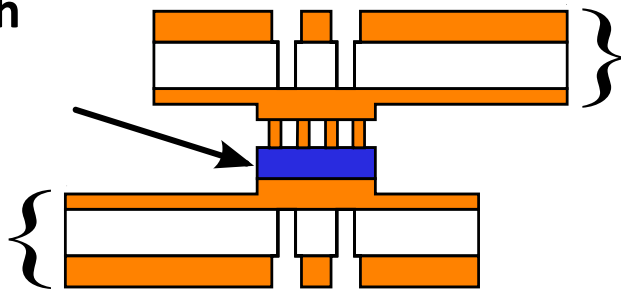
«Bassem Mouawad » [1]



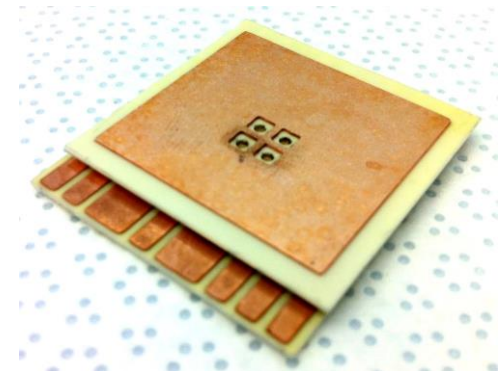
μ post height : 80-90 μm

Diode with μ posts

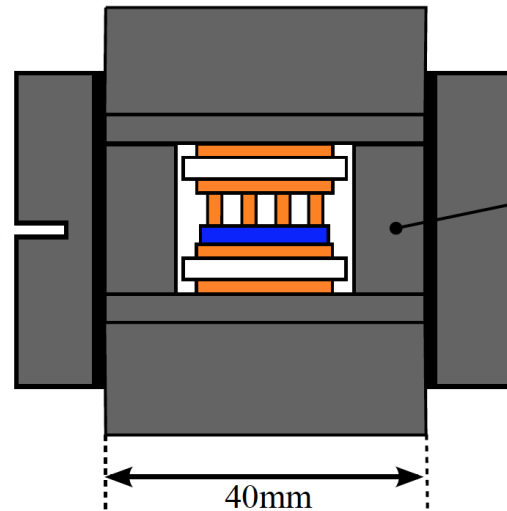
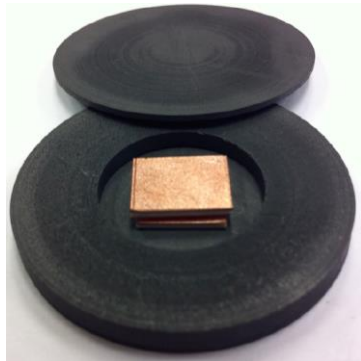
Low side DCB



High side DCB

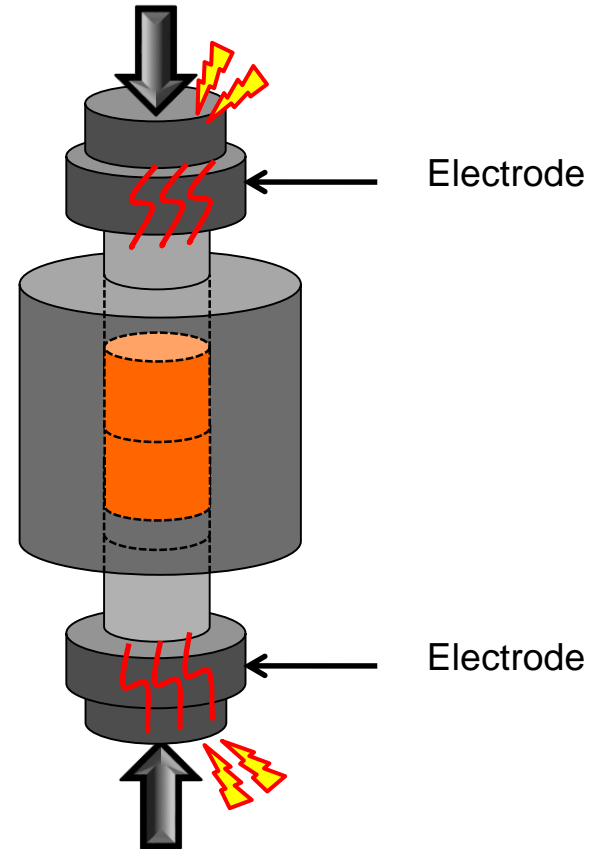


Example “direct copper to copper bonding”



Graphite jig

SPS System

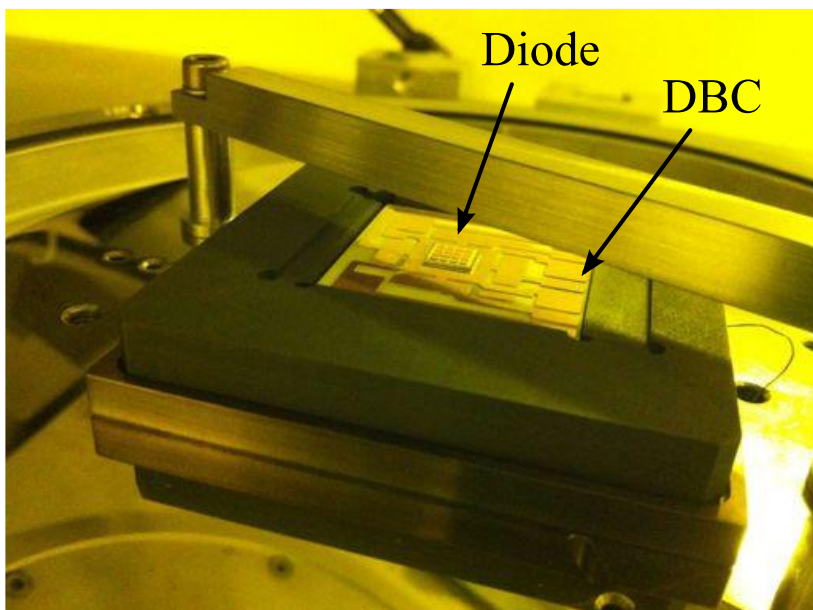


Parameters :

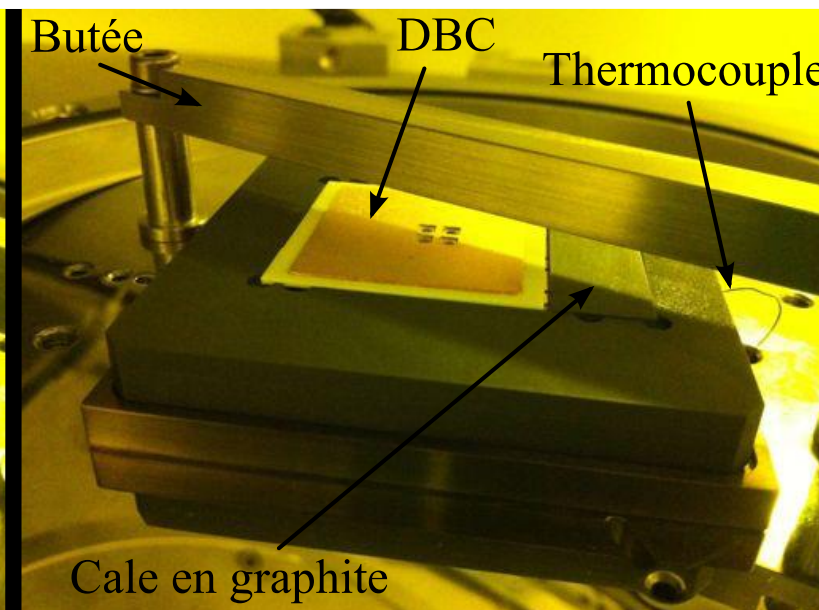
- Atmosphere vacuum 10^{-2} torr
- Peak Temperature 200°C and 300°C (5min)
- Ramp $100^{\circ}\text{C}\cdot\text{min}^{-1}$
- Pressure few MPa (estimated)

Example “direct copper to copper bonding”

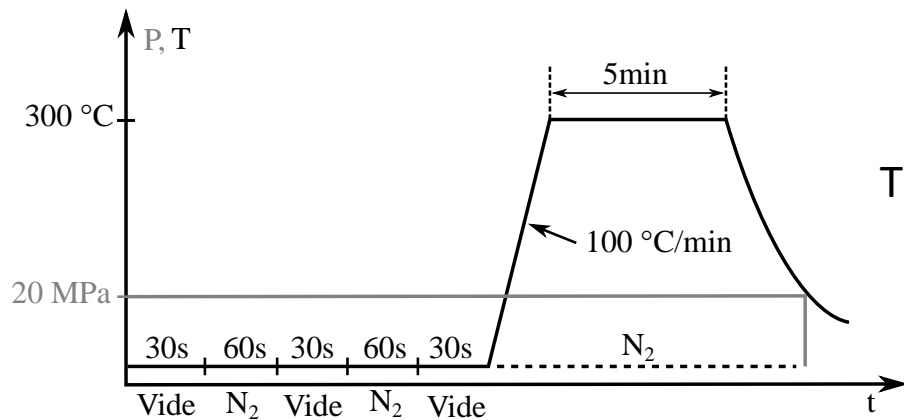
RTA oven



STEP 1



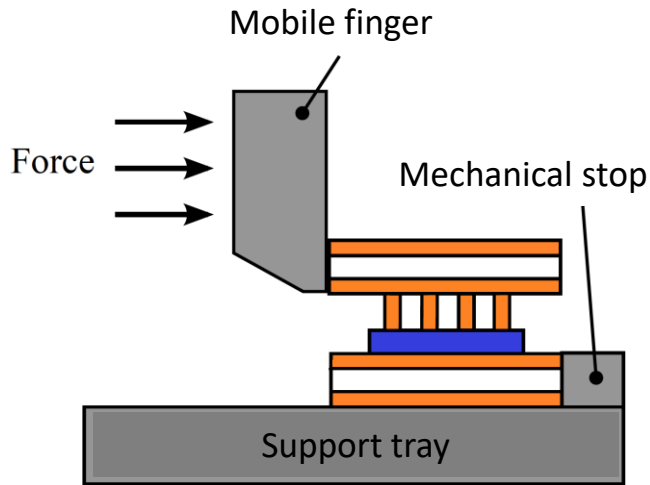
STEP 2



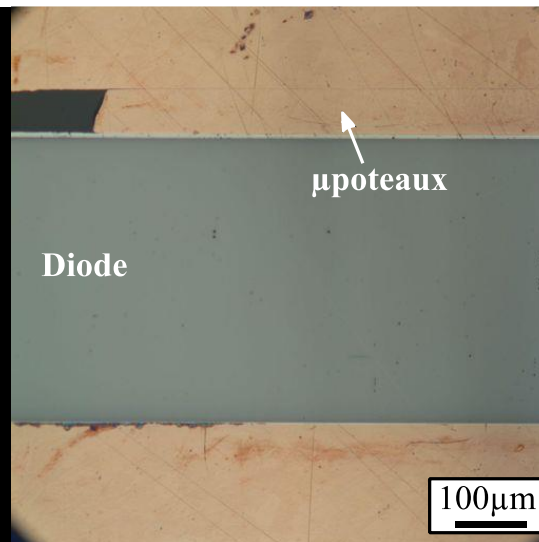
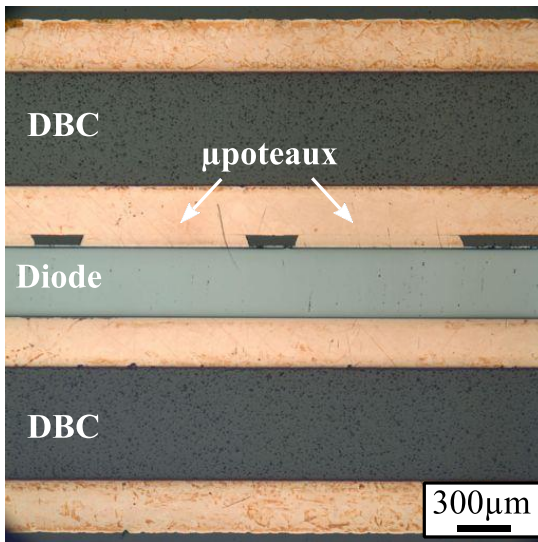
Thermal profile for RTA oven

Direct copper to copper bonding

Mechanical Results

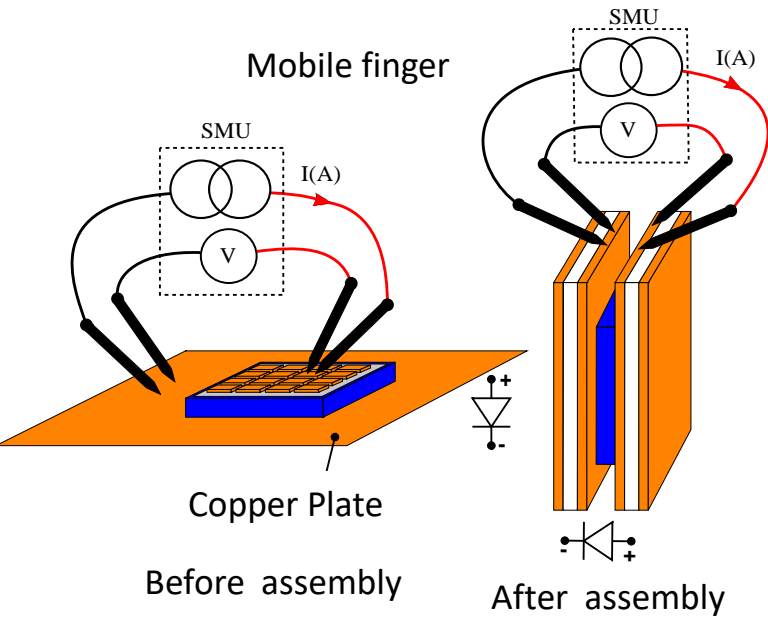


| SPS | | | | | RTA | | | | |
|-----|--------|-------|----------------------|---------|-----|--------|-------|----------------------|---------|
| N° | T (°C) | F (N) | S (mm ²) | τ (MPa) | N° | T (°C) | F (N) | S (mm ²) | τ (MPa) |
| 1 | 300 | 113 | 2.63 | 43 | 1 | 300 | 199 | 11.8 | 16 |
| 2 | 300 | 184 | 8.9 | 20 | 2 | 300 | 93 | 7.3 | 12 |
| 3 | 300 | 275 | 8.4 | 32 | 3 | 200 | 133 | 5.2 | 25 |
| 4 | 300 | 275 | 8.9 | 30 | 4 | 200 | 187 | 4 | 46 |
| 5 | 200 | 181 | 7 | 25 | | | | | |
| 6 | 200 | 21 | 1.1 | 18 | | | | | |
| 7 | 200 | 31.5 | 5.6 | 5.6 | | | | | |
| 8 | 200 | 176.5 | 8.4 | 21 | | | | | |

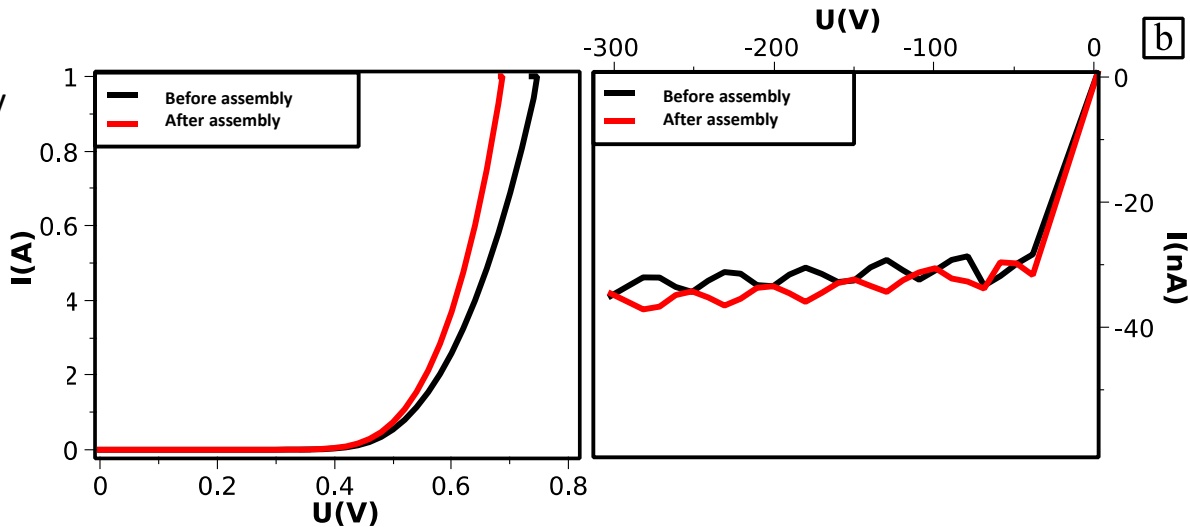


Direct copper to copper bonding

Electrical Results

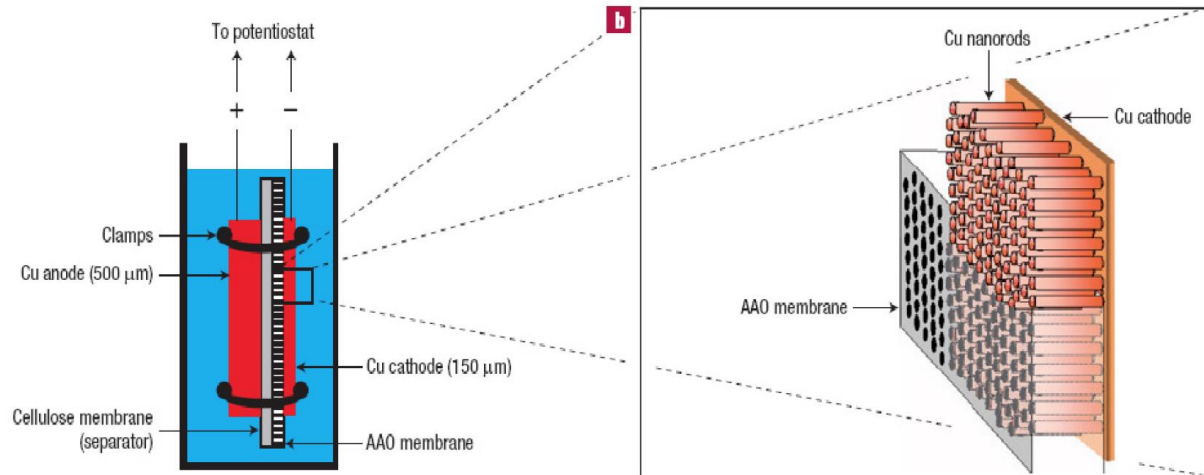
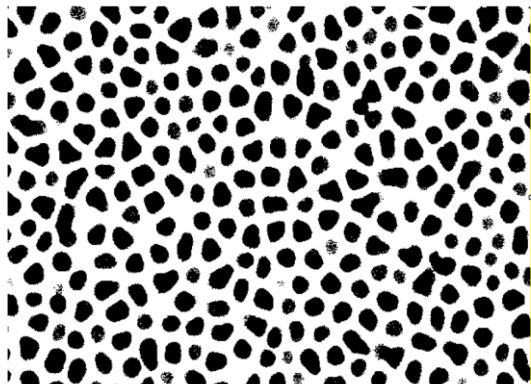
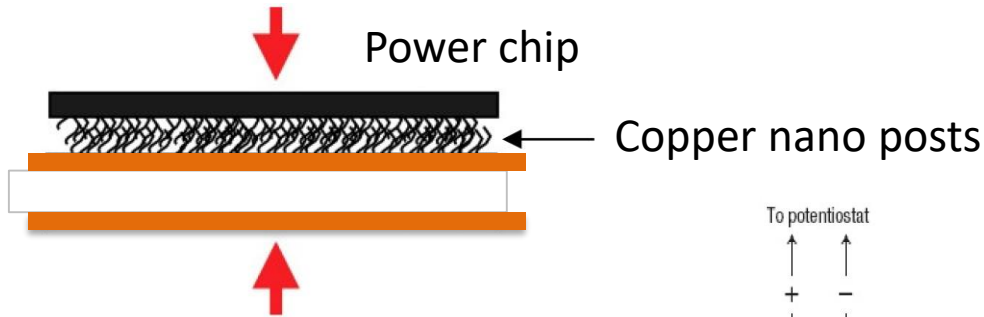


- Improvement of direct characteristic
- No impact in reverse polarization



Copper nano post → nano scratch

A simple principle...

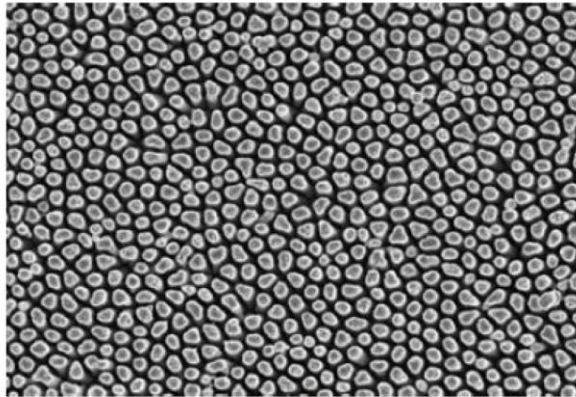


Copper nano wires electrodeposition [2]

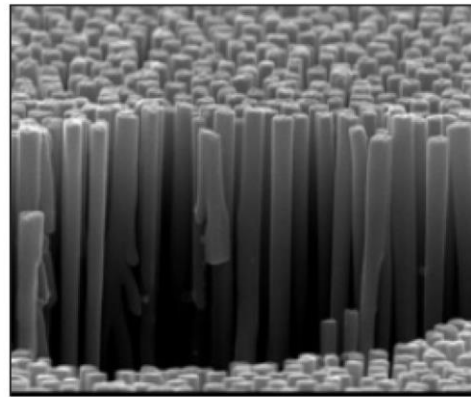
AAO : Anodic Aluminium oxyde membrane

- Nanostructured matrix, 200nm pores, thickness 60 μm
- Around $1 \cdot 10^9$ pores / cm^2

Copper nano post assembly → Results

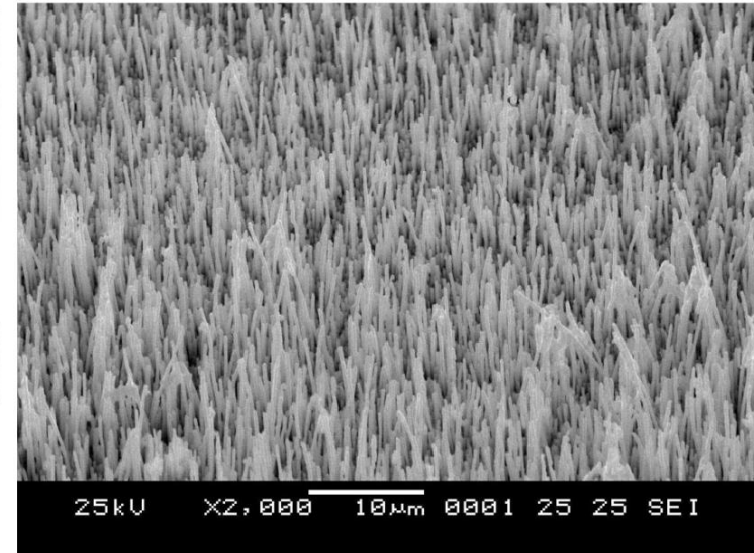


1 μm

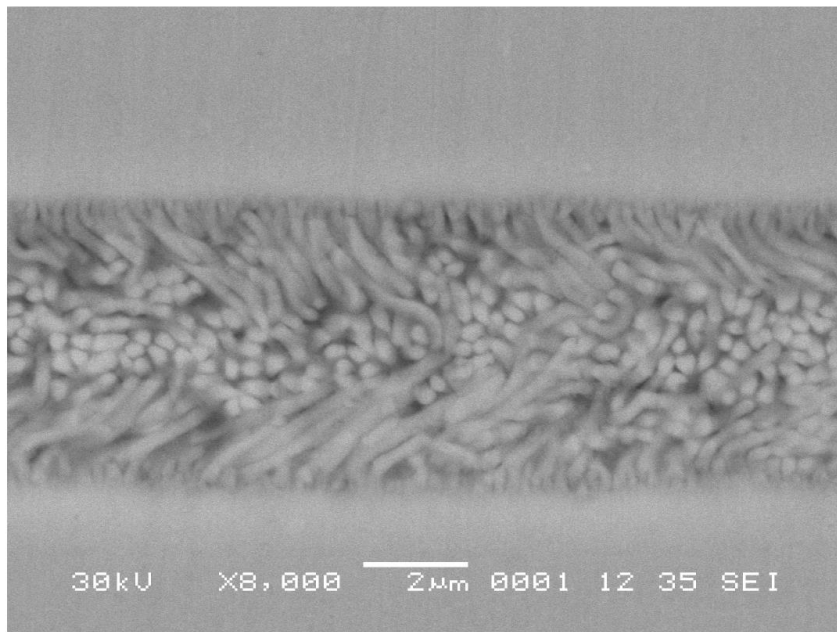


2 μm

Top view and side view of nano posts [3]

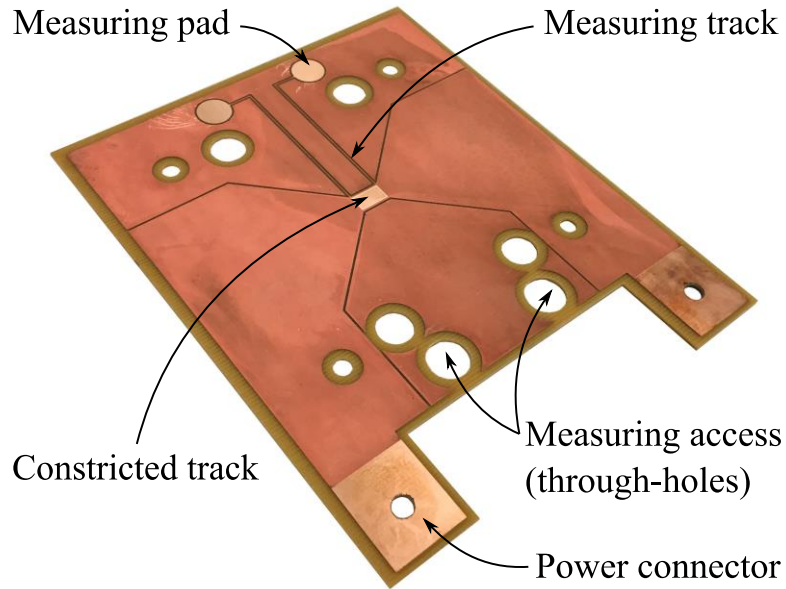


Top view of the nano posts [4]



- Acidic or alkaline electrodeposition bath
- Room temperature assembly
- High pressure applied up to 100MPa
- 60N/cm² pull test
- 80N/cm² shear test
- 10X the brazing resistance

A 0.8 mm high temperature core with two 105 μm thick copper layers



PCB substrate with constricted area, its connectors and kelvin measuring tracks [5]

Power connectors

- For electrical and thermal characterization

Constricted area

- Bare copper area for the interconnection manufacturing
- Constriction is done for helping thermal characterization

Measuring pads and tracks

- Additional contacts for Kelvin measurements

Measuring accesses

- To the opposite substrate measuring pads

Brown oxidized remainder copper and ground planes to increase prepreg adhesion

➤ Opened dry film on constricted area

- Dry film deposition ($\approx 45 \mu\text{m}$) on the whole PCB surface;
- Opening of the dry film over the constricted area.

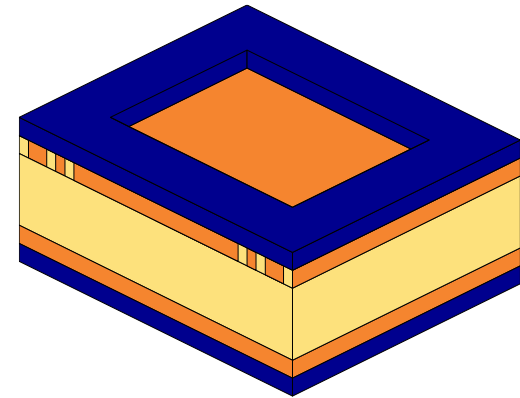


Figure 5: Manufacturing process of interconnection on the PCB substrate

Opened dry film on constricted area

➤ **Copper electro-etching on the constriction**

- a. $\approx 7 \mu\text{m}$ copper electro-etching (pulsed waveform) to increase adhesion of the surface.

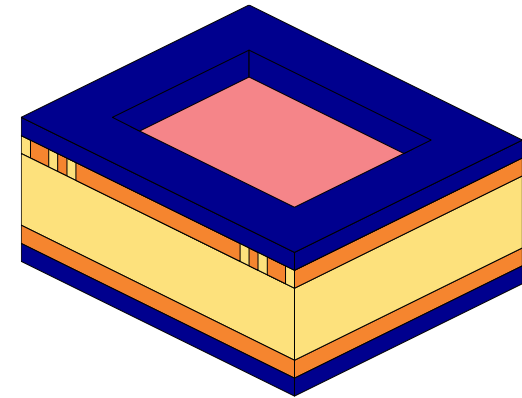


Figure 5: Manufacturing process of interconnection on the PCB substrate

Opened dry film on constricted area
Copper electro-etching on the constriction

➤ **Macro post electroplating (overflowing of dry film)**

- a. $\approx 60 \mu\text{m}$ copper electroplating (pulsed waveform)
The electroplating profile is adjusted to have the top of the post slightly higher than the dry film to ensure a complete filling of the cavity.

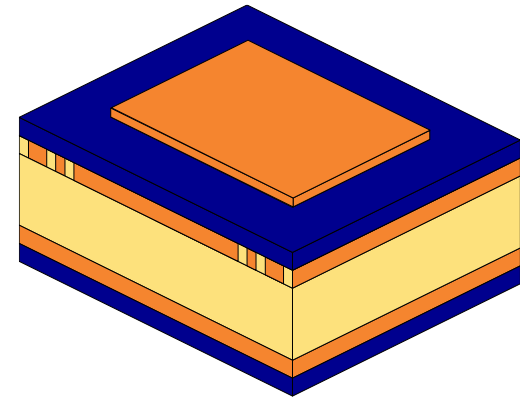


Figure 5: Manufacturing process of interconnection on the PCB substrate

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)

➤ Leveling of the macro post by electro-etching

- a. $\approx 7 \mu\text{m}$ copper electro-etching (pulsed waveform)
The copper post is etched to obtain a flushed surface between the dry film and the copper post. This is the condition to ensure a correct sealing for the forthcoming steps.

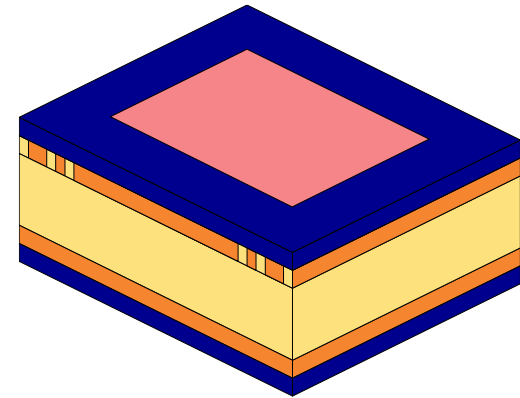


Figure 5: Manufacturing process of interconnection on the PCB substrate

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)
Leveling of the macro post by electro-etching

➤ Nano wires electroplating by pressed anode

- A nanoporous membrane is placed on top of the copper post;
- A solution of copper sulfate is spread over to act as an initiator;
- 2 layers of cellulosic papers are added on top as solution buffer;
- A copper anode is pressed on top of this assembly;
- Copper is electroplated during ≈ 1 hour through the membrane using a pulsed waveform.

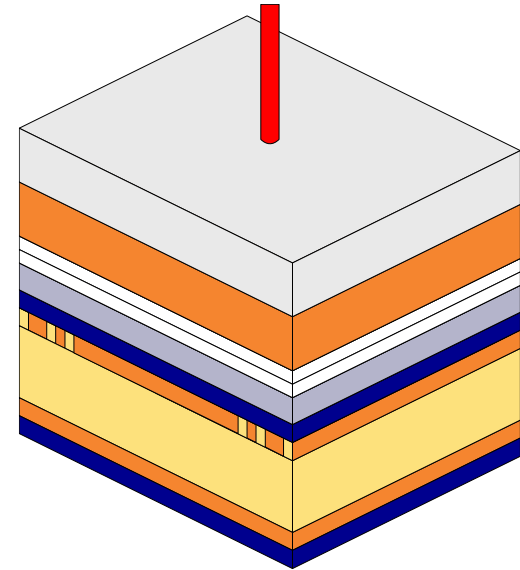


Figure 5: Manufacturing process of interconnection on the PCB substrate

- Opened dry film on constricted area
- Copper electro-etching on the constriction
- Macro post electroplating (overflowing of dry film)
- Leveling of the macro post by electro-etching
- Nano wires electroplating by pressed anode

➤ Membrane filling by distanced anode

- Once the electrodeposition have been initiated
- The 2 layers of cellulosic papers are removed;
 - The anode is placed further away;
 - ≈ 6 hours copper electroplating is done until the membrane is filled.

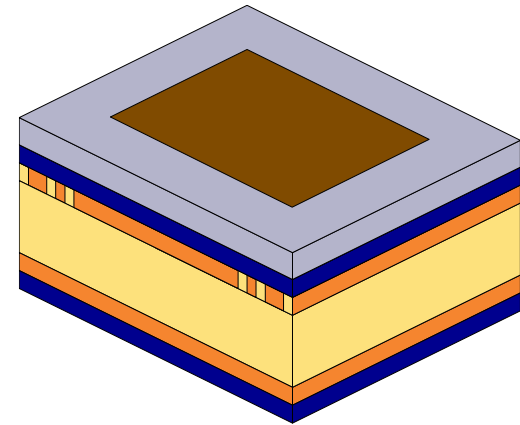


Figure 5: Manufacturing process of interconnection on the PCB substrate

- Opened dry film on constricted area
- Copper electro-etching on the constriction
- Macro post electroplating (overflowing of dry film)
- Leveling of the macro post by electro-etching
- Nano wires electroplating by pressed anode
- Membrane filling by distanced anode

➤ Dry film and membrane removal

- Sodium hydroxide treatment at 45°C during half an hour.

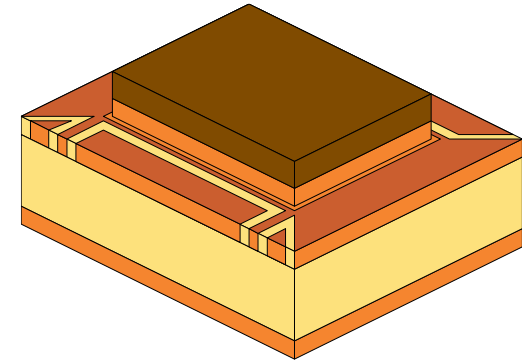
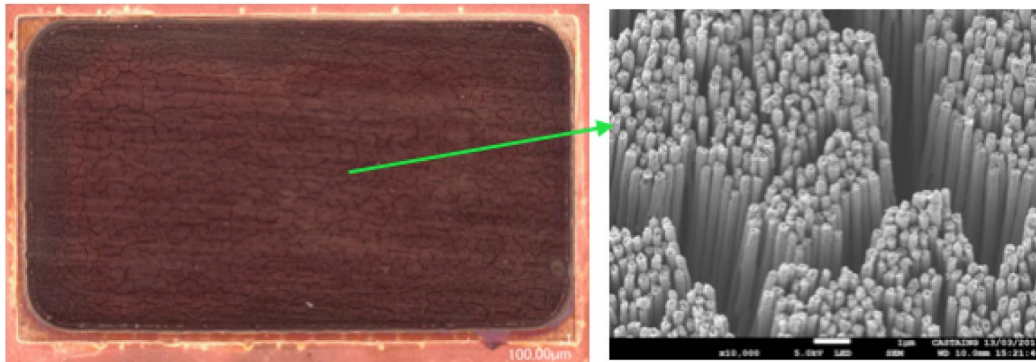


Figure 5: Manufacturing process of interconnection on the PCB substrate

Proposed solution combines

- PCB substrates **(a)**
- having a macro post and nano wires interconnection
- sandwiching a die **(d)** surrounded of core **(c)**
- assembled by thermo-compression of prepregs **(b)**

High level of integration

1. Double-side cooling possible (symmetrical structure)
2. Full copper and flexible interconnection
3. Expected resistant to cyclical stresses
4. Elementary block for power converter

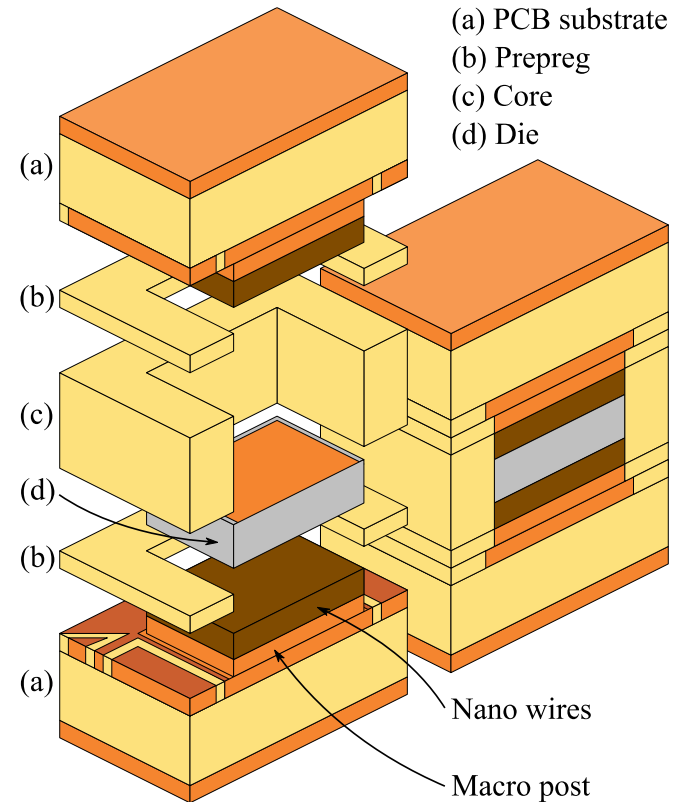
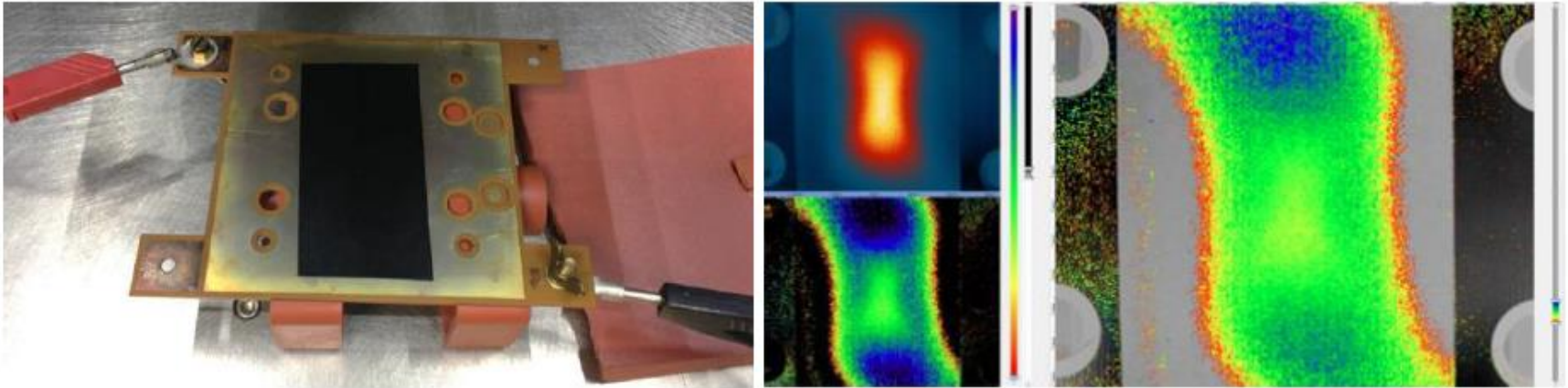


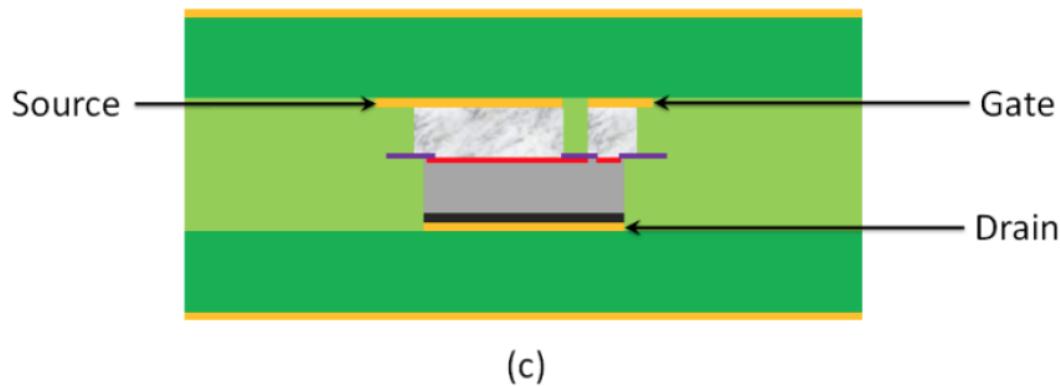
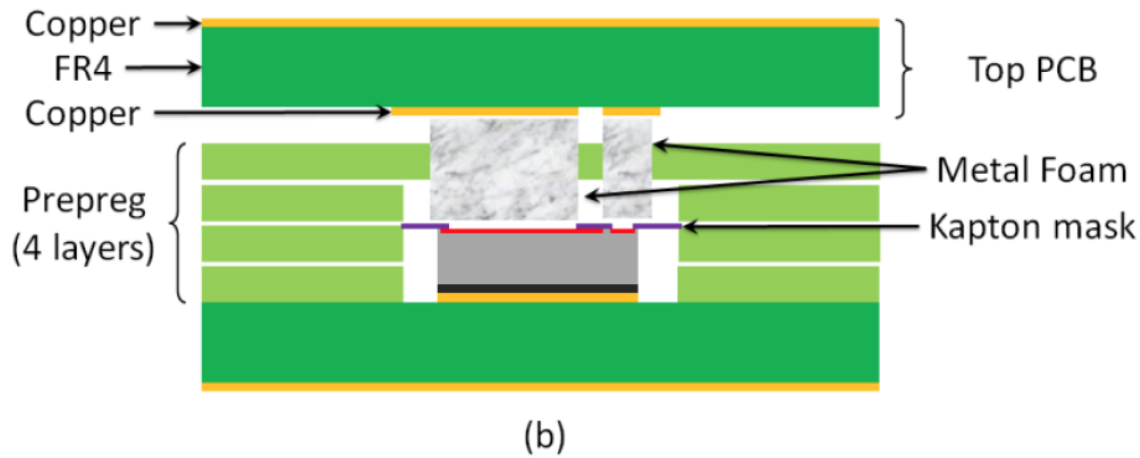
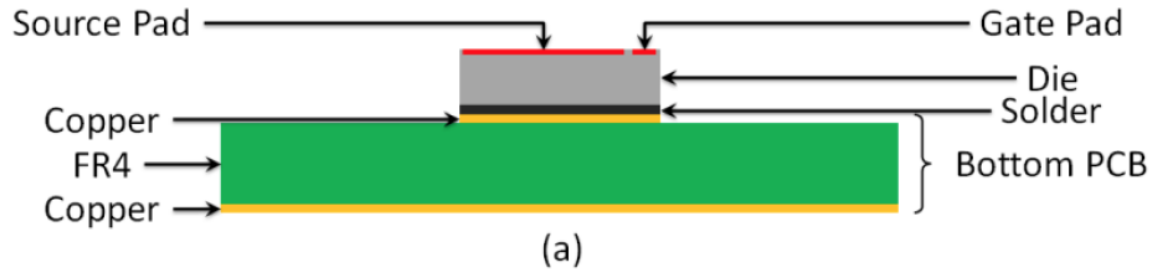
Figure 3: Cross section schematic of the assembly with macro and nano structured interfaces



Lock-in thermography to detect hot spot inside PCB [6]

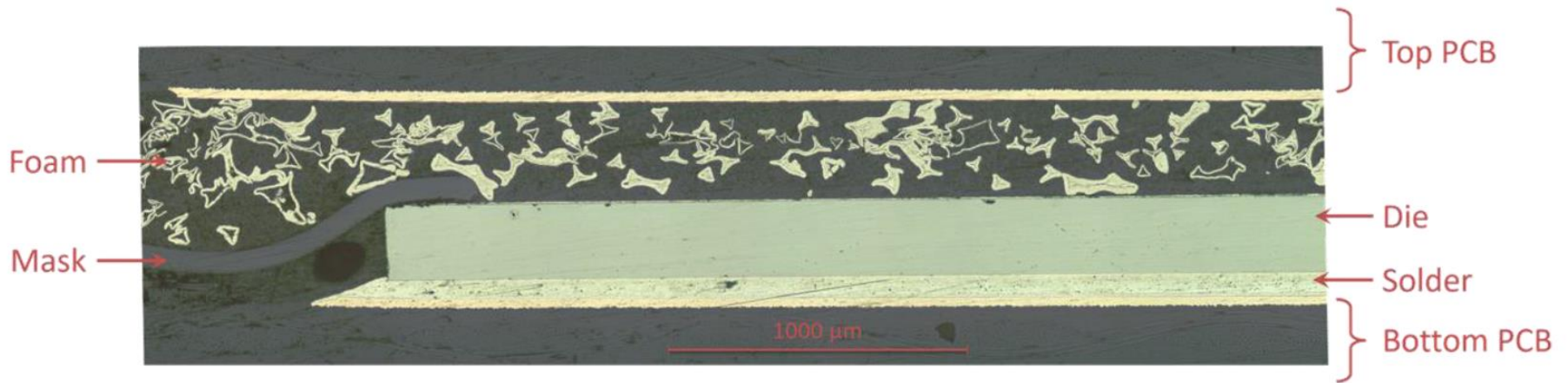
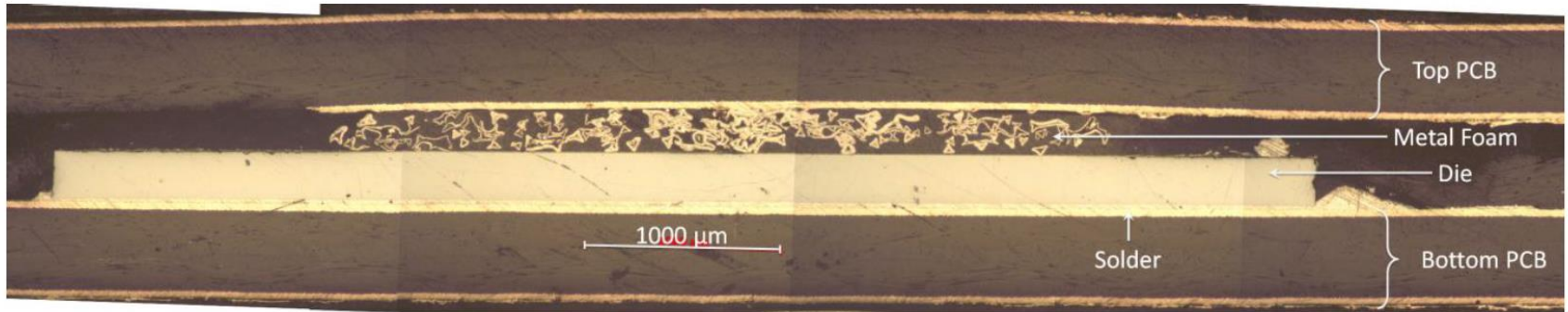
- Low specific resistance $< 100\mu\Omega.\text{cm}^2$
- Compatibility with PCB technology
- Electro - Thermal functions
- Thermal characterization and reliability : test to do...

Metal foam for contacts in PCB : Principle



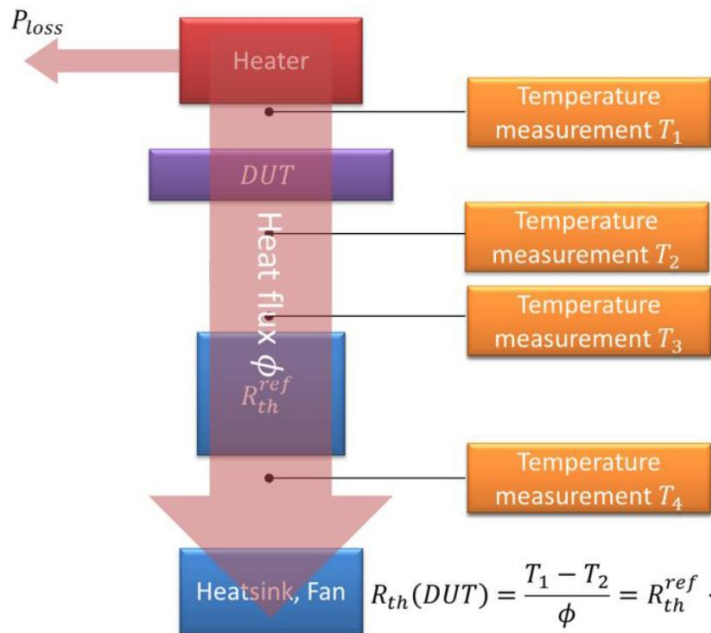
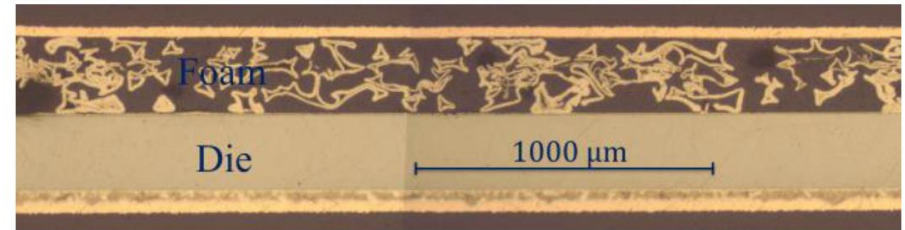
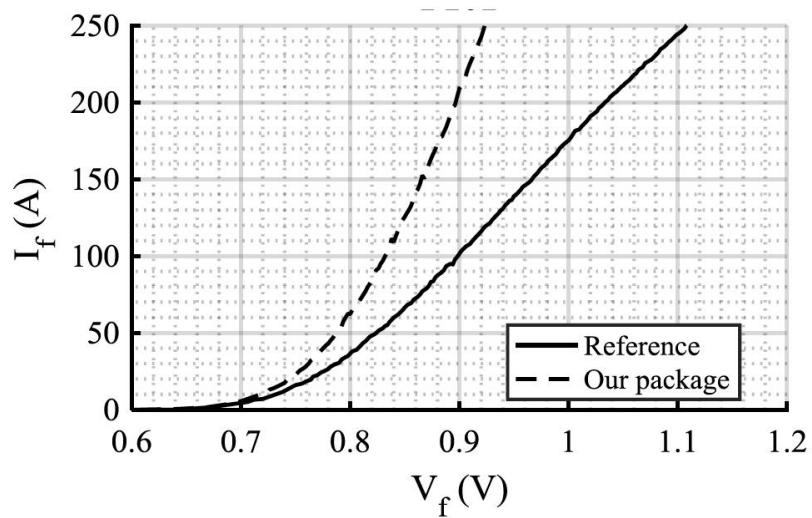
From Yoann
Pascal SATIE [8]

Metal foam for contacts in PCB : Realization



Metallographic sections

Metal foam for contacts in PCB : Results



Estimation of thermal conductivity :
 $\lambda = 2.2 \text{ Wm}^{-1}\text{K}^{-1}$

$$R_{th}(DUT) = \frac{T_1 - T_2}{\phi} = R_{th}^{ref} \cdot \frac{T_1 - T_2}{T_3 - T_4}$$

- Many way to make interconnects...
- Direct bonding or pressed surface depends on environment (DBC, PCB)
- Only academic studies, many parameters to control final characteristics
- Compatible for 3D integration... but many tests to do...

- [1] Bassem Mouawad PhD thesis « Assemblages innovants en électronique de puissance utilisant la technique de « Spark Plasma Sintering » 2013
- [2] P. L. Taberna, et al., "High rate capabilities Fe₃O₄-based Cu nano-architected electrodes for lithium-ion battery applications", Nature Materials, vol. vol. 5. pp. 567-573. ISSN 1476-1122, 2006.
- [3] Quoc hung Luan PhD thesis Etude et mise en œuvre de techniques d'assemblages hybrides pour l'intégration tridimensionnelle en électronique de puissance, 2010.
- [4] Etude et caractérisation d'une nouvelle connectique adaptée à l'intégration tridimensionnelle pour l'électronique de puissance, 2010.
- [5] Bojan Djuric, Vincent Bley, Julien Morand, Olivier Dagut, Jean-Pascal Cambronne, Stefan Mollov Double Side Interconnection for Vertical Power Components Based on Macro and Nano Structured Copper Interfaces and Printed Circuit Board Technologies, MINAPAD 2019 May 22nd-23rd, Grenoble France.
- [6] Morgane Mousnier PhD Thesis «Apport de la thermographie infrarouge à l'analyse de défaillance de composants et systemes electroniques ». 2019
- [7] Yoann Pascal PhD thesis « Etude multicritère pour l'enfouissement partiel ou total de convertisseur d'électronique de puissance dans un circuit imprimé 2019.

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