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# A sub-pJ/bit, low-ER Mach-Zehnder-based Transmitter for chip-to-chip Optical Interconnects

Audrey Michard, Jean-François Carpentier, Nicolas Michit, Patrick Le Maître, *Member, IEEE*, Philippe Bénabès and Pietro M. Ferreira, *Senior Member, IEEE*

**Abstract**—Designing high-speed and low-power interconnects is a challenge for high performance computing applications, while silicon photonics can provide attractive solutions to perform high-density communications. This paper presents an electro-optic transmitter operating at 20 Gbps (gigabit per second), as a first step toward the demonstration of chip-to-chip optical links. The architecture is based on a dual-drive Mach-Zehnder interferometer co-integrated with a 55-nm CMOS driver. Design optimizations and trade-offs analysis enable low-energy and negligible bit error rate ( $BER < 10^{-12}$ ) transmission at 20 Gbps, by exploring a firstly reported low extinction ratio (ER) modulator. A wire-bonding board assembly is then carried out to co-integrate hybrid transmitter. Co-simulations are presented and show good agreement with experiments. Combined with an adequate MZM bias, this solution achieves a minimal energy consumption of 0.9 pJ/bit while ensuring a sufficiently large ER of 0.73 dB for chip-to-chip interconnects applications.

**Index Terms**—Silicon photonics, chip-to-chip communication, hybrid integration, co-simulation, Mach-Zehnder modulator

## I. INTRODUCTION

SILICON photonics (SiP) is considered as a prime technology for high performance computing (HPC) applications [1], [2]. Indeed, future supercomputer architectures require high-speed and high-capacity data transmission solutions, but traditionally used metal interconnects suffer from relevant crosstalk and bandwidth limitations. Optical technologies are therefore emerging as attractive solutions for short range communications, and are suitable, for instance, to connect the cores (CPU/GPU) and the multiple memory resources of a supercomputer. Moreover, silicon photonics has the potential for large-scale industrialization, thus addressing the cost, size, and energy challenges of optical interconnects. Such advance is already proved in the electronic-photonics system proposed by C. Sun *et al.* in 2015, where over 70 million transistors and 850 photonic components are integrated on a single chip to provide logic, memory, and interconnect functions [3].

Very low distance chip-to-chip links are of growing research interest, but few papers demonstrate a complete proof of

concept [3], [4] and some references only concentrate efforts in transmitter [5], [6]. For low-power operation, a photonic ring-based resonator operates at low voltage modulation. However, ring-based solutions must be thermally controlled, and moderate power would be required for thermal tuning [3]. The choice for a Mach-Zehnder modulator (MZM) rather than a ring resonator is dictated by the insensitivity of the MZM interferometer to temperature and process variations. Since MZM can operate over a wide optical bandwidth, it does not require any wavelength tuning, as ring-based solutions does [7]. This advantage is quite explored in the literature, when the MZM remains a reliable solution for a low-power transmitter [6], [8], [9].

As regards the driver architecture, state-of-the-art drivers target, for the most part, large output voltage swings to ensure a large optical modulation amplitude [8], [10], [11]. In [10] and [11], the driver model is based on differential cascode output stages to allow a high voltage swing of four times the nominal supply. In [8], each driver stage is based on stacked inverters, pre-driven by DC-shifted input signals. As a result, a high ER of 4 to 6 dB is achieved. However, all previous demonstrations target datacom applications (100G and 400G small form factor optical modules). For a chip-to-chip HPC application, power consumption constraint is not compatible with a high output swing and a high ER. Thus, a simpler architecture should be considered for an extremely low power consumption as suggested S. Tanaka *et al.* while demonstrating a highly power-efficient (1.59 pJ/bit at 56 Gbps) SiP transmitter using an MZM and a 28-nm CMOS driver [6].

This paper presents an electro-optic transmitter operating at 20 Gbps, as a first step toward the demonstration of short-range optical links. Objectives are to highlight the trade-offs involved in the design of such a link and to fabricate a prototype. Transmitter architecture is based on a dual-drive 850  $\mu\text{m}$ -long Mach-Zehnder interferometer, while the 55-nm CMOS drivers adopt a simple and low-power inverter chain topology. The transmitter demonstrates operation at an  $ER = 0.73$  dB, which is required to achieve 0.9 pJ/bit driver energy consumption. This paper does not claim any figures of merit at the state of the art but proposes a co-optimization framework for short range HPC applications never presented before. This framework includes the following specifications: low energy consumption compatible with chip-to-chip applications and mature technology-based devices intended for short term industrialization. For this reason, the STMicroelectronics industrial photonic platform (PIC25G) [12] is considered.

The paper is organized as follows. Section II revises the

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optical interconnection for chip-to-chip communications presenting the trade-offs between the bandwidth, area, energy and performance. Section III describes the proposed hybrid transmitter detailing the MZM, and the electric driver designs. Section IV validates the proposal with the MZM, and the electric driver measurements. Moreover, it highlights the hybrid transmitter integration on board by co-simulations and measurements of the demonstrator. Finally, paper conclusions are given in Section V.

## II. OPTICAL INTERCONNECT FOR CHIP-TO-CHIP COMMUNICATIONS

High Bandwidth Memory (HBM) systems have been presented as a revolutionary solution to meet the capacity and bandwidth requirements currently identified in high performance computers [13]. HBM uses vertically stacked memory chips and enables a bandwidth higher than 100 GBps (gigaByte per second) per stack. This work aims to replace classical electrical interconnects by optical links since optical interconnects enable the management of high-density communications. A solution uses a silicon photonics-based interposer as illustrated in Fig. 1(a), which supports optical functions to convert electrical data into the optical domain and vice-versa. Such assembly might be performed using 3D flip-chip methods to benefit from close integration and lower parasitic losses.

A transceiver module is implemented from end to end of the optical link, i.e. in the process unit and in the memory chip. Space division multiplexing (SDM) is used to simultaneously deliver several parallel spatial channels, thus increasing the system capacity. A comb laser is also integrated onto the interposer to provide input light at several wavelengths. An arrayed waveguide grating (AWG) [14] is used to separate all wavelengths that are distributed in each SDM channel using successive 1:2 power splitters. Fig. 1(b) shows the SDM electro-optical link, which comprises a bank of modulators in the transmitter side, and a bank of photodiodes (PD) in the receiver side. The modulation is based on balanced MZ interferometers and so no wavelength tuning system is required.

### A. Bandwidth and area trade-off

The aggregate throughput proposed by the HBM solution reaches 1 TB/s by considering four HBM stacks per process unit. Each HBM is composed of 1024 channels with a data rate ( $DR$ ) of 2 Gbps, i.e., 256 GBps per HBM. One can show that the optimal  $DR$  for a short-range optical interconnect is around 10 to 20 Gbps [15]. If one SDM link, shown in Fig. 1(b), propagating 16 wavelengths, each across 8 channels, is used per HBM, this gives a total of 128 channels (i.e., 128 MZM and 128 photodiodes). As a result, the  $DR$  of 16 Gbps is enough to reach an aggregate bandwidth of 1 TB/s. This calculation enables the speed specification for the driver design to be set.

The transceiver module dimensions must not exceed the HBM footprint in order to be fully integrated in the HBM logic die. MZMs are the most area-constrained optical components. The surface of a lumped folded MZM was estimated to be 500

$\mu\text{m} \times 500 \mu\text{m}$ , resulting in a total surface of  $32 \text{ mm}^2$  for all 128 MZMs. Details about the area estimation are presented in Sec. IV. One can show that such a small form factor enables the optical chip to respect the HBM footprint constraint. This is a second specification for the driver design: the electrical chip footprint should be at most equal to the MZM area.

### B. Power consumption and performance trade-off

According to [13], the power efficiency of a HBM is estimated to be more than 35 GBps bandwidth per watt, corresponding to a 3.6 pJ/bit of energy consumption. Published optical solutions often exceed this value due to ER requirements. The optical link consumption should not exceed this value, and thus a low driving voltage combined with a low ER transmitter should be designed to target sub-pJ/bit energy.

The power consumption of the complete electro-optic link is derived by evaluating the consumption of each block: the laser, the transmitter, the receiver, and the serializer/deserializer (SerDes). This calculation is performed as a function of the MZM extinction ratio

$$ER = 10 \log \left( \frac{\cos^2 \left( \frac{-\Delta\phi + 90^\circ}{2} \right)}{\cos^2 \left( \frac{\Delta\phi + 90^\circ}{2} \right)} \right). \quad (1)$$

Considering PIC25G technology of STMicroelectronics [12], MZM phase shift  $\Delta\phi$  is given by  $18^\circ/\text{mm}$  for a  $V_{mod} = 2.5V_{pp}$  and thus a  $\Delta\phi = 6^\circ/V_{mod}$  is found with the modulator length ( $850\mu\text{m}$ ) being fixed due to footprint constraints. A  $ER$  versus  $V_{mod}$  relationship is thus found highlighting driver power consumption (depended to the driver swing) and MZM performance trade-off, as represented by the continuous grey line in Fig. 2.

The laser power consumption is determined from the optical power budget of the link, in such a way that the power received by the photodiode is enough to ensure a BER of  $10^{-12}$  (i.e.  $SNR = 14.07 \text{ dB}$ ). Considering [16] and [17], a receiver sensitivity of -20 dBm seems to be reachable on the transimpedance amplifier (TIA) at 16 Gbps. An ultra-low-noise TIA should be designed considering noise cancellation techniques [18] to achieve -20 dBm OMA at 20 Gbps. Global transmission losses in the channel are about 9 dB, being: propagation, MZM, and splitters losses of 3 dB; around 3 to 4 dB losses in the AWG; and from 2 to 3 dB due to coupling onto the chip. By considering ER ranging from 0.8 to 2.7 dB and 3 dB MZM insertion losses (operating at quadrature), the input channel power is derived. The comb-laser must provide as much optical power to supply 16 wavelengths across 8 channels. The laser wall-plug efficiency is estimated to be 10%, which results in the continuous blue bars in Fig. 2, representing the total power consumption in a HBM block. The smaller the ER, the higher the laser consumption to reach the desired receiver sensitivity.

The driver power consumption is determined from the classic energy formula  $E = \frac{1}{4} \frac{CV_{mod}^2}{\eta_{dr}}$  which estimates the dynamic consumption of a CMOS-inverter-based driver having an efficiency of  $\eta_{dr}$ . The driving amplitude  $V_{mod}$  depends on the CMOS technology and on the driver architecture.

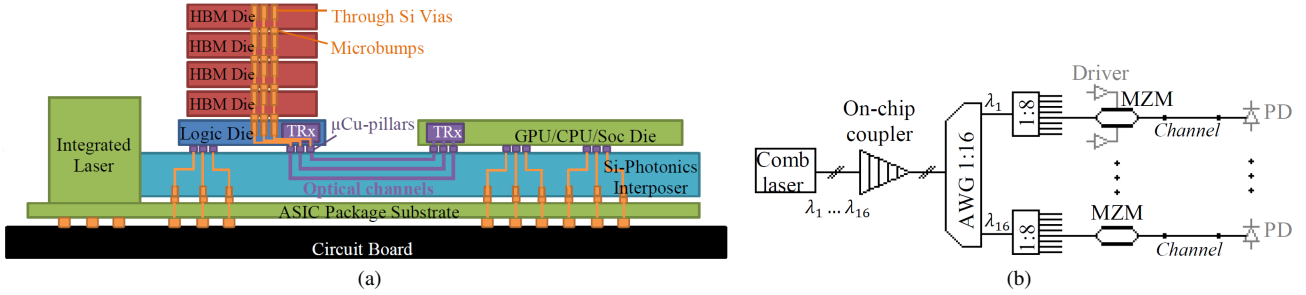


Fig. 1. Chip-to-chip optical interconnect architecture illustrated by: (a) a 3D assembly of CPU/GPU memory onto a silicon photonic interposer with optical interconnects; (b) a MZM-based SDM link using 16 wavelengths distributed on 16 resulting in an aggregate throughput of 2048 Gbps (i.e. 256 GBps).

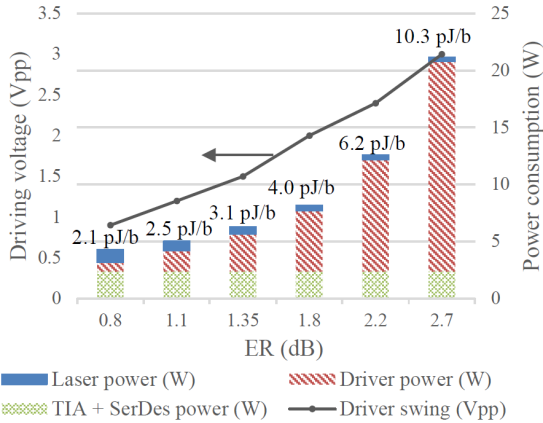


Fig. 2. Power consumption of 8x16 channels at 16 Gbps with respect to the MZM ER. The corresponding driving voltage is also plotted using the black line. Note that the laser consumption is relatively small. Values indicated on top of each bar are the total energy per bit consumption of the link.

Typically, a higher driver swing is obtained by using a level shifter to double the output voltage compared to the supply voltage [8]. The load capacitance  $C$  comprises the MZM and pad capacitance (roughly 300 fF for a 1-mm-long MZM and 100 fF for pads), and the driver parasitic capacitance, which depends on the technological node. The  $\eta_{dr}$  considers the driver complexity (pre-driver stages including level shifter) and is estimated around 30% to 40%. The derived energy consumption is consistent with values reported in the literature [5], [8], [19]. In an HBM block, there are 128 MZM and 2 drivers per modulator, resulting in the red hatched bars of total power consumption in Fig. 2, for a  $DR = 16$  Gbps. The receiver and SerDes power consumptions do not depend on the modulator ER. They are respectively estimated to be 300 mW (0.15 pJ/bit for TIA [20]) and 2 W (1 pJ/bit for SerDes [21]). They are represented by green dotted bars in Fig. 2.

The optical interconnect is optimized when a small ER is used for the modulator. Indeed, the driver consumption is largely predominant on laser consumption. This analysis enables a third transmitter specification to be established: a low driver output swing is required to ensure a low driver energy of approximately 1 pJ/bit. Designing an optical interconnect to perform HBM communications seems to be a viable solution. This implementation achieves at least equivalent performance

with respect to existing products, provided three conditions are satisfied: a high  $DR$ , low ER MZM, and extremely low power driver. Besides, the proposed optical system presents high flexibility for further optimization and performance improvement. To this end, the proposed 20 Gbps, sub-pJ/bit, low ER MZM-based transmitter is a first demonstration of a chip-to-chip application.

### III. HYBRID TRANSMITTER DESIGN

#### A. Lumped Mach-Zehnder modulator design

The dual-drive architecture of an MZM is depicted in Fig. 3. This configuration implements two high-speed phase modulators (HSPM), which are driven by complementary voltage signals and are responsible for output optical power modulation. Additionally, two PIN junction-based phase modulators (PINPM) are used to induce a constant phase shift of  $90^\circ$  between arms in order to place the MZM at its quadrature point. The modulation principle of HSPM devices is based on the variation of free carrier concentration. A PN diode is integrated into the waveguide. When reverse biased, the diode enters in carrier depletion mode. This expands the space charge region and changes the carrier concentration. This variation creates a change in the optical index of the material, which results in a phase shift of the light wave.

The modulator performance is designed through two main metrics. The optical modulation amplitude (OMA) is defined as the difference between the high (bit '1') and low (bit '0') levels of output power:  $OMA [mW] = P_{high} - P_{low}$ . The ER is defined as the ratio between the high and low levels of power:  $ER [dB] = 10 \log \left( \frac{P_{high}}{P_{low}} \right)$ . The ER is an intrinsic property of the modulator since it does not depend on the input power and varies as a function of the HSPM modulation efficiency.

The STMicroelectronics industrial photonic platform allows doping implants in waveguides bends [12]. To minimize the footprint, the MZM active region is folded into an S-bend along its length instead of having one long straight shape. Moreover, the MZM length is limited to 1 mm allowing the PN junctions to be considered as localized modulators. This avoids the use of more complicated architectures such as traveling-wave MZMs [9] or multistage MZMs [8].

The MZM layout is illustrated in Fig. 4(a) with 0.6 mm-long active sections. A bump matrix with 100  $\mu$ m pitch is

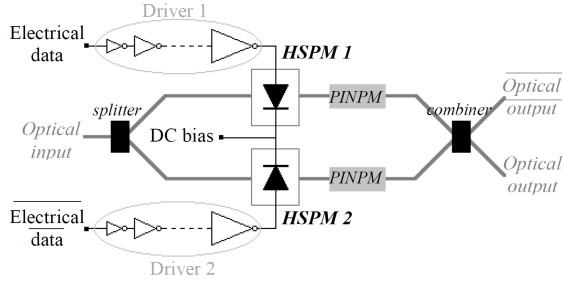


Fig. 3. Dual-drive architecture of MZM. Both drivers are identical and constituted by  $N$  inverter stages. A DC voltage enables to bias the PN junctions in reverse and weakly forward modes.

superimposed onto the photonic integrated circuit (PIC) to perform connections with the electrical die. The MZM occupies a surface area of  $500 \mu\text{m} \times 500 \mu\text{m}$ , which is compatible with the dimensions of the related electrical components (drivers, TIA). Such a small form factor is of great interest for chip-to-chip optical interconnects, as optical I/Os should be of a similar size to a CPU to memory link. Also, electrical crosstalk between transmission lines can be attenuated.

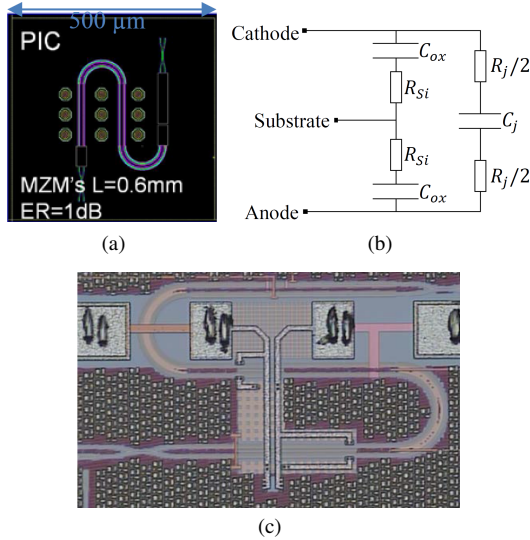


Fig. 4. Lumped MZM with active bends to minimize PIC footprint: (a) layout projection with copper pillar matrix, (b) circuit model of a HSPM and (c) microphotography of the test structure.

## B. MZM Modeling

MZM modeling is an important asset for a hybrid transmitter design. Such expertise is found from STMicroelectronics industrial photonic platform documentation. The main equations describing the MZM operation are given below based on [22]. MZM modeling were used to perform electro-optical co-simulations of the transmitter. Expressions based on experimental measurement are thus preferred in this work rather than analytical equations.

The free carrier variation  $\delta N$  in the PN junction is linked to the HSPM capacitance according to

$$\delta N = -\frac{1}{q} \frac{C_{j0} V_{bi}}{1 - MJ} \left(1 - \frac{V_{mod}}{V_{bi}}\right)^{1-MJ}, \quad \text{where} \quad (2)$$

- $q = 1.6 \cdot 10^{-19} \text{ C}$  is the electric charge;
- $C_{j0} = 295 \text{ fF/mm}$  is the HSPM junction capacitance at 0 V bias;
- $V_{bi} = 0.58 \text{ V}$  is the built-in potential;
- $MJ = 0.25$  is a coefficient specific to the PN diode;
- $V_{mod}$  is the voltage applied on the HSPM.

Numerical values of the parameters  $C_{j0}$ ,  $V_{bi}$ , and  $MJ$  were fitted using HSPM measurements (see Sec. IV) to accurately reproduce the optical behavior of the phase modulators. From electrons ( $\delta N_e$ ) and holes ( $\delta N_h$ ) concentration variations, the induced change in optical index ( $\delta n$ ) at an optical wavelength of 1310 nm is derived according to Soref's equations [23], as

$$\delta n = -\text{sign}(\delta N) \left(2.98 \cdot 10^{-22} \cdot \delta N_e^{1.016} + 1.25 \cdot 10^{-18} \cdot \delta N_h^{0.835}\right). \quad (3)$$

A refractive index change leads to an optical phase variation of

$$\delta \phi = \frac{2\pi \delta n}{\lambda} L_{HSPM} \text{corr}_\phi, \quad \text{where} \quad (4)$$

- $\lambda = 1310 \text{ nm}$  is the optical wavelength;
- $L_{HSPM} = 850 \mu\text{m}$  is the HSPM length;
- $\text{corr}_\phi = 0.6$  is a parameter for HSPM fitting.

The HSPM phase shift ( $\Delta \phi$ ) in degrees is then calculated by considering the difference between the phase variation under  $V_{mod}$  bias ( $\delta \phi_{V_{mod}}$ ) and 0 V bias ( $\delta \phi_0$ ) as

$$\Delta \phi = \frac{180}{\pi} (\delta \phi_{V_{mod}} - \delta \phi_0). \quad (5)$$

The MZM converts the HSPM phase shifts into optical output power variation, according to the relation

$$P_{out} = \text{loss} \cdot P_{in} \cdot \cos^2 \left( \frac{\Delta \phi_{HSPM1} - \Delta \phi_{HSPM2} + 90^\circ}{2} \right), \quad \text{where} \quad (6)$$

- $\text{loss} = 0.76$  is a factor that considers the optical losses due to directional couplers, HSPMs, PINPMs, and propagation;
- $P_{in}$  is the optical input power;
- $90^\circ$  is the phase shift between MZ arms.

In addition to the static behavior model described from (2) to (6), an electrical model of the HSPM is required to consider the dynamic performance of the PN diode. The HSPM circuit is illustrated in Fig. 4(b), where  $C_j$  and  $R_j$  are the junction capacitance and resistance,  $C_{ox}$  is the oxide capacitance, and  $R_{Si}$  is the substrate resistance. The junction capacitance is a function of voltage bias according to

$$C_j (\text{fF/mm}) = \frac{C_{j0}}{\left(1 - \frac{V_{mod}}{V_{bi}}\right)^{MJ}}. \quad (7)$$

A microscope image of a lumped, folded MZM is illustrated in Fig. 4(c). Model parameters obtained from measurements are:  $C_{j0} = 295 \text{ fF/mm}$ ,  $R_j = 11.5 \Omega\text{-mm}$ ,  $C_{ox} = 46 \text{ fF/mm}$ , and  $R_{Si} = 5k\Omega\text{-mm}$  [22]. MZM measurements are detailed in Subsec. IV-A.

### C. Driver circuit design

The purpose of the driver is to shape input signals and to drive the capacitive modulator load. The driver plays the role of a buffer to adapt the input signal to the logical effort required by the MZM. Therefore, the architecture of the driver is based on an inverter chain known for its low power consumption. Two identical circuits are used to drive both HSPM anodes in a dual-drive MZM, as illustrated in Fig. 3. A common DC voltage source applies a bias to the HSPM cathodes in order to ensure a depletion mode of the PN diodes.

The design methodology proposed in [24] is applied here to find both the ideal number  $N$  of inverter stages and the transistors sizes of the driver. Such methodology is built on the logical effort method. There, the propagation delay is minimized when each stage in the path bears the same stage effort. In the case of an inverter chain, the stage effort also corresponds to the ratio between the inverter sizes. As a result, electrical data signals propagate through  $N$  consecutive CMOS inverters with transistor sizes increased by a constant factor. The proposed circuit provides signal amplification up to full-swing CMOS level to drive the HSPM load.

According to [24], the driver optimization leads to a trade-off between speed, energy efficiency, and area. To highlight these relationships, equations are presented hereafter to estimate the  $DR$  limitation and power consumption from the inverter sizes. The  $DR$  is limited by the inverter rise and fall rates, i.e., the slew-rate constraint. Consequently, the  $DR$  limitation comes to

$$DR = \frac{J_{D,n} W_{n,N}}{2 \cdot V_{dd} (C_{mod} + C_p W_{n,N} (1 + \beta))}, \text{ where} \quad (8)$$

- $J_{D,n}$  is the current density of NMOS transistors;
- $W_{n,N}$  is the NMOS transistor width of the last stage;
- $V_{dd}$  is the voltage source;
- $C_{mod}$  is the MZM load;
- $C_p$  is the parasitic capacitance per transistor width considering gate-drain and drain-body capacitances;
- $\beta$  is the ratio between the PMOS and NMOS transistor widths required for equal rising and falling time.

Similarly, the energy consumption is estimated by

$$E_{avg} = \frac{1}{4} \left( C_{mod} + C_p (1 + \beta) \sum_{i=1}^N W_{n,i} \right) V_{DD}^2, \quad (9)$$

considering the sum of the modulator and driver parasitic capacitance [24]. From experimental data, one may define  $E_{avg} = P_{avg}/DR$  using the average power consumption.

Figure 5 illustrates the trade-off between the energy efficiency, from (9), in pJ/bit with respect to the  $DR$ , from (8), in Gbps for different CMOS technologies. Table I highlights the different CMOS technologies from which optimization is performed. One may conclude the compromise between the speed and the energy consumption, i.e. a restrained  $DR$  is preferred to ensure moderate power consumption. However, driver performance can be improved by choosing a more advanced technological node. Advanced technological nodes are capable of higher speed and efficiency but at the detriment of higher process complexity and cost.

The driver optimization depicted in Fig. 5, enables the designer to choose the most suitable technology for the proposed application. With respects to the targeted driver's specifications, i.e., a 300 fF modulator load,  $DR = 20$  Gbps, and sub-pJ/bit consumption, 55-nm CMOS technology from ST is chosen. By applying the design methodology described in [24], the driver is designed with four inverter stages of increasing dimensions. The ratio between the inverter sizes is set to 2.3 and the widths of the last NMOS and PMOS transistors are 39 and 78  $\mu\text{m}$ , respectively. Schematic and layout details are developed in Subsec. IV-C.

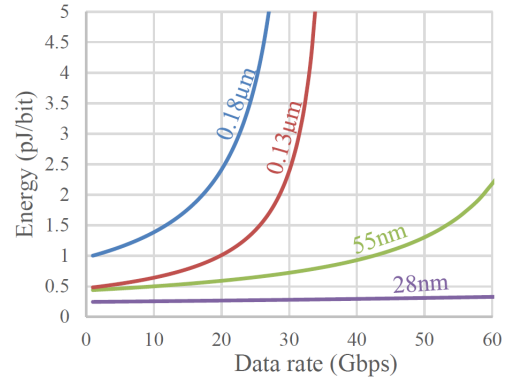


Fig. 5. Driver design optimization: the trade-off between the energy efficiency with respect to the  $DR$  for different CMOS technologies presented in Table I.

TABLE I  
CMOS TECHNOLOGIES USED FOR THE DRIVER OPTIMIZATION  
( $C_{mod} = 300$  fF).

	XFAB SOI 180 nm	ST BiCMOS 130 nm	ST BiCMOS 55 nm	ST FDSOI 28 nm
$V_{dd}$ (V)	1.8	1.25	1.2	0.9
$J_{D,n}$ (mA/ $\mu\text{m}$ )	0.38	0.42	0.42	0.56
$C_p$ (fF/ $\mu\text{m}$ )	0.9	1.5	0.78	0.44
$\beta$ (V)	2.5	2	2	2

## IV. HYBRID TRANSMITTER DEMONSTRATOR RESULTS

### A. Mach-Zehnder modulator measurements

The MZM is designed using the second generation PIC25G ST technology on 300 nm SOI wafers. MZM microscope image is illustrated in Fig. 4(c). The HSPM length is 850  $\mu\text{m}$ , its phase shift at 2.5 V reverse bias is 18  $^\circ/\text{mm}$  for losses of 0.6 dB/mm [25]. High-speed measurements were performed using a Keysight BERT M9505A for pattern generation together with a Keysight DCA-X 86100D sampling oscilloscope for optical eye diagram inspection. A continuous light wave at 1310 nm is injected in the MZM with a laser output power of 12 dBm (16 mW). Complementary electrical patterns are amplified and added to a DC bias through a bias tee to drive both HSPMs at the desired operating point. Measurements have been performed at 15 Gb/s using two  $2^7 - 1$  non-return-to-zero (NRZ) pseudo random bit sequences (PRBS). No pre-emphasis signal was used.

The MZM eye diagram is shown in Fig. 6(a) with a 1.2 V<sub>pp</sub> driving voltage applied on each HSPM, under -2 V bias. An ER of 1 dB and an OMA of -10.5 dBm (90 μW) on the DCA's photodiode (PD) were achieved. As expected, the ER is very small since a low modulation voltage was used and the HSPMs are very short. However, no signal processing is required to obtain these results. These results confirm that data transmission based on short MZM is possible despite the low ER, validating their potential for future chip-to-chip communications.

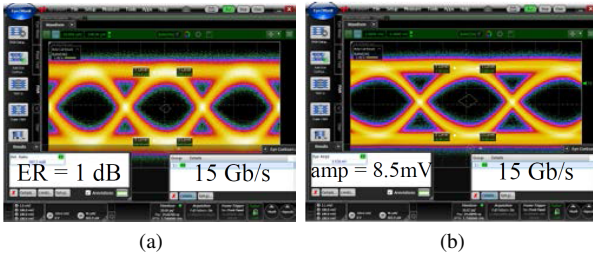


Fig. 6. MZM eye diagrams performed with same experimental conditions (1.2 V<sub>pp</sub>, -2 V bias) at 15 Gb/s: (a) optical output measured with DCA's PD ( $P_{high} = 429 \mu\text{W}$ ,  $P_{low} = 341 \mu\text{W}$ ), (b) electrical output coming from integrated PD.

To circumvent the DCA's PD limitations in terms of noise, a second MZM structure is implemented. It integrates the PD on the PIC to perform an electrical measurement of the PD current. This MZM test structure implements a Y-junction at the MZM output which splits the power in two branches: the first one is dedicated to electrical measurement and results of integrated PD are depicted in Fig. 6(b). One can note the improvement of the signal to noise ratio with respect to the electrical measurement. Thanks to the integration of the opto-electrical conversion, the average optical power incident on the PD can be reduced while maintaining an open eye diagram since the oscilloscope is more sensitive in electrical domain.

The MZM test structure enables the evaluation of BER curves which are reported in Fig. 7. BER curves are plotted with respect to the integrated PD sensitivity, i.e. the optical modulation amplitude received on the PD. Measurements have been performed with two driving voltage amplitudes leading to a MZM ER of 1 dB or 3 dB. For a  $10^{-9}$  BER, an additional transmitter penalty of 3 dB should be taken into account to compensate the low ER. Nevertheless, these curves demonstrate that error free communication with a 1 dB ER is possible. To the best of authors' knowledge, the BER for an ER as low as 1 dB is reported for the first time in the literature.

### B. Comparison of MZM reverse and a weak forward bias

Another improvement to the MZM performance comes from applying a weak forward bias to the PN junction. Indeed, the equations that govern HSPM modulation show that the PN junction remains in depletion mode if the driving voltage is below the built-in potential. This built-in potential is around 0.5 V to 0.7 V, depending on the junction doping. Therefore, biasing the HSPM with a small forward voltage does

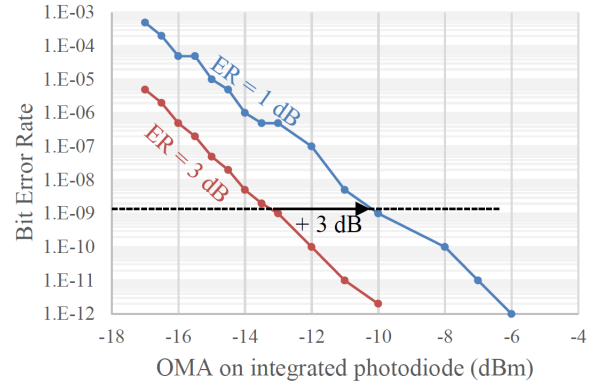


Fig. 7. BER with respect to output OMA for ER = 1 dB (blue curve) and ER = 3 dB (red curve).

not impede its operation by a longer carrier recombination time. Moreover, this operating mode benefits from a better modulation efficiency, which is very interesting in the case of lumped short devices.

Figure 8 compares a reverse and a weak forward biased MZM, similar to the one described in the previous section. Measurements have been performed optically (without the integrated PD) at 15 Gb/s with a 1 V<sub>pp</sub> driving voltage in both instances. When a -2 V bias is applied (see Fig. 8(a)), each HSPM is operating over the range [-2.5; -1.5] V resulting in an ER of 0.75 dB. When a 0 V bias is applied (see Fig. 8(b)), each HSPM is operating over the range [-0.5; +0.5] V resulting in an ER of 1 dB. The same modulation efficiency is achieved here (with a weak forward bias) as indicated by the eye diagram in Fig. 6(a) performed at 1.2 V<sub>pp</sub> and -2 V bias. Thus, the weak forward bias mode favors a transmitter power consumption reduction, which is proportional to the square of the driving voltage.

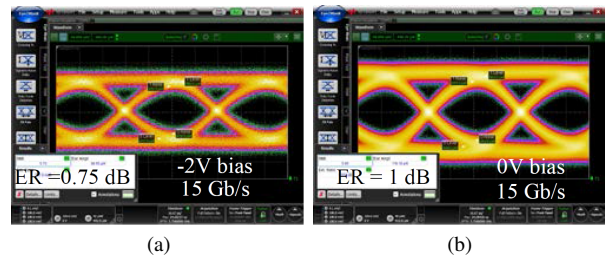


Fig. 8. MZM eye diagram with: (a) 1 V<sub>pp</sub> biased at -2 V ( $P_{high} = 560 \mu\text{W}$ ,  $P_{low} = 470 \mu\text{W}$ ), and (b) 1 V<sub>pp</sub> biased at 0 V ( $P_{high} = 563 \mu\text{W}$ ,  $P_{low} = 444 \mu\text{W}$ ).

### C. High-speed low-power driver measurements

The driver test structure was fabricated using STMicroelectronics BiCMOS 55 nm technology. A die microphotograph is illustrated in Fig. 9(a) having a die area of  $356 \mu\text{m} \times 509 \mu\text{m}$ . The driver itself has an area of  $5.3 \mu\text{m} \times 18.6 \mu\text{m}$  and sizing details (transistor widths and lengths) are presented in Fig. 9(b). A 100 pF MIM decoupling capacitance ( $C_{dec}$ ) is added in the driver schematic (see Fig. 9(b)), filling all available space between pads.

The experimental setup, illustrated in Fig. 9(c), uses a Keysight BERT M9505A for pattern generation and error detection, together with a Keysight DCA-X 86100D sampling oscilloscope for eye diagram inspection. The digital communication analyzer (DCA) makes use of remote heads to avoid back reflections at the output port. Measurements have been performed using  $2^7 - 1$  NRZ PRBS7. Being DC-coupled, DCA 50  $\Omega$  internal load leads to a reduction of the output modulation amplitude due to a voltage divider bridge. However, power measurement is achieved without any external load and is only representative of the driver. Experimental results are presented and compared to simulations carried out using Keysight ADS software. Simulation circuitry, shown in Fig. 9(b), reproduces in the best way the experimental conditions and are used for optical-electrical co-simulations in Subsec. IV-E. To enable accurate comparison, simulations consider the BER tester, the DCA modeled by a filter and a 50  $\Omega$  resistive output load, and the connection losses due to probes and RF cables.

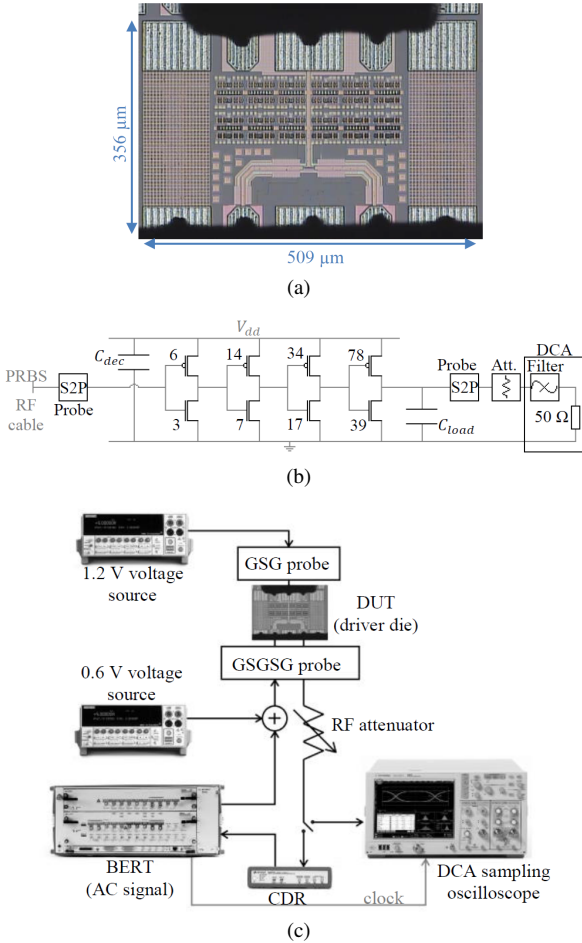


Fig. 9. High-speed low-power driver: (a) die microphotograph of the driver test structure, (b) simulation setup and transistors' sizing ( $W$  in  $\mu\text{m}$  and  $L = 55$  nm), and (c) measurement setup using a clock data recovery (CDR) for BER measurements (see Fig. 11).

Figure 10 shows the measured eye diagrams (red curves) on which simulated eye diagrams (blue curves) have been superimposed. Figure 10(a) results are for a  $DR = 20$  Gbps.

To reduce adverse effects of noise caused by external cables and probes, de-emphasis of 7 dB loss is included in the Fig. 10(b) experiment, which is performed at the same  $DR$ . Fig. 10(c) shows results for a  $DR = 25$  Gbps with input signals de-emphasized with a 9 dB loss. At this frequency, the driver speed limitation is reached, and de-emphasis is unavoidable. The experiment in Fig. 10(d) is the most accurate for the working conditions of hybrid demonstrator. Indeed, it includes an integrated 300 fF load ( $C_{mod}$  in in Subsec. III-C). Results are shown for a  $DR = 20$  Gbps, and 6 dB loss de-emphasis. Regarding simulations, a 100 fF pads capacitance ( $C_{pad}$ ) is used from Fig. 10(a) to 10(c), and a 400 fF load is used in Fig. 10(d) considering  $C_{pad}$  and  $C_{mod}$  ( $C_{load} = C_{pad} + C_{mod}$  in Fig. 9(b)). The eye opening is very clean, and good agreement can be noticed between the simulation and measurement results for all driver working environments. Furthermore, eye diagrams have asymmetrical crossings due to the mismatch between falling and rising times. However, this will not impact the transmitter operation thanks to the dual-drive architecture.

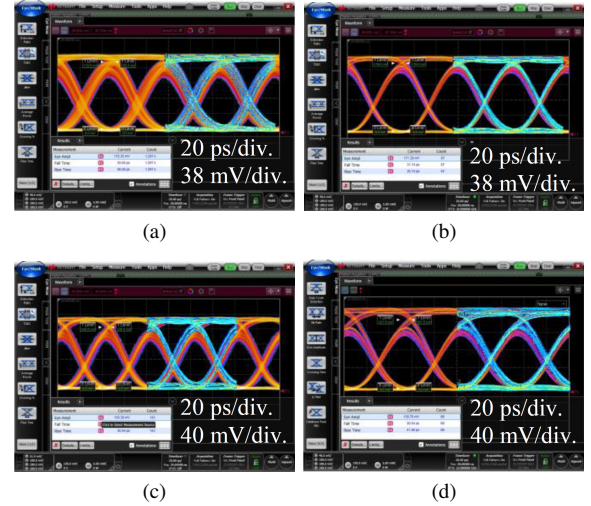


Fig. 10. Measured (red curves) and simulated (blue curves) eye diagrams for different driver working conditions: (a) 20 Gb/s, no emphasis is used with  $C_{load} = C_{pad} = 100$  fF; (b) 20 Gb/s, de-emphasis is set to 7 dB loss; (c) 25 Gb/s, de-emphasis is set to 9 dB loss; and (d) 20 Gb/s, de-emphasis is set to 6 dB loss with  $C_{load} = C_{pad} + C_{mod} = 400$  fF.

The energy consumption and the BER achieved by the driver without de-emphasis are highlighted in Fig. 11 for different  $V_{dd}$  values. The power consumption of the driver has been measured at different  $DR$  and supply-voltage levels. Based on these measurements, the energy efficiency has been calculated and is illustrated in Fig. 11(a) (blue curves). The simulated energy consumption is also plotted in red curves for comparison. At  $DR \geq 15$  Gbps, the energy consumption is reduced because the output driver signal is progressively degraded and cannot reach the desired voltage swing anymore. This is confirmed by the BER curves in Fig. 11(b), where an error-free transmission ( $BER < 10^{-12}$ ) is observed up to a maximum  $DR$ , depending on  $V_{dd}$  value. One can note that the error-free limit under regular operating conditions ( $V_{dd} = 1.2$  V,  $2^7 - 1$  PRBS input signal, room temperature) is 20 Gbps (see continuous line in Fig. 11(b)).



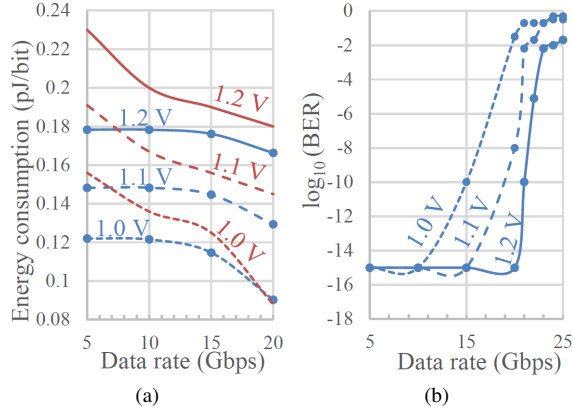


Fig. 11. Driver performance with respect to supply voltage  $V_{dd}$ , being: (a) Energy efficiency and (b) BER. Measurement results are in blue whereas simulation results are in red.

Table II shows an overview of the proposed driver performance, and a comparison with the state-of-the-art. This work achieves one of the best energy efficiency at comparable  $DR$  as presented in [19]. In addition, the design optimization, described in Subsec. III-C, predicts the trends highlighted in [19] and enables here a maximum load of 400 fF required for a MZM driver.

#### D. Hybrid transmitter integration on a board

Hybrid integration is an attractive solution to assemble photonic and electronic chips since it benefits from separate optimization of both integrated circuits and it leads to better performance than monolithic integration. A short-range optical interconnect based on a photonic interposer is often implemented using 3D flip-chip method (see Fig 1(a)). However, this work prefers a wire-bonding board integration due to its simplicity and a reduced fabrication time. Main objectives are to validate the operation of a low-ER transmitter and to track co-integration difficulties for the future 3D assembly.

Figure 12(a) shows a microphotograph of the hybrid transmitter demonstrator, including two proposed driver test structures (see Fig 9(a)) and the optical integrated MZM (see Fig 4(c)). Both circuits are integrated onto a board. A fiber-array is glued on top of the optical circuit, as depicted in the inset, to provide input light and to collect output light. Wire-bonding is used to connect driver I/Os, voltage supplies, and phase shifters bias, either to the HSPM electrodes or to board pads.

#### E. Hybrid transmitter results

Co-simulations are performed using Keysight ADS software. Two complementary bit patterns are fed to the drivers, one for each MZM arm. The HSPM small-signal circuit, shown in Fig. 4(b), is used as the driver load. For an 850  $\mu\text{m}$ -long HSPM, the junction capacitance is 250 fF at 0 V bias. Figure 12(b) illustrates the co-simulation setup. Similarly presented in Fig. 9(b), the setup takes into account the BER tester, connections losses (probes, RF cables, and bond wires)

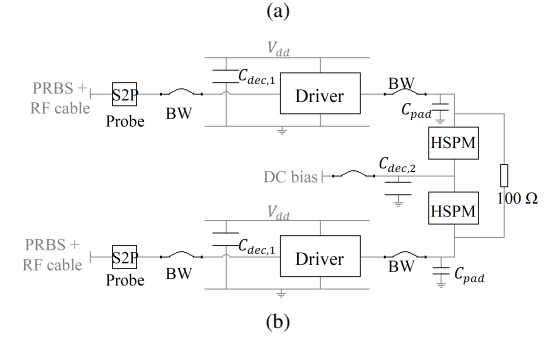
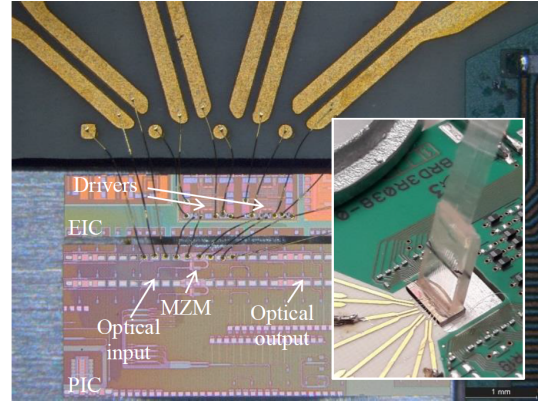


Fig. 12. Hybrid transmitter integration: (a) wire-bonding assembly microphotograph, and (b) co-simulation schematic.

and the MZM termination resistance. Electrical transient simulations result in waveforms of the modulation voltage across the HSPMs. Then, a post-treatment is achieved from (2) to (6) in order to model the optical behavior of the MZM, which comes to the optical output power eye diagrams.

Co-simulations have shown that the bonding wires between drivers and HSPMs induce back reflections towards the bit pattern generator. The MZ demonstrator includes a 100  $\Omega$  resistance to end the transmission lines. This terminated resistor results in lower modulation amplitude than theoretical results, which would not include wires and resistance. Moreover, power dissipation is not only the modulator power consumption since it also comprises dissipated power into the resistance load.

Figure 13 highlights the optical eye diagram at 20 Gbps for the hybrid transmitter. In Fig. 13(a), co-simulations are performed using a  $2^7 - 1$  PRBS signal at the driver inputs, DC bias of 0.7 V, and optical input power of 5 dBm (i.e. 3.2 mW). The eye opening is well symmetric, owing to the dual-drive MZM architecture. The output ER is estimated to be 0.76 dB, which corresponds to an OMA of -6.7 dBm (i.e. 213  $\mu\text{W}$ ). The average power consumption is evaluated to 13.3 mW at 20 Gbps, leading to  $E_{avg} = 0.66$  pJ/bit.

Measurement was performed applying the same experimental conditions of the simulated results. A measured  $ER = 0.66$  dB is achieved at 20 Gbps and 0.7 V DC bias. The power consumption is 18 mW, leading to  $E_{avg} = 0.9$  pJ/bit. These slight differences compared to the co-simulations could be the result of model approximations in the simulation environment. Some imprecisions in the simulation can take place in the

TABLE II  
DRIVER PERFORMANCE COMPARISON.

Ref.	This work	[5]	[4]	[8]	[10]	[19]	[6]
Techn.	55 nm BiCMOS	130 nm SOI	40 nm CMOS	65 nm CMOS	65 nm CMOS	32 nm SOI	28-nm CMOS
$DR$ (Gbps)	20	25	20	25	25	25	28
Energy (pJ/bit)	0.18	0.68	1.3	1.83	1.6	0.19	2.08
Max. load (fF)	100	28	NA	150	105	NA	NA
Output swing ( $V_{pp}$ )	1.2	2.4	1.95	2.5	4.8 (diff)	1	2
$V_{dd}$ (V)	1.2	$\pm 1.2$	1.3	1.25& 2.5	1.2& 2.4	1	1

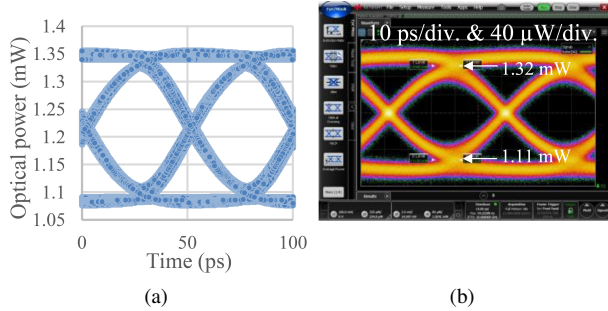


Fig. 13. Optical eye diagram at 20 Gbps:(a) co-simulation, having  $V_{bias} = 0.7$  V and  $ER = 0.76$  dB; and (b) measurement results, having  $V_{bias} = 0.5$  V and  $ER = 0.73$  dB.

blocks shown in Fig. 12(b) modeling RF connections, bond wires or, eventually bond pads. Another explanation of those degradations could be a leakage current during the measurement. Both hypotheses are under investigation but are out of the scope of this paper. The ER can be improved up to 0.84 dB by varying the DC bias. A comparable result of Fig. 13(a) is presented in Fig. 13(b), where it shows the eye diagram at 20 Gbps for  $V_{bias} = 0.5$  V and  $ER = 0.73$  dB.

Table III compares the proposed hybrid optical transmitter with published MZ-based transmitters. Applications targeted by papers in Table III are related to long-reach data-center communications. Thus, different figures of merit, in terms of  $DR$  and  $ER$ , are presented; resulting in larger modulators and much more complex driver design. When high- $ER$  applications are addressed, a higher energy consumption is found. Owing to its electronic driver's simplicity, this work reaches the best energy efficiency, but this is at the detriment of a reduced  $ER$ . In the best of our knowledge, this is the first work dealing with MZM-based transmitters for chip-to-chip applications and unfortunately a more relevant comparison is not available.

## V. CONCLUSIONS

Silicon photonics is considered as a prime technology for HPC applications. This paper proposed a co-optimization framework for short range HPC applications never presented before. This framework includes the following specifications:

low energy consumption compatible with chip-to-chip applications and mature technology-based devices intended for short term industrialization. For this reason, PIC25G is considered to fabricate a transmitter operating at 20 Gbps and  $ER = 0.73$  dB. Transmitter architecture is based on a dual-drive 850  $\mu\text{m}$ -long Mach-Zehnder interferometer, and low-power inverter chain topology in 55-nm technology to achieve 0.9 pJ/bit driver energy consumption. To the best of authors' knowledge, a  $BER < 10^{-12}$  is obtained for an ER as low as 0.73 dB is reported for the first time in the literature.

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TABLE III  
PERFORMANCE COMPARISON OF HYBRID MZ-BASED TRANSMITTER.

Ref.	This work	[8]	[9]	[11]	[6]
Integ.	Wire-bonding	Flip-chip	Flip-chip	Wire-bonding	Flip-chip
MZM length	1-seg. 850 $\mu\text{m}$	6-seg. 3 mm	TW* 3.15 mm	3-seg. 3 mm	2-seg. 500 $\mu\text{m}$
Load (fF)	250	150	950	300	1360
ER (dB)	0.73	4 to 6	2.5	6.1	3.6
Driver type	inv. chain	level shifter +stacked inv.	ECL <sup>†</sup> -pair stages	level shifter +cascode inv.	CML+inv. chain
Techn.	55 nm BiCMOS	65 nm CMOS	55 nm BiCMOS	130 nm CMOS	28 nm CMOS
Output swing	1.2 V <sub>pp</sub> (2.4 V <sub>diff</sub> )	2.5 V <sub>pp</sub>	1.6 V <sub>pp</sub>	2 V <sub>pp</sub> (4 V <sub>diff</sub> )	2 V <sub>pp</sub>
DR (Gbps)	20	25	56	20	28
$E_{avg}$ (pJ/bit)	0.9 <sup>§</sup>	11	5.4	14.5	2.08

\* Traveling wave (TW); <sup>†</sup> emitter-coupled logic (ECL); <sup>§</sup> comprises the 100  $\Omega$  load dissipation

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transistors aging simulation and modeling.

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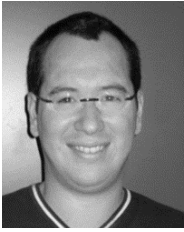


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From 1995 to 1997, he was an Assistant Professor in University of Lille engaged in frequency domain numerical techniques for 3-D electromagnetic simulations. In 1997, he joined STMicroelectronics, Central R&D, Crolles, France. He developed electromagnetic simulations activity for passive components and interconnections for RF, analog, and digital applications on silicon. In 2002, he moved to RF design with MEMS, especially with bulk acoustic wave resonators. In 2005, he was with the Passive and RF-MEMS Above IC group, and he managed a group on filtering with BAW resonators, including modeling, RF characterization, and filter designs. In 2010, he joined R&D process development group as team manager to develop integration of heterogeneous systems on silicon interposers, with special interest on 60 GHz module with beamforming in WiGig context to provide Gbit/s data transfer. Since 2012, he has been engaged in a new More than Moore activity inside STMicroelectronics relative to photonics. He was in charge of test chips specification, design, and characterization to qualify the technology.



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