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Abstract

We perform the growth of GaAs epilayers by molecular beam epitaxy (MBE) on Ge pseudo-substrates obtained by the Aluminium Induced Crystallisation (AIC) of thin amorphous Ge layers deposited on silica. Despite the apparent uniformity of the AIC-Ge layer, large domains (more than 50 μm wide) previously thought to be monocrystalline are found to actually consist in smaller grains (500 to 1000 nm wide), separated by low angle grain boundaries. These defects are transferred during epitaxy to the GaAs layer and degrade the quality of the III-V material. In our growth conditions, the MBE results in the selective deposition of thin GaAs layers on Ge with respect to the silica support, but selectivity is progressively lost with increasing layer thickness.

Keywords:
Metal Induced Crystallization, ALILE, Germanium, Aluminium, Gallium Arsenide, Molecular Beam Epitaxy

1. Introduction

Metal induced crystallization (MIC) is a promising technique for the fabrication of crystalline Si or Ge layers on low cost supports. Depending on the nature of the metal, the crystallization of amorphous Ge can occur at very low temperatures, down to 177°C for Au or 211°C for Al, below the respective eutectic temperature of the binary mixtures (Ge-Al 420°C, Ge-Au 361°C)[1, 2, 3]. The aluminium-induced crystallization (AIC) of Ge has attracted much interest due to the peculiar layer inversion process (ALILE) during the crystallization[4]. The low cost of the ALILE technique has primarily prompted solar applications[5, 6, 7, 8], although there have been other outcomes such as transistors[9, 10].

Interestingly, the control of the diffusion of Ge in the metal can lead to the crystallization of oriented grains with normals mainly along the [111] or [100] directions, depending on the nature of diffusion barrier and substrate[11, 12, 13, 14, 15, 16, 17]. The fabrication of flat oriented crystals with large grains (wider than 50μm) is interesting and can compete with other approaches such as localized liquid phase crystallization[18] or laser annealing[19, 20].

Yet, the use of MIC layers as oriented crystalline pseudo-substrates for subsequent epitaxy has been rather limited. Thin MIC-Si or MIC-Ge layers on silica have been used as substrates for the growth of GaAs[21, 22] or Ge[23] nanowires, but nanostructures with small footprints are not very demanding in terms of substrate crystallinity[24]. In an attempt to reduce defect density present in the MIC-Ge layer, Toko *et al.* performed the homoepitaxy of planar Ge layers on MIC-Ge pseudo-substrates by molecular beam epitaxy[15] (MBE). Due to the good lattice match between Ge and GaAs (lattice parameters GaAs 5.653Å, Ge 5.658Å), the direct epitaxy of GaAs on such low-cost Ge layers is a promising route for the fabrication of cheaper III-V devices and solar cells. Comparable approaches have already been investigated in the literature, with GaAs solar cells grown on large-grain poly-Ge[25, 26] or Ge buffer on Si(100)[27]. Recently, work by Toko *et al.* has shown a promising photoresponse from GaAs epilayers grown by MBE on MIC-Ge pseudo-substrates[28].

Yet the quality of MIC-Ge pseudo-substrates, which

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consist in wide 'monocrystalline' domains[13, 15, 28], remains lower than commercial mono-crystalline Ge wafers. In particular no study has looked in details at the microstructure of the so-called 'mono-crystalline' MIC-Ge domains and how it affects the subsequent GaAs epitaxy.

2. Materials and methods

We use here a fabrication procedure similar to that of Toko *et al.*[28]. A simplified scheme is presented Fig. 1 and highlights the two main steps: the fabrication of the MIC-Ge pseudo-substrates (Fig. 1.a) and the epitaxy of the GaAs epilayers (Fig. 1.b).

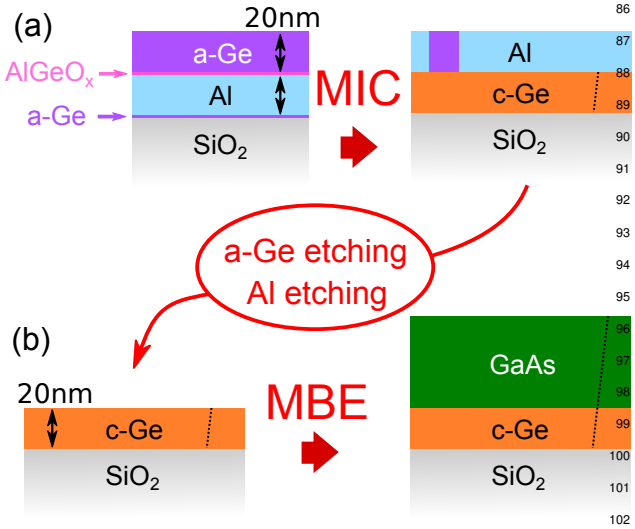

Figure 1: Simplified processing scheme of the samples. (a) Fabrication by MIC (ALILE) of the crystalline (c-Ge) pseudo-substrates starting from 20 nm thick amorphous Ge (a-Ge) and aluminium layers deposited on silica. (b) Growth of GaAs on the Ge pseudo-substrates by molecular beam epitaxy (MBE).

The MIC-Ge pseudo-substrates are fabricated as follows. First, we form a 70 nm thick silica layer on standard Si(100) 2" wafers (Siltronix) by dry oxidation at 1050°C for 15 min, which acts as a virtual amorphous silica substrate for the rest of the process. Samples fabricated from such oxidized Si wafers can be easily cleaved to fit the various equipments used in this study. Then, we deposit the Al and Ge layers by e-beam evaporation using a Plassys MEB550SL, as detailed in our previous work[29].

Before crystallization, the MIC-Ge sample consists in a 1.0 nm Ge underlayer[30], followed by 20 nm of Al and a 1.0 nm thick Ge layer which is exposed to air (for 10 min) to form a $AlGeO_x$ diffusion barrier[31, 32], and a final 20 nm thick Ge top layer. The MIC is performed in a programmable hot plate (Harry Gestigkeit) flushed with nitrogen gas by heating the sample at 270-300 °C during 15 to 20 h. After the annealing, the remaining amorphous Ge is selectively removed using reactive ion etching (CCP/RIE Nextral NE100, using O_2 and SF_6 for 4 min)[33]. Then the top Al layer is removed chemically using H_3PO_4 at 100°C during approximately 60 s. The change of the surface reflectivity, from the bright Al layer to the darker crystalline Ge material (c-Ge), is used to control the wet etch duration.

Before introduction in the Molecular Beam Epitaxy (MBE) chamber (RIBER 32) the MIC-Ge pseudo-substrates are further cleaned using H_2O_2 (30 s) and HF 1% (30 s) treatments, with intermediate rinse in deionized water. The MIC-Ge substrates are then outgassed at 400°C in a dedicated ultra high vacuum chamber, before transfer to the main growth chamber (base pressure 1.0 10^{-10} Torrs). The GaAs epitaxy is performed using parameters previously optimized for the twin-free epitaxy of GaAs(111) on Ge(111) monocrystalline wafers[34].

Here, gallium is provided by a standard effusion cell, while arsenic is delivered by a valved cracker cell (RIBER VAC500) producing As_4 tetramers (cracker temperature 600°C). The Ga beam equivalent pressure (BEP) is set to 1.5 10^{-7} Torrs, corresponding to a growth rate of ~1.5 Å.s^{-1} on GaAs (100). The ratio of arsenic to gallium (BEP_{As_4} : BEP_{Ga}) is approximately 60:1. The substrate temperature is 625-635°C, as measured by thermocouple and optical pyrometry, during all the growth procedure.

The samples are characterized before and after growth using Scanning Electron Microscopy (SEM, FEI Magellan). The local crystalline orientation is measured using Electron Backscatter Diffraction (EBSD, ZEISS Supra 55 VP with Hikari/OIM TSL EDAX detector). The layers are also characterized by Transmission Electron Microscopy (TEM, FEI Titan THEMIS) using Energy Dispersive X-ray Spectroscopy (EDX, Bruker Super-X). Focused Ion Beam (FIB, FEI Helios) is used to prepare the TEM foils.

3. Results

3.1. Growth

Figure 2 presents the surface morphology before and after the GaAs growth. The initial MIC-Ge surface is shown Fig. 2.a, in which the silica support appears dark. The growth of a 40 nm thick GaAs layer (at 630°C for 4.5 min) creates large density of triangular terraces and

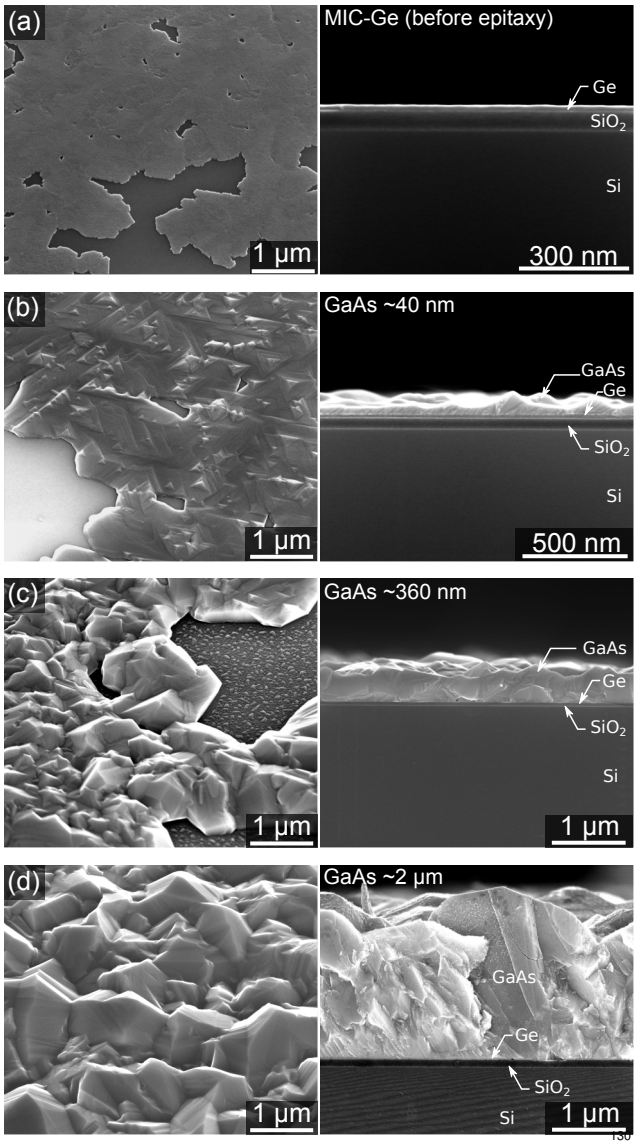

Figure 2: SEM image of the samples before and after GaAs growth of increasing thickness. (a) Bird's eye view (45° tilt) and cross sectional image of the initial MIC-Ge layer. (b-d) Similar images after 40 nm, 360 nm and 2 μm thick GaAs growth on MIC-Ge pseudo-substrates.

small pyramidal hillocks, Fig. 2.b. The triangular shape of the hillocks is compatible with a (111) orientation of the layer. For this short duration, the MBE growth of GaAs is selective and no GaAs crystal nucleates on the silica surface.

For 60 nm thick GaAs layer (Fig. 2.c), grown for 40 min, the surface becomes rougher and small GaAs crystals appear on the SiO_2 layer. For even thicker GaAs layers (2μm), grown for approximately 200 min, the surface is very rough and the growth is not selective at all

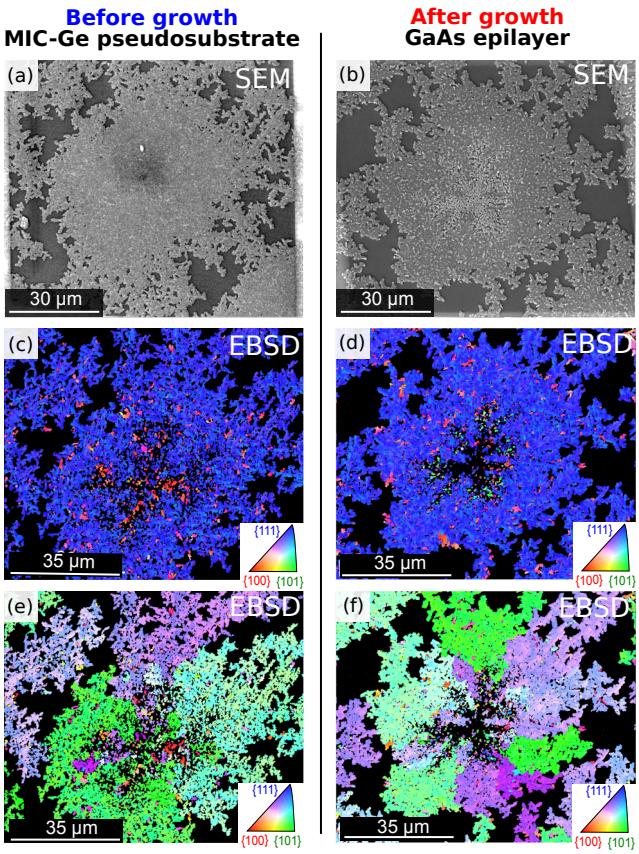

Figure 3: Different zones from the initial MIC-Ge pseudo-substrate (before growth, left) and the GaAs epilayer (after growth, right). (a)(b) SEM top views of the MIC-Ge and GaAs surfaces, respectively. (c)(d) Corresponding ESBD maps of the *out of plane* crystal orientation. The color is assigned from the inverse pole figure in insert. (e)(f) Corresponding EBSD maps of the *in plane* crystal orientation. Same color scale as in (c-d).

(Fig. 2.d).

3.2. Crystal orientation

Figure 3 presents SEM and EBSD characterizations of the sample before and after 40 nm thick GaAs growth. Before growth (Fig. 3.a) MIC-Ge pseudo-substrate is structured in large Ge islands on SiO_2 (more than 50 μm diameter, 20 nm thick) which are mostly (111) oriented, as indicated by the dominant blue color in the *out of plane* EBSD (Fig. 3.c). Although the island shown in Fig. 3.a appears homogeneous, it is actually made of three separate dendritic crystals with different *in plane* orientations (Fig. 3.e). The central core is a defective zone with mixed orientation[29]. Due to the small grain size and poor crystal quality in this area, the corresponding zones appears black in the EBSD maps, Fig. 3.c and 3.e. Between the Ge islands, the amorphous

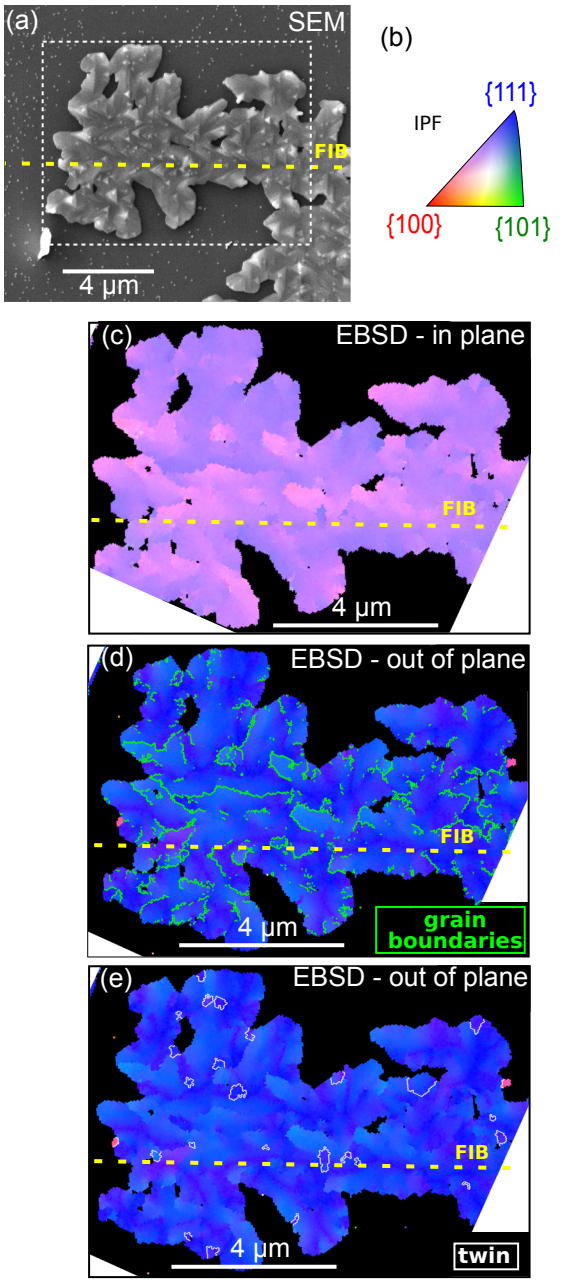

Figure 4: SEM and EBSD characterizations of an area with uniform *in plane* orientation. The yellow dashed line marks the position of the FIB cut used to extract the TEM foil. (a) Top view SEM image showing the zone selected for EBSD analysis (white rectangle). (b) Inverse pole figure (IPF) color scheme used in the EBSD maps.(c) EBSD map of the *in plane* crystal orientation. (d) *Out of plane* EBSD map showing grain boundaries (0-10°) in green. (e) *Out of plane* crystal orientation, twin boundaries are marked in white.

silica substrate does not yield any diffraction signal and also appears black on the EBSD maps.

Figure 3.b presents the morphology after the growth of a thin GaAs layer (40 nm). As already seen in Fig. 2.b, this short GaAs deposition is selective with respect to the silica support and the GaAs crystals only grow on the MIC-Ge islands. EBSD characterization (Fig. 3.d) shows that the preferential (111) orientation of the MIC-Ge layer (Fig. 3.c, blue color) is conserved in the GaAs layer. The central defective core and the dendritic crystals with different *in plane* orientations are also visible in the GaAs crystal orientation (Fig. 3.f), as observed in the MIC-Ge layer before growth (Fig. 3.e).

By zooming on the termination of a large dendrite (Fig. 4.a) we can focus on an apparently monocrystalline area with uniform *in plane* orientation (Fig. 4.c) and (111) crystal orientation (Fig. 4.d). At this scale, small correlated color in the *in plane* and *out of plane* EBSD maps shifts hint at the presence of small adjacent grains with slightly different crystal orientation. To reveal this grainy structure, we highlight in bright green local misorientations (0-10°) between neighboring points (Fig. 4.d). The obtained set of grain boundaries drastically reduces the typical grain size from several tens of microns to one micron approximately. Figure 4.e highlights in white color another set of misorientation (60° *in plane* rotation), which corresponds to twinned domains for (111)-oriented cubic crystals. The typical lateral size of twinned domains is also of the order of one micron or smaller.

3.3. Microstructure

To better understand the microstructure of the MIC-Ge and GaAs layers, we perform a FIB cut in the previously analyzed 'monocrystalline' area (see yellow dashed line in Fig. 4). Figure 5 shows g_{002} dark field images from the TEM cross section oriented along the $[1\bar{1}0]$ zone axis. This type of image is sensitive to compositional changes and permits to differentiate GaAs from and Ge, despite the close lattice match and crystal structure.

In a defect free region (Fig. 5.b), we observe a smooth MIC-Ge layer with a thickness of 20 nm, which is equal to the nominal thickness of the initial amorphous Ge layer (see methods). The thickness of the GaAs layer is 40 nm, as expected from the MBE growth rate (1.5 Å.s^{-1}) and duration (4.5 min).

While no defect is visible in this smooth area (Fig. 5.b), pyramidal hillocks and vertical defects are found in zone with thicker (~60 nm) GaAs (Fig. 5.c). These defects originate from the MIC-Ge layer (orange arrow) and extend to the whole GaAs thickness (green arrows). The area bordering these vertical defect are

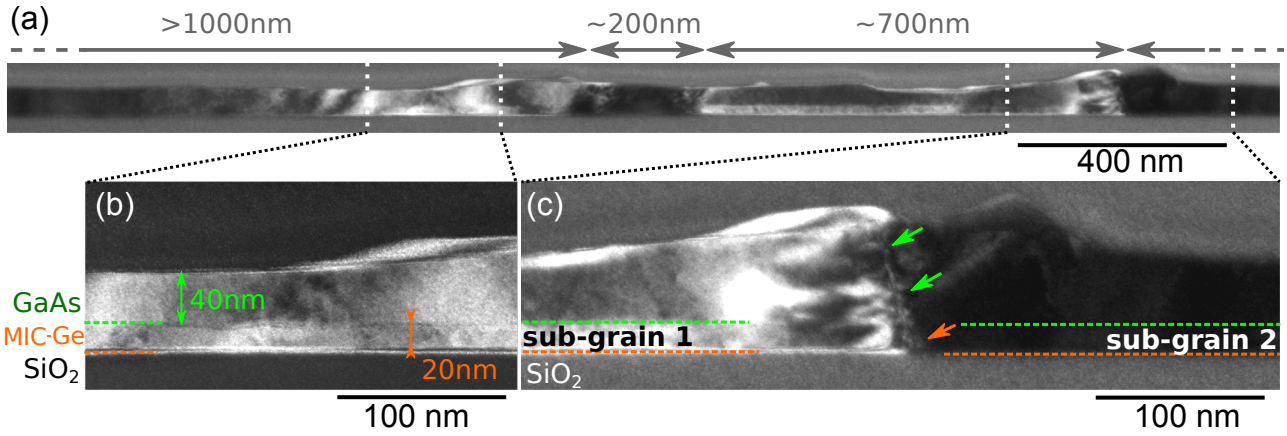

Figure 5: Dark field cross-sectional g_{002} TEM image of the GaAs / MIC-Ge pseudo-substrate near the $[1\bar{1}0]$ zone axis. (a) Large scale view showing the zones selected for further analysis. The lateral size of the sub-grains is indicated above the image. (b) Details of a smooth area showing the thickness of each layer on the SiO_2 support. (c) Details of a pyramidal hillock. A defect from the MIC-Ge pseudo-substrate (orange arrow) extends to the GaAs layer (green arrows).

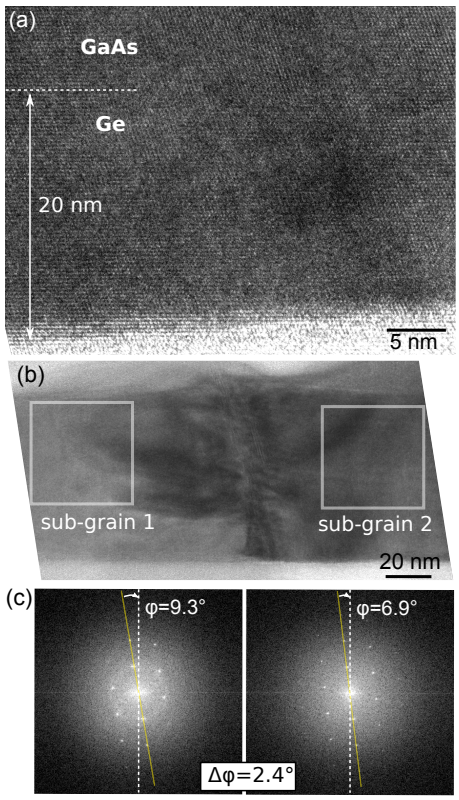

Figure 6: HR-TEM images of the zones analyzed in Fig. 5. (a) Atomically resolved image of the smooth area (see Fig. 5.b). (b) Image of the defective zone with two sub-grains (see Fig. 5.c). The left and right squares mark the zones used to perform FFT. (c) FFT patterns of the left and right sub-grain. Both GaAs crystals are cubic with a relative angular misalignment of $\Delta\varphi$=2.4°.

highly contrasted. Sub-grain #1 (left of the defect) appears in light color while sub-grain #2 (at right) is dark. The lateral size of the sub-grains is between 200 and 1000 nm, or possibly larger (see Fig. 5.a).

Figure 6 presents high resolution TEM (HR-TEM) images of the zones previously analyzed in Fig. 5. The smooth area is detailed in Fig. 6.a. There, we observe the continuation of the cubic crystal lattice from the MIC-Ge pseudo-substrate to the GaAs layer. Figure 6.b shows HR-TEM image of the defective area of Fig. 5.c . Two zones are selected in this image to compute a fast Fourier transform (FFT). This FFT (Fig. 6.c) reveals that two standard cubic patterns with a relative misorientation of $\Delta\varphi$=2.4° between the two crystals. This demonstrates that the extended defect of Fig. 5.c and Fig. 6.b is a low-angle grain boundary (LAGB).

4. Discussion

Beside a few reports on nanowire growth[21, 22, 23], we could only find an two attempts at planar layer epitaxy on MIC substrates: homoepitaxy of Ge on MIC-Ge(111)[15] and hetero-epitaxy of GaAs on MIC-Ge(111)[28]. Contrary to Toko *et al.*[28], who report good photoresponse from GaAs layers grown on MIC-Ge, the disrupted morphology of our thick GaAs layers (Fig. 2) indicates that defects degrades the III-V material quality, at length scales much smaller to the apparent domain size (over 20μm) determined by large scale EBSD (Fig. 3).

4.1. Absence of antiphase boundaries

Compared to commercial 'epiready' monocrystalline Ge wafers, the surface of our MIC-Ge pseudo-substrates is very rough: nanometer sized variations of the MIC-Ge thickness can be seen directly by cross-sectional TEM in Fig. 5, even in the defect-free area. Due to the small thickness of the MIC-Ge layer (20 nm) further chemical or mechanical polishing is proscribed. It is thus critical that the GaAs epitaxy is not sensitive to the Ge surface roughness. Yet, even the standard epitaxy case of polar GaAs on non-polar Ge is known to require a carefully reconstructed double-step Ge(100) surface and a specific wafer miscut[35, 36]. The direct GaAs epitaxy on (100)-oriented MIC-Ge layers is thus likely to hold high densities of antiphase boundaries (APB).

The identification of APB from EBSD maps is a difficult task, as the standard IPF color scheme (Fig. 4.b) is insensitive to 180° rotations, so that it cannot discriminate grains with opposite orientations. Note that this applies to both *out of plane* (Fig. 4.d) and *in plane* (Fig. 4.c) EBSD maps.

Fortunately, the EBSD data (Fig. 3 and 4) show that the main orientation of our MIC-Ge layers is (111), similarly to most layers fabricated by ALILE on silica[13, 30, 15]. On commercial 'epiready' Ge(111) wafers, the polarity of GaAs epilayers grown by MBE is uniquely determined and insensitive to the surface roughness, so that no antiphase domain form during the growth[37, 34]. Our TEM analysis (Fig. 5) did not reveal any APB in our GaAs layers, despite the lower surface quality of our MIC-Ge pseudo-substrates compared to commercial Ge(111) wafers. The growth of GaAs on (111)-oriented MIC-Ge templates remains ABP-free and it is thus a promising combination for the fabrication of low-cost III-V devices on silica.

4.2. Selective growth of GaAs on MIC-Ge(111)/SiO_2

The use of a silica support for the MIC-Ge layers is particularly relevant since SiO_2 masks are already used in the selective area growth of Ge[38] or GaAs[39, 40] by MBE. Despite the relatively high substrate temperature (~630°C), we only observe a partial selectivity for the GaAs growth between the MIC-Ge islands and the SiO_2 support, which is progressively lost as the deposition duration increases from 4.5 to 40 min (Fig. 2). It is possible that the exposed silica still host some residual Al or Ge contaminations from the deposition of the initial MIC structure, despite the thorough chemical cleaning of the MIC-Ge layers (see methods). A solution to this partial selectivity issue is to fabricate MIC-Ge layers with a high surface coverage[13, 15] so that no SiO_2 is exposed to GaAs during the MBE growth[28].

4.3. Epitaxial relationship GaAs/MIC-Ge(111)

By focusing on the thin GaAs layer (~40 nm) for which the growth is still fully selective (Fig. 2), we can learn more about the epitaxial relationship between the GaAs layer and the MIC-Ge pseudo-substrate. The transfer of the large scale (111) crystal texture from the MIC-Ge template to the GaAs epilayer (Fig. 3) is a good indication of the epitaxy relationship. This hypothesis is confirmed by cross-sectional HR-TEM images (Fig. 6), where we observe the continuation of the crystal lattice from the cubic MIC-Ge grain to the GaAs cubic crystal. The growth of GaAs (111) on the MIC-Ge(111) thus proceeds as on standard monocrystalline Ge substrates[37, 41, 34] and preserve in GaAs the same *in plane* and *out of plane* orientations as the Ge substrate. The absence of visible defect by TEM at the GaAs/Ge(111) interface (Fig. 5) demonstrates that our substrate fabrication and cleaning procedures enable the defect-free epitaxy of GaAs(111) on MIC-Ge(111).

4.4. Twinning in GaAs(111) epilayers

As the GaAs growth proceeds in epitaxy with the MIC-Ge substrate, it seems likely that the crystal orientation of MIC-Ge grains is exactly that of GaAs epilayer. Yet it is possible that extended defects in the GaAs layer alter this initial epitaxy relationship.

The color scheme of the EBSD maps stems from a standard IPF (Fig. 4.b). As stated before, this color coding does not differentiate between 180° rotations, so that it is not only insensitive to antiphase domains but also to twin defects. However twin boundaries can be revealed by showing the local 60° *in plane* misorientations in (111)-oriented domains (Fig. 4.e).

From previous work[34] and literature[41] using commercial monocrystalline Ge(111) wafers, we know that the MBE growth of GaAs on Ge(111) is prone to twinning and that the twin density can be minimized by adapting the V:III ratio during growth. The Figure 4.e shows that twinned area fraction is relatively low (3%) using MIC-Ge pseudo-substrates. Yet, we cannot fully replicate the growth of twin-free GaAs layers obtained on commercial Ge(111) wafers, even we use the same optimized growth conditions[34]. It is also possible that twinning occurs in the MIC-Ge layer, during the Ge crystallization, but we did no investigate this hypothesis further due to the low density of twinned domains compared to other extended defects.

4.5. Microsctructure of MIC-Ge pseudo-substrates

We previously studied the macrostructure of our MIC-Ge layers on silica using *in situ* optical

microscopy[29]. This study showed that the defective core of each Ge island crystallizes from a parasitic MIC process, while the radially expanding (111)-oriented dendrites are created by the standard ALILE mechanism. These large Ge have different *in plane* orientations (Fig. 3.e), and it is generally accepted that they are monocrystalline[15, 30, 31], as supported by large scale EBSD maps.

However, one can usually find grains with a different orientation, typically close to (100), in the otherwise (111)-oriented dendritic crystal (see red dots vs blue patches in Fig. 3.c). By zooming on the termination of a large dendrite (Fig. 4), we avoid such localized defects and we can assess the quality of the main fraction of the GaAs epilayer. Hence, whereas the GaAs appears homogeneous at large scale, it breaks down into small sub-micronic domains at small scale. Beside a minor fraction of twinned domains (Fig. 4.e), we observe correlated color shifts in the *in plane* (Fig. 4.c) and *out of plane* (Fig. 4.d) EBSD projections, some of which are identified as grain boundaries (Fig. 4.d). However EBSD characterization is usually performed on flat surfaces, which are usually obtained after fine mechanical polishing or ion milling. Considering the disrupted morphology of our 40 nm thick GaAs layers (Fig. 4.a), the small angular misorientations highlighted in Fig. 4.d could be EBSD artefacts due to rough surface of the sample. It is therefore important to complement the EBSD data by another characterization technique.

Using cross-sectional TEM, we link the position of the triangular hillocks observed by SEM (Fig. 4.a) with those of extended defects inside the GaAs layer (Fig. 5). Further analysis (Fig. 6) demonstrates that the observed extended defects are low angle grain boundaries (LAGBs). Combining both TEM analyses (Fig. 5-6) with the SEM overview (Fig. 4), we hypothesize that each hillock may be associated to a LAGB. This high density of LAGB is coherent with the estimated position of grain boundaries computed by EBSD (Fig. 4.d). The typical grain size determined by TEM, (200-1000 nm, Fig. 5) matches the length scale of the small tonal changes in the EBSD maps (Fig. 4.c) and the sub-grain width of Fig. 4.d. The inner structure of a LAGB consisting in a dense 1D array of dislocations[42], the high density of LAGBs also explains the poor optical quality of our GaAs epilayers (not shown).

The Fig. 5.a and Fig. 6.b clearly show that the LAGB originates from the MIC-Ge layer. This implies that the epitaxial growth merely extends the defective microstructure of the MIC-Ge pseudo-substrate to the GaAs layer. Compared to other attempt at planar epitaxy using MIC-Ge pseudo-substrates[15, 28], we observe defect-free regions (MIC-Ge and GaAs layers) which span more than several hundreds of nanometer (Fig. 5), with only a couple of LAGB over one micron. This suggests that the quality of our MIC-Ge material is better if not comparable to the state of the art.

Moreover, we note that the small orientation shifts characterized by EBSD (Fig. 4), which we link to the defective LAGB microstructure (Fig 6), are visible in most of the literature on crystalline Ge layers fabricated using ALILE[15, 30, 31, 13] or gold-induced crystallization[43]. It is thus likely that the formation of LAGB is intrinsic to the metal-assisted crystallization of thin Ge layers, as regards the published results on (111)-oriented MIC-Ge layers on silica.

5. Conclusion

We have successfully performed the heteroepitaxy of GaAs by MBE on (111)-oriented MIC-Ge pseudo-substrates fabricated on SiO_2 supports. The epitaxy relationship between GaAs and MIC-Ge is the same as for standard growth on monocrystalline bulk Ge wafers. No extended defect nucleates at the GaAs/Ge growth interface, which indicates that our cleaning procedures are adequate. The low fraction of twinned GaAs crystals indicates that our MBE growth conditions are close to optimal values. However, the epitaxial growth transfers the defective microstructure of the MIC-Ge pseudo-substrate to the GaAs epilayer so that the final III-V material is of poor quality. Despite an apparent homogeneity at large scale and EBSD maps similar to the current literature, we find that our MIC-Ge layers are composed of slightly misaligned small crystallites (200 to 1000 nm wide), even in apparently 'monocrystalline' domains. This defective microstructure appears as small tonal variations in standard EBSD maps. The observed high density of low-angle grain boundaries, hence dense dislocation arrays, impact the final III-V material quality and may limit the performance of III-V devices fabricated on MIC-Ge pseudo-substrates.

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