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# Impact of Technological Trends and Electromagnetic Compatibility of Integrated Circuits

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## Abstract:

This paper introduces the main trends in the integrated circuit manufacturing industry, the driving forces in relation to complexity, operating frequency, device performance, trends in supply voltages and data rate exchange between devices. The roadmap summarizes IC performance in terms of technology nodes, ranging from  $\mu\text{m}$  to nano scales and targeting CMOS technology. The consequences of this technological evolution on Electromagnetic Compatibility (EMC) of ICs are also discussed. Finally, a review of recent research in EMC of ICs is proposed through a selection of recent scientific papers published these last three years.

*This paper was presented as a keynote speech by E. Sicard at EMC Compo 2019, Haining, China. This paper has been submitted to "Safety & EMC", English Edition 2020.*

## 1. Introduction

Integrated Circuits (ICs) are key elements in EMC issues of electronic equipments, as they are both the sources and the victims of electromagnetic disturbances that they produce. Although semiconductor devices are not subject to EMC regulations such as the European EMC Directive or FCC Part 15, IC end-users decline the EMC constraints at electronic equipment level to the IC level, pushing pressure on IC designer to take into account EMC.

In parallel, IC development is pushed by an incredible technological evolution to scale down MOS devices constantly and increase the level of integration of heterogeneous functions within the the same die or the same package. However, this technological evolution has consequences on EMC and put pressure on IC designers to meet EMC requirements at reasonable costs. For more than 40 years, researchers and engineers have continuously developed measurement methods prediction tolls and design techniques for improving the EMC performance of ICs [1]. These huge research efforts is still on-going to keep building low emission and noise immune ICs.

The purpose of this paper is to present a brief overview of the main current trends of semiconductor market which push IC manufacturers to innovate continuously to design smaller MOS devices with a denser level of of integration, and then discussed about the consequences on EMC of ICs. Finally, this paper also provides a selection of recent scientific papers published these last three years. This selection is not exhaustive and the authors apologize for all the publications not mentioned here.

## 2. The growth of the Electronics Industry

The growth of the overall electronic market over the last 40 years is illustrated in Fig. 1. It can be seen that electronic equipment for companies was the main driving force for electronic market growth up to 1995. Then, from 2000, consumer electronics, e.g. home computers, Internet-related devices and personal mobile phones, took the lead. Although the economic recessions in 1990 and 1997 did not severely impact the electronic industry, the "telecom crash" also called "dot.com" recession in 2000 led to a historic decrease, with the market shrinking by nearly 12%. While DVDs, flat screens, automobile equipment and 3G phones stimulated a market recovery in the 2002-2007 period, the "sub-prime bank crash" of 2008 again slowed down the electronics economy. In the 2010-2019 period, new markets in relation to society as well as 4G smartphones, Internet of Things and 4K TV have lead to sustainable growth. The overall market reached 1 Tera \$ in 2016, and thanks to an expected Average Consolidated Growth Rate (ACGR) around 6% from 2019 to 2024, 2 Tera \$ could be reached by 2025.

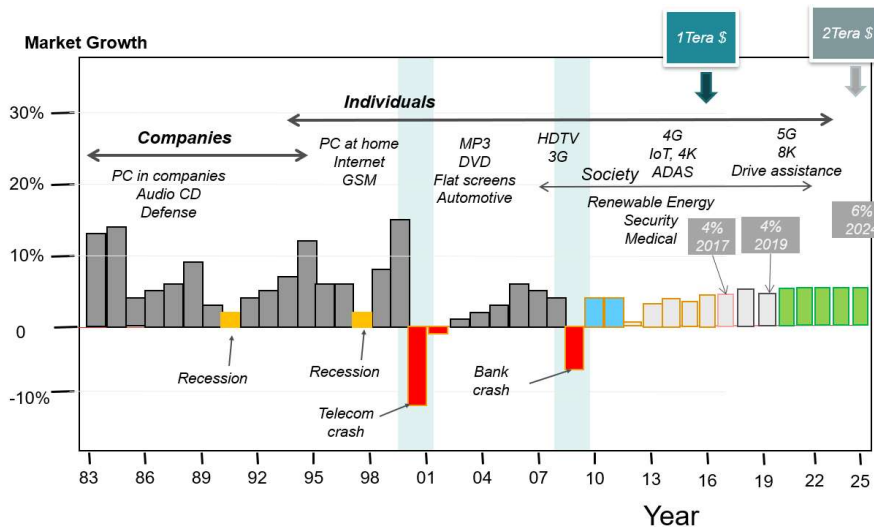


Fig. 1 - The trends in electronic growth over the last 40 years

Share of system sales  
2024 vs 2019

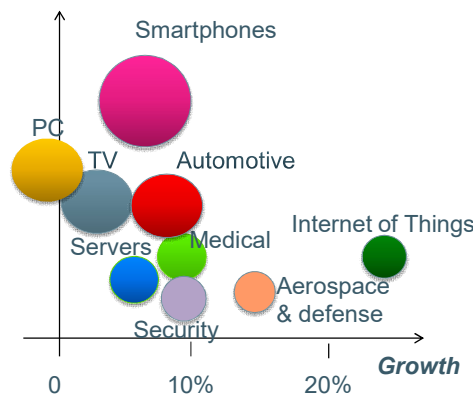


Fig. 2 - Electronic market growth by application, from 2019 to 2024

Due to an increasing disposable income and reduced prices of electronic products, the expanding urban population, growing Internet penetration and the availability of wideband communication networks, we foresee a significant growth in the Internet of Things, 5G smartphones, 4-8K resolution TV sets, artificial intelligence, cloud computing, smart home/city, wearable for autonomous cars, hybrid and electric vehicles and medical (personal health care) applications (Fig. 2). Moreover, the upgrade of existing power infrastructure, the development of renewable energy sources (e.g. photovoltaic and wind energies) and the increasing demand of power management in battery-powered portable devices boost the market of power electronic. Electronic products can be classified in various categories, such as discrete devices, sensors, modules and integrated circuits. ICs are fundamental parts of electronic systems and constitute a major part of the electronic market. The semiconductor industry market is 440 billions \$ in 2019 with an average growth of 13 % over the period 2016-2018. It is expected to reach 573 billions \$ in 2024. We may also distinguish four main classes of ICs:

- microprocessors and microcontrollers: a market of 65 billions \$ in 2018 with a growth of +3.5 %
- logic circuits (e.g. Programmable Logic Devices, Application Specific Integrated Circuits): a market of 108 billions \$ in 2018 with a growth of +7 %
- memories (mainly NAND Flash and DRAM): a market of 134 billions \$ in 2018 with a growth of +9.3 %
- analogue components: a market of 56 billions \$ in 2018 with a growth of +6.1 %.

Microprocessors are the main components of laptops, which need external components to operate, while microcontrollers usually include several types of memories and interfaces such as analogue converters and buses for self-sufficient operation. Considering mobile communications itself, the web site gsm-intelligence gives in real time the overall numbers regarding mobile communications (9,320 billion in Oct. 2019), unique mobile subscribers (5,146 billion) and the global revenue higher than 1 Tera \$ (Fig. 3). Memory ICs dominate the market because they are predominant in many applications

such as smartphones, tablets, computers, smart cards, digital cameras, media players, medical devices or USB drives.

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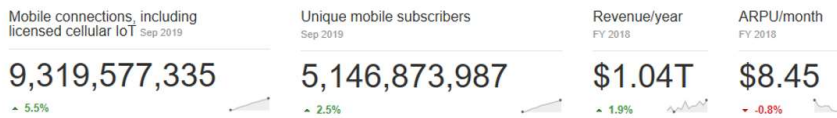


Fig. 3 - Mobile communications in Oct. 2019 (from www.gsmaintelligence.com)

Analog circuits form an heterogeneous class since it includes various types of electronic functions: operational amplifiers, audio-amplifiers, LED/display drivers, data converters, serializer/deserializers, timing control, radiofrequency transceivers, bus drivers, voltage regulators, power converter controllers, power management, etc.

### 3. Technological trends of Integrated Circuits

#### a. Increasing Integrated Circuit Complexity

The evolution of CMOS digital ICs, e.g. microprocessors and memories, follows Moore's law, which predicts that the number of transistors on a same die doubles every 18 months, due to a continuous shrinking of the physical dimensions of MOS devices. The promise of this driving force is to offer a more performant and complex IC (i.e. more functionalities) to the end-user at a lower cost. The trend towards more complex ICs is illustrated in Fig. 4, taking as an example the mobile generations from 2G from 5G. Although the number of devices per die may saturate due to cost, design and yield issues, advanced packaging technologies such as the 3D stacking of chips or interposer technology may offer around 150 Giga Transistors by 2020. Single dies such as Kirin 990 from HiSilicon which controls the Huawei Mate 30 integrates 10 Billion devices in 7nm technology. 5G processing devices include eight 32-bit microprocessors (MCU), 8K image processing, 4 to 8 cameras, around 16 Graphic Process Units (GPU), but also dedicated processors for artificial intelligence (IA), positioning, cryptography as well as millimeter wave communication devices in the newly opened 27 GHz bandwidth.

It is anticipated that autonomous cars will require highly intensive and reliable computing, with a global trend towards hybrid/electrical car for low carbon emission, embedding 100 to 1000 processors and multi-sensor approaches with very high data rates.

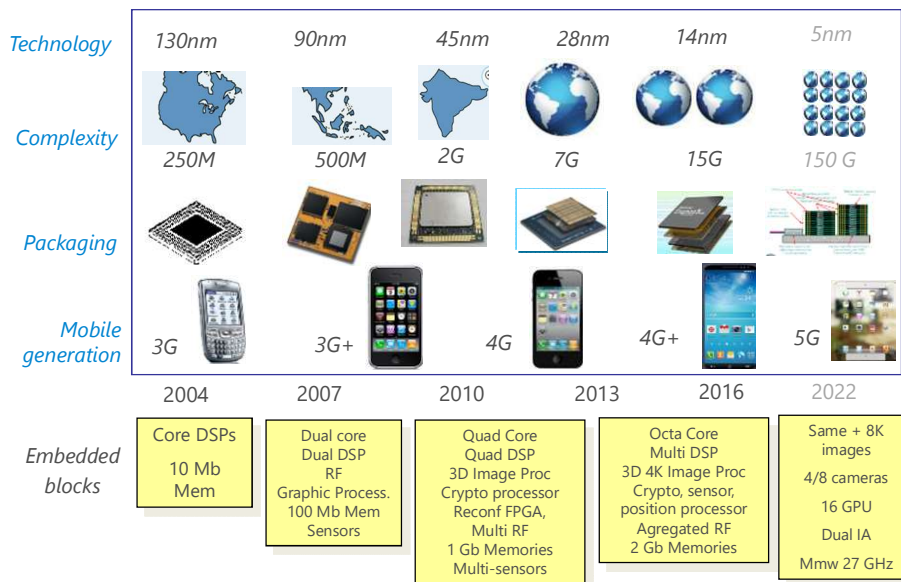
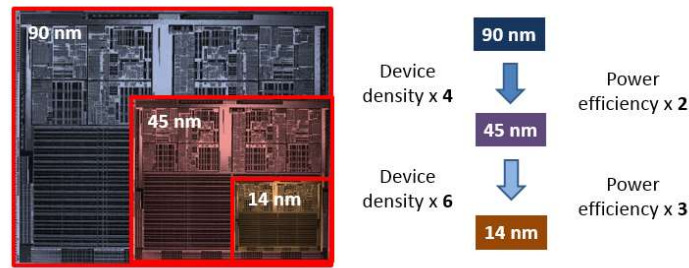


Fig. 4 - Illustration of increasing complexity of digital ICs and trends up to 2022

Two important arguments for feature size reductions are the decreases in die size and power consumption. Talking of size reductions, a factor of 20 is achieved moving from 90 nm to 20 nm technology while reducing power consumption for the same functionality by a significant factor (Fig. 5). The power consumption per gate is tending to decrease due to a combination of positive factors such as reduced capacitance loads and supply voltage, and negative factors such as shorter

channels, increased switching efficiency and a lower threshold voltage. The overall trend is a reduction of the power per gate by 40% between technology nodes (90 nm to 65 nm, 65 nm to 40 nm, etc).



**Fig. 5 - Feature size and power consumption reduction trends. The device density is multiplied by four from 90 to 45 nm, and by six from 45 to 14 nm with important power savings**

Similarly, for the other class of ICs (e.g. analog ICs), the complexity also increases not only due to MOS device miniaturization, but also due to a diversification of the embedded functions embedded within the same circuit. This trend, called More than Moore, is based on the integration of heterogeneous functions such as power, RF, digital, sensors, etc... , either on the same or in the same package. For example, the massive introduction of electronics in automotive these last decades was possible due to the development of smart power ICs, i.e. complex system-on-chip including a digital signal processors along with the power device (e.g. monolithic DC-DC converter, power drivers, bus transceivers or battery management circuits). In these circuits, power devices, drivers, filters, command, configuration and diagnosis functions are integrated in the same chip to reduce cost and improve safety. Smart power ICs will continue to play a major role in automotive electrification. Heterogeneous integration is also fundamental in the development of advanced sensors required in mobile devices and Advanced Driver-Assistance Systems, or in 5G wireless networks which use adaptive antenna arrays for beamforming.

### b. Improved switching devices

The improvement of lithography techniques and the introduction of strain-enhanced, high-K gate dielectric materials, metal gates and, more recently, FD-SOI and, especially, FinFET technologies have led to continuous improvements in the intrinsic current-switching capabilities of MOS devices, characterised by their drain current at on state,  $I_{on}$ . The trend between  $I_{on}$  (switching performance) and  $I_{off}$  (parasitic leakage) currents is illustrated in Fig. 6 by the three lines ( $I_{off}$ =100, 10 and 1 nA/ $\mu$ m) [2]. High performance tolerates very high leakage (100 nA/ $\mu$ m), while low power is only around 1 nA/ $\mu$ m, with reduced switching capabilities. It is anticipated that "ultimate" nano-cmos technology nodes starting 5nm and beyond will replace the FinFET with a so-called Gate-All-Around Multi-Gate device (GAA-MG) as announced by IMEC & Samsung [3]. To fabricate such devices and the overall embedded electronic equipment, a considerable variety of materials is required among which some very rare or critical materials, as reported in Fig. 7.

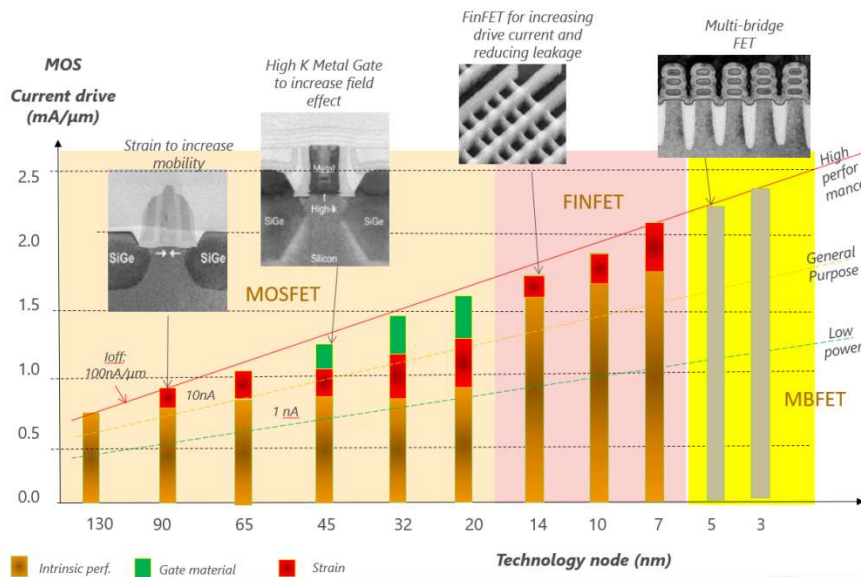


Fig. 6 - Trends towards an increase in the current drive of MOS devices [2]

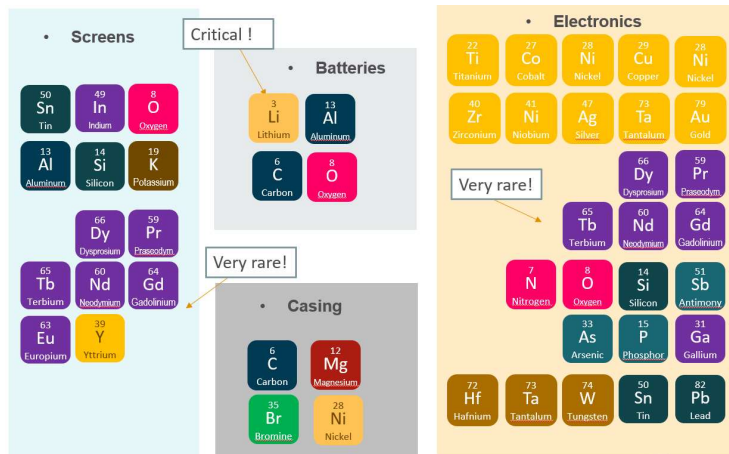


Fig. 7 - Some key materials used to fabricate embedded devices such as smartphones

### c. Reduced power supply voltage

In order to maintain sufficient reliability and avoid thermal issues due to dynamic current, the power supply of IC is scaled down according to the technology node. The reduction in power supply voltage from 0.35  $\mu\text{m}$  to 45 nm technology was very rapid, but slowed down between the 90 nm and the 7 nm node (Fig. 8). The scaling of power supply voltage is not obvious: decreasing power supply voltage reduces dynamic current  $I_{\text{on}}$  but degrades transistor performance. It can be compensated by a reduction of the threshold voltage which, in turn, increase leakage current. The introduction of FinFET starting at 7 nm for most silicon foundries should enable further reductions in VDD power supply, as the threshold voltage may be scaled accordingly. Considering a noise tolerance around +/- 10% of the nominal supply, the noise margin has been rapidly decreased from a comfortable 300 mV in 180-nm technology to less than 50 mV in 7-nm technology. The reduction of power supply voltage has also consequences on analog IC design. Typically, analog blocks are made of a stacking of several transistors which requires a sufficient voltage swings. This situation gets worse with the slower reduction of threshold voltage. Mixing digital and analog functions in nanometer technologies and ensuring excellent performances is a real challenge for designers. They have to find acceptable compromises by using technology options and original design techniques.

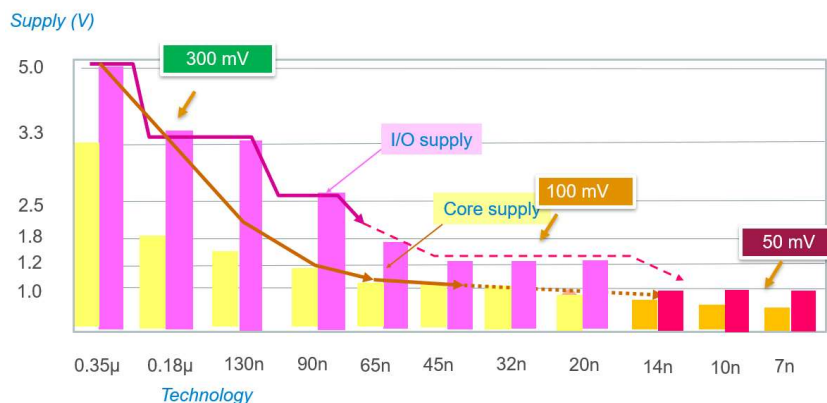


Fig. 8 - Trends in IC voltage supply showing a decrease in VDD, with a target around 0.5 V with 5 nm technology, and 10 % noise margin

### d. Towards higher Frequencies

Fig. 9 gives an indication of the saturation effect of CPU clock frequency, the average lying around 2-3 GHz in 2015-2020 designs. However, high-end products such as Intel core i9 and AMD A-10 are approaching 5 GHz. This saturation effect is due to the parasitic capacitance and delay effects in IC interconnects with the technology scale down, which tend to limit circuit switching performance. The trend is clearly to compensate this frequency saturation through a multicore rather than single core design. Up to 30 dedicated processors are implemented in a single SoC for handling the 5th generation of mobile communications.

Meanwhile, licenced bandwidths for 2-6G communications regroup a wide range of small bandwidths, each of them having its own specificity in terms of efficiency, allowed number of users, modulation & propagation characteristics (Fig. 10). At frequencies below 1GHz, efficient wave propagation enables to construct large radiocommunication cells (meaning a reduced number of base stations). As the bandwidth is usually very reduced and shared among all operators, data rate is limited. In the 1-5 GHz bandwidth, propagation starts to be more efficient but allowed bandwidth is larger, meaning medium cell size and medium data rate. In the new 27 GHz bandwidth for 5G, propagation is much less efficient, requiring a huge number of base stations to communicate with user's equipments, but with a much larger bandwidth enabling high data rates.

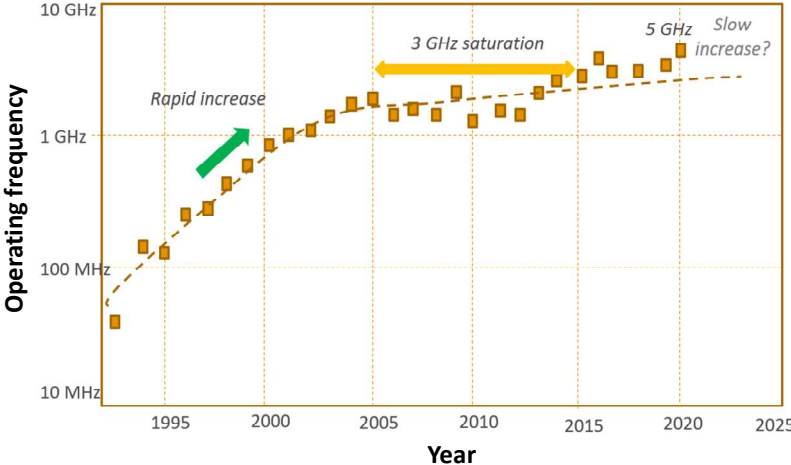


Fig. 9 - The trend towards saturation of CPU clock frequencies



Fig. 10 - 2-5G mobile bandwidths, and prospective 6G bandwidths in 100 GHz range

Currently EMC at IC level is usually characterized up-to 6 GHz. Most measurement standards like IEC 61967 [4] for emission and IEC 62132 [5] for immunity cover the range 150 KHz to 1 GHz. Extensions of these standards have been proposed up to 3-6 GHz and even 10-25 GHz such as the GTEM cell. However, as millimeter-wave 5G operates at 27 GHz and 6G may operate at 100-200 GHz (Fig. 11), either substantial extensions of existing approaches or completely new measurement approaches are required to characterize future EMC of ICs.

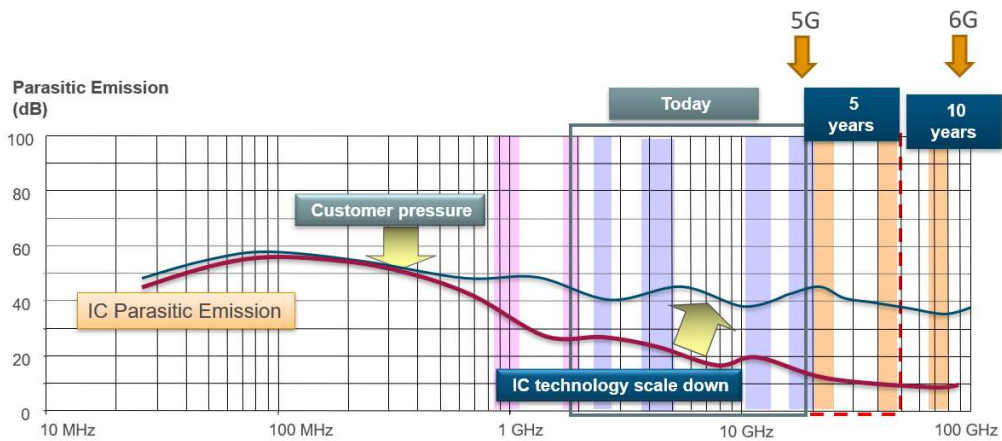


Fig. 11 - Customer pressure towards lower parasitic emission and measurements extended to several GHz

### e. Input/output Data Rate increase

The link between microprocessors and memories has been the subject of intensive research in order to improve the data rate of exchanges required by high performance computing, high speed networking and high resolution real-time graphic processing. One of the proposed solutions is DDR, which stands for “Double Data Rate”, with GDDR standing for for “Gigabit Double Data Rate”. In other words, data is transferred two, three or even four times faster than the clock.

The rapid increase in data rate for exchanges between the CPUs and the external memories is illustrated in Fig. 12, according to Micron memory manufacturer. The voltage supply is globally decreasing (2.5 V in DDR1, 1.2 V in DDR4), while data rates have reached 10 Gigabits per second per pin. The memory bus should increase in size, as forecast by Micron.

We may consider three classes of memories:

- High Bandwidth Memory targeting and increased memory/ processor bandwidth. Using 3D integration and stacked silicon layers, devices such as Hybrid Memory Cubes (HMC) are targeted for high performance computing in Artificial Intelligence, for typical applications such as autonomous drives.
- Mobiles use dedicated low-power memory devices called LPDDR. Currently, generation 5 (LPDDR5) enables data rate per pin approaching several giga bits, thanks to low voltage swing and symbol duration less than 50 ps.
- Graphic memories (GDDR5, GDDR6) are focused on high resolution games, high resolution screen management, real-time video encoding and object recognition [6].

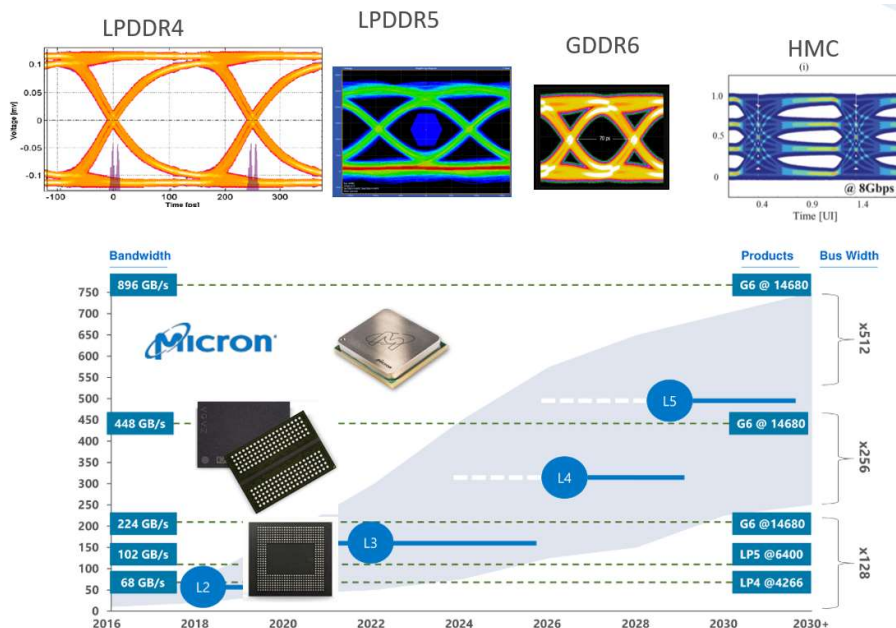


Fig. 12 - The trend towards faster CPU-memory data rates according to Memory manufacturer Micron [6]

## f. Technology options to reduce substrate coupling

The design of mixed-signal analog digital circuit in traditional bulk CMOS process can be compromised by substrate coupling. The noise from noisy blocks can degrade the performance of sensitive blocks. Similarly, in high voltage smart power Bipolar-CMOS-DMOS (BCD) or high voltage CMOS technology, the large voltage fluctuations due to power MOSFET switching may produce minority carrier injection which can be collected by surrounding low voltage device. In the best case, it may affect their performance but, in the worst case, destructive latch-up may occur. The sensitivity to electrical fast transient and ESD is also affected by substrate of the ICs. Isolation must be brought between transistors and it is provided only by PN junctions and guard rings in traditional CMOS process.

To overcome these different issues, CMOS process has evolved these last decades and several advanced techniques are now available, according to the technological process introduced in the 1990's, isolation can be improved by triple well CMOS process, where a deep N-well layer provides a double PN junction isolation. Recently, wafer thinning with backside contacts has been developed to reduce on resistance and inductance of power MOSFET, which reduce latch-up risks. Moreover, it facilitates the 3D integration. Deep trench isolation is powerful option to reduce substrate coupling, for example in power ICs or imaging sensors. With the introduction of buried oxide layer, Silicon On Insulator cancels the risks of latch-up while it reduces significantly substrate coupling in digital-analog mixed ICs. Obviously, the introduction of advanced techniques to reduce substrate coupling is costly compared to the traditional bulk CMOS process.

## e. Going 3D

The move towards 3D integration is due to the bandwidth limitation inherent in 2D implementation. Interconnects are long and may introduce excessive resistive, capacitive and inductive stray elements. It may lead to substantial power dissipation and high-speed signal distortion.

Package-on-package (PoP) technology has reduced the physical distance between ICs, thus increased signal transmission efficiency while limiting power dissipation. The packages are connected using dedicated through-mould vias (TMV) which make the electrical link between the packages' bottom and top pins as short as possible. However, limiting factors include the packages' inductive and highly coupled signal traces, together with thermal and reliability issues linked to the stacking of packages.

The main driving forces behind the adoption of 3D ICs are the increasing demand for devices with faster data exchanges, lower power consumption and smaller chip size. The global 3D IC market has until recently been dominated by the information and communication technology sector due to bandwidth requirements for high-performance networking and the demand for increased storage capacity. Major players from the semiconductor and packaging industry (TSMC, Xilinx, Samsung and Terrazon) have entered the 3D IC integration arena, making competition intense.

As for PoP technology, one of the first commercial 3D IC products featured a memory stacked on a processor, with the following main advantages :

- a massive increase in bandwidth due to use of TSVs instead of conventional I/O pins;
- an increase in on-chip storage capacity enabled by the ability of 3D integration to mix heterogeneous process technologies;
- power savings achieved by reducing the need for the interconnect and I/O drivers associated with off-chip memories.

An example of a 3D IC is shown in Fig. 13. Silicon dies are stacked directly then connected together using direct bond interconnects (DBI) and TSVs. Note that the upper memory die is thinned to 10  $\mu\text{m}$ , and that more thinned dies may be stacked on top of the structure.

## 3. Impact of technology trends on EMC of ICs

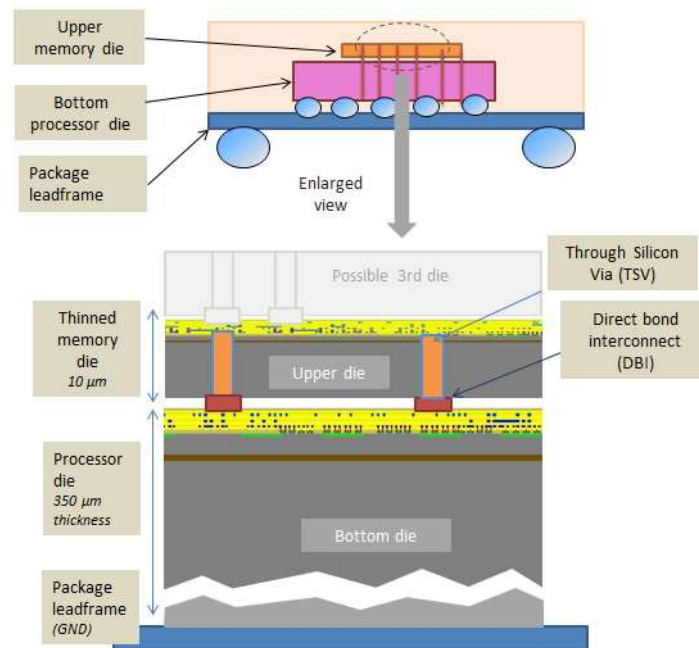
In the previous part, the main driving forces which govern the evolution of semiconductor and IC package technologies have been presented. They have an impact on emission and susceptibility issues at IC level, that is discussed in this part. IC technological evolution is complex and may have contradictory effects on emission and susceptibility. Thus, it is extremely difficult to draw definitive conclusions about increase of EMC risks. The purpose of this part is to present the different likely effects and highlight the consequences for IC designers.

### a. Effect of technological trends on electromagnetic emission

Electromagnetic conducted emission of ICs depends mainly on two parameters [7]:

- the dynamic current consumption, related to the internal activity of the IC and I/O switching

- the filtering provided by IC internal interconnects and package pins, mainly related to power supply and ground paths



**Fig. 13 - Example of a 3D IC with one bottom die and a thinned die on the top, linked with Through-Silicon-Via and Direct Bond Interconnects**

The radiated emission depends also on the length of the interconnects and distance of external decoupling capacitors. The dynamic current consumption depends on the number of I/O and digital gates which may switch simultaneously, and the dynamic current that each gate consumes. The technology shrinking of MOS devices leads to a reduction of dynamic current per gate, but this effect could be counterbalanced by the number of devices per die surface. It is unrealistic that the technological evolution leads to a dramatic increase of the noise produced by ICs since it would be unacceptable from a power consumption point of view. However, increasing the number of devices within the same die or the same package forces IC designers to control and limit conducted emission, for example to ensure power integrity (PI). A typical and essential approach consists in distributing on-chip decoupling capacitors as close as possible to the noisy blocks. We can expect that the miniaturization trend of MOS device will not reduce the surface allocated to on-chip decoupling capacitors.

The increase of data rate exchange leads to faster I/O buffers which enhance the high frequency content of electromagnetic emission. The same trend can be expected for internal activity noise due to the reduction of interconnect length. In spite of shorter interconnects between IC dies (e.g. TSV), which reduce the effective length of parasitic antenna, they can be excited by larger high frequency current if it is not controlled. Besides, the development of faster I/O buffers requires more stringent time margins which are combined with tighter voltage margins. This trend will not relaxed signal integrity (SI) constraints which will require continuous efforts in interconnect design and signal processing to be fulfilled. The use of differential bus would provide a significant reduction of comomo-mode radiated emission only if rigorous symmetrical design is done.

The reduction of interconnect length has a serious impact on the attenuation of signal integrity and radiated emission issues. However, it can enhance side effects such as the risk of near-field or substrate couplings. It is especially true for mixed-signal circuits, 3D assembly of heterogeneous functions, RF/microwave package [8] [9]. Evaluating the significance of these couplings is not straightforward and relies on precise 3D electromagnetic simulation for near-field coupling and TCAD simulation for semiconductor substrate coupling.

Semiconductor technology shrinking and new package assembly techniques offer new possibilities to designers to develop more and more complex ICs, but create new challenges. One of them is related to simulation and modeling to anticipate EMC non compliance and failures. The increasing number of devices in the same die makes full-chip simulation more and more time consuming and difficult to be accurate and efficient in an industrial process. The development of model order reduction methods is absolutely necessary to accelerate simulation and provide efficient prediction tools to IC designers. Advanced packaging assembly, with the increase of interconnect density and 3D stacking, introduces the same type of problems for electromagnetic simulation [10]. IC-package-printed circuit board co-simulation is essential for SI, PI and radiated emission prediction in order to validate designs. Continuous efforts must be brought to develop simplified modeling procedures and efficient simulation tools. The increase of complexity of IC poses also a serious problem to end-users for the

validation of EMC of their final products. From end-user point of view, IC becomes more and more a black-box. Because of the extremely high level of intellectual property associated to IC, IC manufacturers deliver little information to help end-users to develop IC equivalent models. Even if they can provide standard equivalent models, such as IBIS files for SI simulation, equivalent models for PI and emission simulation are rarely provided. Even if technical solutions exist (e.g. IEC62433-2 standard Integrated Circuit Emission Model (ICEM) [11] and ANSYS Chip Power Model), they are not completely mature and accepted. Huge efforts must also be brought to develop standard exchangeable equivalent models for the simulation of IC emission issues.

## b. Effect of technological trends on electromagnetic susceptibility

The susceptibility of ICs to electromagnetic disturbances depends mainly on several parameters [7]:

- the filtering of incoming conducted disturbances by internal interconnects and package pins
- the clamping of large disturbance provided by ESD protection structures
- the intrinsic sensitivity of on-chip electronic functions

The sensitivity of electronic functions is strongly dependent on their nature (analog or digital) and their design. For example, a RF receiver is extremely sensitive to electromagnetic noise coupling to its inputs and power supply compared to a digital circuit. Thus it is difficult to draw a definitive conclusion about the impact of technological evolution on electromagnetic susceptibility. Nevertheless, it is obvious that the decrease of power supply voltage lowers the noise voltage margins of both digital and analog circuits. As the immunity level does not change at system level, either more external filtering or design of more robust IC is required. The reduction of power supply voltage is also challenging for the design of analog functions. Designing performant and robust analog functions is always a search for compromise [12], which will become more and more difficult as the power supply voltage decreases.

As underlined in part 3.a, miniaturization and advanced package assembly lead to the integration of mixed-signal functions in a smaller volume. The proximity of RF, analog, digital and power management on the same substrate or in the same package increases the risk of intrasystem interference within the same IC. Ensuring coexistence of these different functions requires better filtering of noise, better substrate isolation techniques, less noisy and more robust functions, which push more pressure on IC designers. The validation of the proposed solutions relies on accurate and efficient enough modeling and simulation tools, which still lack for substrate coupling issues in smart-power devices [13].

IC susceptibility to transient disturbances, such as electrostatic discharge (ESD) or electrical fast transient (EFT), is highly related to on-chip ESD protections. As MOS device gate oxide becomes thinner, semiconductor devices break down at lower voltage. Unfortunately, since the mid 90's, the robustness level of IC to ESD decreases continuously (from nearly 6 kV HBM level in 1993 up to less than 2 kV in 2020) [14]. This trend is mainly due to better process and manufacturing control in ESD protected areas, which reduces the robustness requirements of ESD protections. However, it raises serious problems to IC immunity to high level transient disturbance. Designers must elaborate more and more complex ESD protection strategies to trigger on incoming disturbance correctly and evacuate current [15], which may have negative consequences on EMC [16]. As underlined in part 3.a, the increase of complexity of ESD protection strategy leads also to modeling issues for IC end-users, especially for automotive equipment manufacturers which have to comply with stringent transient immunity requirements. Due to the high level of confidentiality about ESD protection strategy, no equivalent models are delivered by manufacturers and it remains a black box for end-users.

Contrary to SI, PI or emission issues, no mature standard IC models exist. Only standard proposals have been developed such as IEC 62433-4 - Integrated Circuit Immunity Model [17] for RF conducted immunity modeling purpose and on-going works are done by the ESD Association Working Group 26 - System ESD Modeling for immunity to transient disturbance.

## 4. Approaches to improve EMC of Integrated Circuits

There is a variety of approaches to improve EMC performances of ICs described in reference books such as [18] mostly focused on logic circuits and [12] for analog circuits. One tutorial book [7] gives the basis of EMC-IC modelling and details several case studies, with comparison between predicted EMC using IC-EMC [19] and measurements according to IEC emission & immunity standards.

Considering the most recent publications during the three last years, we observe many different types of approaches, serving either an improved robustness to EM interference, reduced parasitic emission or self-immunity within the circuit itself. An overview of the existing approaches to tackle EMC problems at IC level is given in Fig. 14. The next parts provide a brief summary of recent significant contributions according to the authors' point of view.

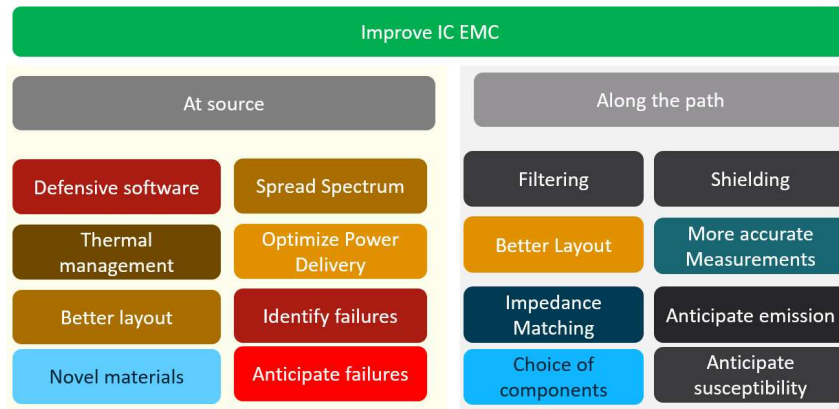


Fig. 14 - Existing approaches to improve EMC at IC level

### a. Shielding

The development of 3D ICs increases the risk of intrasystem interference due to the short distance between noise source and victim circuits within the same package. Shielding is a traditional technique to reduce both far-field and near-field radiated emission. However, adding metal cans increases the cost and result in larger modules. New shielding concepts emerge these last years to overcome these issues. For example, conformal shielding consists in a thin conductive and adhesive layer placed directly on the molding of a 3D assembly. In [9], a 400  $\mu\text{m}$  conductive layer is used to shield a chip in an assembly of two stacked dies and provides an improvement of 20 to 50 dB of the isolation between both chips. Other works deal with the material to reduce the shield layer thickness while maintaining excellent shielding effectiveness.

New materials such as negative and near-zero permeability metamaterials have been analyzed in [20], featuring 15 dB shielding effectiveness. Flexible, thin composite films are proposed by Rathi [21] to enhance the electromagnetic compatibility of biomedical electronic devices, with an Electromagnetic shielding effectiveness ranging from 20 to 30 dB. Graphene, carbon-nanotubes (CNT), as well as polymers are also compared in this publication. Such approaches may be good candidates for IC shielding and enclosure in 3D stacking of active layers such as Hybrid Memory Cubes. At IC interconnect level, Multi-Wire Carbon Nano-Tubes (MWCNT) interconnects prove to provide more important crosstalk effects reductions as for conventional copper [22].

### b. Optimized die placement to reduce near-field coupling

Parasitic coupling between nearby devices can also be solved by an optimized placement between noise source and victim circuits. This solution is costless as no extra shielding layer or filter is required. This strategy is also interesting to reduce near-field coupling within 3D system-in-package assemblies. The selection of the optimized placement of dies relies on electric-electromagnetic co-simulations to determine the minimum separation distance, orientation and stacking orders. The first research works have been done around 2010 to investigate near-field coupling between power and sensitive analog IC, such as in [23], [24] and [25]. More recently, a similar work has been presented in [26] in order to select the best placement of two PoL voltage regulators mounted in the same package than a huge digital circuit in order to reduce electric field coupling. Placing voltage-regulator on the top of the assembly rather than on the bottom divides by three the amount of electric field coupling.

### c. Reduction of TSV - substrate coupling in 3D ICs

As TSV constitutes a key element of 3D integration of ICs, many research works about their modeling have been published since 2010 [27]. An important problem from an EMC point of view is the TSV to Si substrate coupling and numerous papers deals with the modeling of this issue. For example, in [8], the authors propose an equivalent electrical model of a TSV which takes also into account the non linear behavior of its parasitic capacitance due to the Si substrate effects. Their model improves the accuracy of the computation of the coupling between TSV and nearby active devices and, thus, helps to implement noise mitigation techniques.

Other publications focuses on design rules to reduce TSV noise coupling, such as [28] where the effects of ground network inductance and distance between noise source and victim are evaluated according to the substrate type (Si, Ge, Ga-As, Hg-Cd-Te). In [29], the authors proposes an original techniques to suppress vertically propagated noise between 3D ICs, by forming a periodic shielding structure based on a ground TSV array. Compared to the conventional guard ring techniques, the isolation improvement ranges from 20 to 50 dB between 10 MHz and 50 GHz.

## d. Filtering

Filtering is another traditional approach to mitigate emission disturbance propagation and new techniques are continuously developed to adapt them to new devices or improve their integration. Switched-mode power supplies, power inverters and digital lines are major contributors of conducted and radiated emission in electronic systems and huge efforts are brought to develop integrated filters in order to increase their insertion loss. For example, silicon-based integrated passive device (IPD) process can be used to design miniature EMI filter which can be easily integrated into high-speed digital ICs. In [30], an IPD differential bridged-T coils is designed as a common-mode rejection filter. With a size of 3.71 mm by 1.86 mm, the filter provides a noise rejection of more than 20 dB up to 8 GHz.

Another popular research topic is related to the design of active EMC filters to reduce the size due to conventional EMI passive filters. Thus, many research works have been published on this topic these last years. Recent examples of implementation of active EMI filters can be found in [31] and [32].

In [33], an original active common mode (CM) EMI filter, called Predictive Pulsed Compensation (PPC), is presented. This filter reinjects a pulse during the switching of a DC-DC converter to compensate the pulse responsible of common-mode conducted emission, showing reduction of 20 dB of conducted emission up to 10 MHz. Compared to previous active EMI filters, this solution does not require analog components or digital-to-analog converter, but only an extra power half bridge, which reduces its cost and improves its robustness. Similar solution is presented in [34] where a cancellation inverter is added to a three-phase inverter to suppress common-mode emission. In [35], an approach called Adapted Harmonics Cancellation is introduced to cancel electromagnetic emission produced by stationary clocked systems. Common-mode noise reduction may also be achieved by parasitic capacitance cancellation, as demonstrated by Zhang [36] in the three-phase inverter device for solar panel power management.

Careful positioning on on-chip and on-package capacitors is a very efficient technique to provide wide-band filtering. Several papers have been presented at EMC Compo Haining 2019 [37] on this topic, with filtering efficiency up to 10-20 dB. Significant emission reduction using field cancelation may be also be obtained by smart design on embedded inductances, as planar Honeycomb-based Inductor proposed by [38].

## e. Spread Spectrum

Spread spectrum modulation is a well known technique to reduce electromagnetic emission produced by fixed clocked device (PLL, PWM driver, DC-DC converter, class-D amplifier) and measured by EMI receiver. Regular improvements of this technique are provided by researchers and engineers. A review of Spread-Spectrum-Based Pulse Width Modulation (PWM) techniques has been published by [39]. The optimal spread of energy was obtained by chaotic profiles of the clock frequency variations, enabling the harmonics of the clock signal to be reduced around 20dB as compared to purely fixed clock frequency (Fig. 15).

In [40], the authors presents a similar technique but based on frequency hopping. Implemented in a DC-DC converter IC and combined with deadtime control, this technique reduces by 13 dB the radiated emission of the circuit.

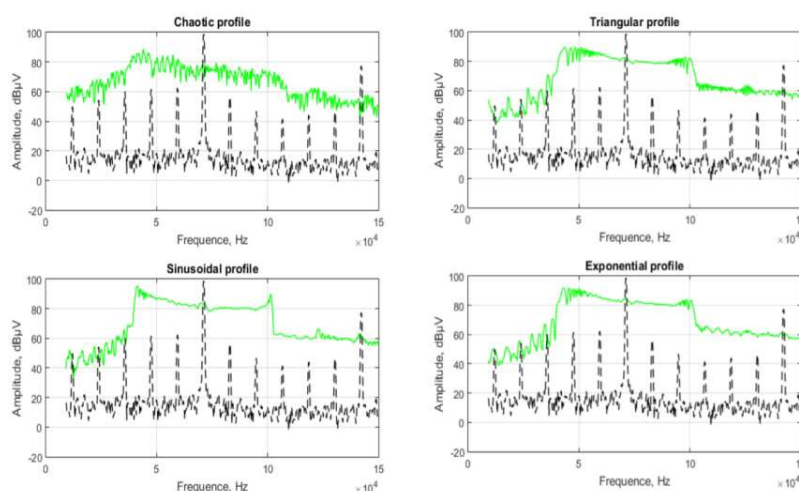
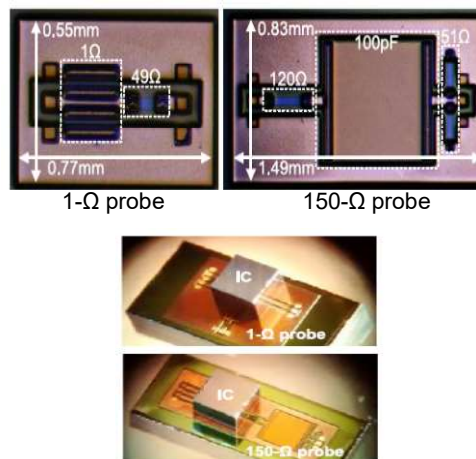


Fig. 15 - Review of Spread-Spectrum-Based PWM Techniques [39]

#### f. More accurate and faster measurements for EMC of ICs

The first standard EMC measurement methods dedicated to ICs, IEC61967 and IEC62132, were published at the beginning of 2000's. The purpose is to offer accurate and repeatable experimental techniques to characterize both conducted and radiated emission and susceptibility of ICs. Regularly, new methods or improvement of the existing methods are published in order to extend their frequency range, improve their accuracy and adapt them to new configurations.

IEC61967-4 standard, called 1- $\Omega$ /150 $\Omega$  probe, describes the most usual method to characterize conducted emission from ICs. Usually, a small network made of passive is mounted on a test board close to the circuit under test. Despite its simplicity, the main drawback is related to the stray elements of passives and PCB traces which limit the bandwidth of the measurement system to 1 GHz. In [41], a compact chip probes realized with the integrated passive device (IPD) technology is presented in order to extend the bandwidth of 1- $\Omega$ /150 $\Omega$  probe. As shown in Fig. 16, the IC under test is directly mounted on the probe, reducing the stray elements. With probes with 0.55 mm $\times$ 0.77 mm and 0.83 mm  $\times$  1.49 mm dimensions, a bandwidth of 15 GHz is reached.

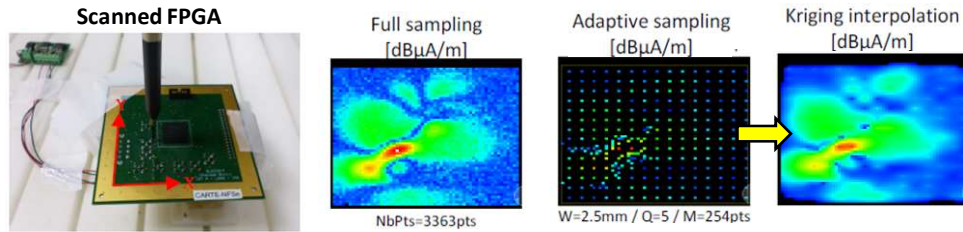


**Fig. 16 - 1  $\Omega$  and 150  $\Omega$  chip probes designed in IPD process (top) and mounting close to the IC under test [41]**

IC stripline method (IEC 61967-8) has been introduced nearly ten years ago to improve the sensitivity of TEM cell radiated emission and immunity measurements. Improvements have been proposed these last years. For example, a test structure for the EMC characterization of small integrated circuits has been proposed, which consists of the TEM and IC stripline method adaptation to very small packages [42] to measure emission and susceptibility using standardized methods. Also concerning the TEM and IC-Stripline, Fang [43] proposed a rotating test board to extract the electromagnetic radiated emission of ICs not only in 0, 90°, 180° or 270° as stated in the standard, showing that maximum power is not always matched with these angles. One important constraint of the IC stripline design proposed in IEC 61967-8 is the VSWR requirement, which is difficult to reach when heatsink or metallic cans are mounted on ICs. In [44], the design of IC stripline to overcome this issue.

Near-field scan has become a popular technique for the analysis of IC emission and susceptibility issues for nearly twenty years and numerous research works have been done on this topic, especially on near-field probe design for scan at IC level. Yan [45] proposes novel designs of noncontact wideband current probes which provide more precision and resolution than commercially available probes upto 10 GHz. In [46], a classical monopole coaxial-based E field probe is used but an absorbing material is introduced to suppress common-mode current that circulates on the outer surface of the probe and degrade measurement seriously. This probe captures successfully the vertical electric field around an IC heatsink up to 10 GHz in order to predict far-field emission.

One drawback of near-field scan is related to the long measurement time since electric and magnetic must be captured in the vicinity of the IC under test over several hundreds or thousands positions. In [47], an original sequential adaptive sampling algorithm is proposed to reduce the measurement time of near-field scan. Based only near-field probe dimension and scanning height, the algorithm decides if a measurement must be done or not on a given point. Applied for the near-field scan measurement over a FPGA, the paper shows a division by nearly ten of the measurement time without any significant loss of accuracy (Fig. 17).



**Fig. 17 - Illustration of a magnetic near-field scan reconstructed according to sequential adaptive sampling algorithm presented in [47]**

### g. Anticipating IC Emission

Modeling approaches as promoted by IEC standard 62433 (ICEM) [11] have led to several publications, such as [48] which explains how to build the internal activity block (referenced as IA in the standard) for conducted emission prediction, without complex and inaccurate experimental extraction process. Deterministic or statistical approaches for evaluating the internal activity of an FPGA have been described.

The analysis of the Power Distribution Network (PDN) in 3D ICs using TSVs has been performed by [49] combining both transient current estimation and thermal management thanks to electrothermal simulation. Specific hot-spots in 3D structure have been detected, in relation to 20-40 GHz resonance effects in the PDN.

Another critical aspect of anticipating emission is the ageing of components. Ghfiri [50] proposed a methodology for EMC Prediction of Integrated Circuits after aging using thermal cycling combined with voltage stress to accelerate the degradation of IC, measuring and modeling the degradation of Ring Oscillator frequency and the overall reduction of conducted emission. Most of publications related to IC emission are related to power integrity and conducted emission simulation, but IC radiated emission is seldom dealt. In [51], the authors presents a coupling model of an IC mounted in a wire bonded BGA and the IC stripline in order to predict the emission level measured with this method. The method is based on a 3D electromagnetic solver (FEM) combined with SPICE simulation.

### h. IC immunity prediction

Immunity is a big concern for IC and electronic equipment manufacturers so that huge efforts are brought to develop IC modeling and simulation techniques for the prediction of susceptibility. Semiconductor industries have developed proprietary simulation environment to predict the susceptibility of their own circuit for nearly ten years. A recent simulation environment, called electromagnetic compatibility qualification environment (EQE), is presented in [52]. It aims at predicting susceptibility level of custom digital circuit to DPI and BCI tests at the schematic level and postlayout level.

However, such approaches which requires proprietary design kits and standard cell models are not adapted for the need of IC end-users. IEC62433-4 ICIM-CI (Integrated Circuit Immunity Model - Conducted Immunity) standard has been developed to offer a non-confidential behavioral macromodel of ICs for conducted immunity prediction. Although the first demonstration of this model has been done at the end of 2000's, the model is not completely mature and widely accepted. Recent research works have been led to reinforce this approach. In [53], the ICIM-CI model of a voltage regulator is built to simulate the rectification of incoming disturbance which introduces DC offset at the regulator output. The paper presents the different step to build the two main subblocks of the model: the passive distribution network (PDN) block and the immunity behavior (IB) block. The proposed model is in good agreement with measurement result and can predict variation of immunity when external filter is introduced.

In [54], an equivalent immunity model of voltage regulator based on DPI test results is coupled with the result of the electromagnetic simulation of BCI test bench. The model reproduces the failures observed experimentally. A similar approach is presented in [55] to simulate failures of a capacitive touch sensors during BCI test.

Comparable approach based on simple measurement to build rapidly a generic immunity model of several op-amps is presented in [56]. In spite of some inaccuracies in the simulation results, the model is able to reproduce the general immunity behavior up to several hundreds of MHz and is sufficient to select the correct component and design an appropriate EMC filter.

ICIM was also used to simulate the radiated immunity of IC mounted in SOIC packages in [57]. The authors show that the dominant coupling mechanisms of disturbance is the conducted mode up to 10 GHz, i.e. the radiating disturbance couples on PCB traces before being conducted to IC pins. Prediction and GTEM measurement of the radiated immunity of a 5 cm trace and an LM7805 voltage regulator have been compared with good agreements. The prediction was based on the extraction to the IB block for a given voltage output failure criterion.

Immunity of IC to transient disturbances, e.g. ESD, is another important concern for electronic equipment manufacturers, especially for automotive and mobile equipments. Simulation constitutes the only method for designers to anticipate failures

and, sometimes, understand why failures arise as it is highlighted in [58]. In this paper, the authors characterize and compare the susceptibility to ESD of three LIN bus drivers separately. However, when these different drivers are mounted on a same network, the observed failure and susceptibility level is extremely dependent of the combination of components. The analysis of the measurement results shows that susceptibility level of a driver in a bus configuration is not completely related to the susceptibility level measured in stand-alone configuration. The authors underlines the essential role of IC modeling and simulation to help designers to clarify such situation.

Full-wave simulation has been used by [59] to analyze the system-level disruption of a smartphone during ESD events. Model-order-reduction algorithms have been used to avoid handling the 5-billion initial mesh to 8 million. The discharge current & victim noise could be predicted and compared to measurements. Similarly, Koch [60] identifies soft failure mechanisms triggered by ESD Stress on a powered USB 3.0 Interface and characterizes the types of software failures observed in the communication bus.

Another important aspect of immunity prediction is the robustness to data injection attacks. Kaji [61] uses a log-periodic antenna at 2-m distance to provoke changes in electrical signals equivalent to the communication between UARTs. Information security threats were also demonstrated on Ring-Oscillator-based True-Random Number Generators by S. Osuka [62]. EMC countermeasures such as ferrite cores, or dynamic analysis of the load impedance have been outlined and may be able to prevent from intentional interference.

### i. Choice of components

Choosing components based on EMC criteria is one practical approach to enable EMI-hardened designs. Pouant [63] has analyzed 2 MOS references BSS83 and 3N170 which were compared in terms of rectifying effects when disturbed by conducted electromagnetic interference within the 1 MHz – 3GHz bandwidth. A comparative study between standard and EMI-Hardened Operational Amplifiers from Texas Instruments has been conducted by Boyer [Boyer, 2019], showing superior robustness to direct power injection on differential inputs or outputs, and consequently larger EMI Rejection Ratio (EMIRR) as demonstrated in Fig. 18.

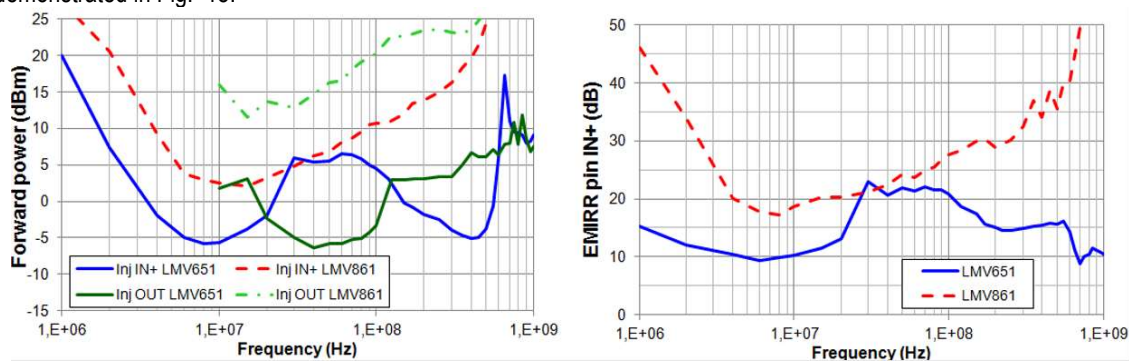


Fig. 18 - Superior EMI rejection ratio for EMI-hardened Operational Amplifiers compared to standard references [56]

## 9. Conclusion

This paper has introduced the main current trends of semiconductor market, highlighting the global growth of the market, driven by forces such as the increase in complexity, decrease in voltage supply, gains in data rate for exchanges between ICs and the move towards 3D implementation. We also highlighted the effects of technology trends on electromagnetic issues such as emission, susceptibility, signal integrity and power integrity. As these driving forces should lead to degradation of electromagnetic emission and susceptibility, it forces IC designers to provide continuous efforts to develop low emission and noise immune ICs. Based on recent publications published these last three years, we listed some interesting contributions to reduce parasitic emission and susceptibility to radio-frequency interferences. These contributions improve some existing approaches, extend frequency limits or propose radically new techniques to measure, predict or solve EMC issues. With the on-going development of new market demanding high performance ICs (e.g. autonomous cars, 5G), we can bet that EMC will remain a major concern for IC designers and an exciting research subject.

## About the authors



Professor Sicard is currently a professor in the Department of Electrical and Computer Engineering at INSA, an engineering school part of the University of Toulouse, France. He is associate researcher at IRIT laboratory, and research director at LURCO laboratory. Granted the Monbusho scholarship award, he conducted post-doctoral studies at Osaka University, Japan (1988-1989). He received a B.S degree and a PhD in Electrical Engineering from the University of Toulouse, France, in 1984 and 1987 respectively. He was elected Distinguished IEEE Lecturer of the EMC society for 2006 -2007. Professor Sicard has authored or co-authored over 20 books, 10 commercial software packages (Microwind, IC-EMC, Vocalab, Diadolab) and more than 250 technical papers in a many areas of electrical engineering, including nano-scale CMOS technology, integrated circuit design automation and digital signal processing for speech therapy. He is the founder of EMC Compo international workshop ([www.emccompo.org](http://www.emccompo.org)) focused on Electromagnetic Compatibility of Integrated Circuits.



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