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# Zero sequences optimizing different criteria for three-phase multilevel inverters

Bernardo Cougo  
 MEA department  
 IRT Saint-Exupery  
 Toulouse, France  
 bernardo.cogo@laplace.univ-tlse.fr

Thierry Meynard and Guillaume Gateau  
 LAPLACE  
 University of Toulouse  
 Toulouse, France  
 thierry.meynard@laplace.univ-tlse.fr

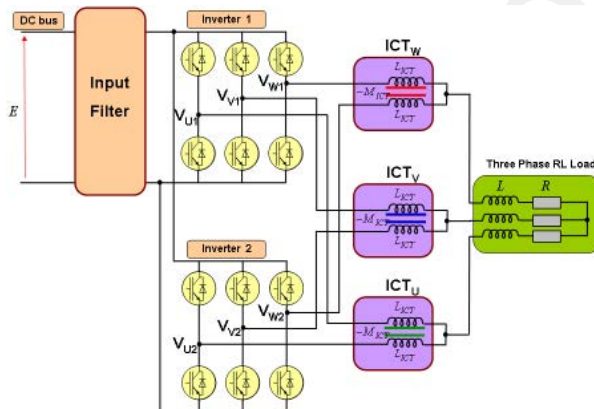
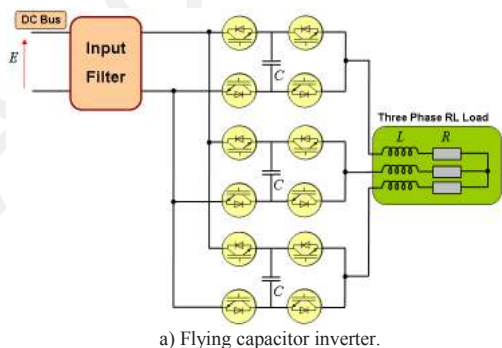
Lenin M. F. Morais  
 Departamento de Engenharia Eletronica  
 Universidade Federal de Minas Gerais  
 Belo Horizonte, Brazil  
 lenin@cpdee.ufmg.br

**Abstract**—In a world with growing concern for efficiency, power electronics associated to high level control techniques are more and more used in different fields of application. One of the most common applications are three-phase machines fed by three-phase inverters to tune precisely the power consumption. In recent years, multilevel inverters have become the best solution to address the problems of high voltage, high current or high efficiency. PWM modulation strategies play an important role in the design of such converters and one may choose adequate carriers and zero order signals in order to improve the design of an important component of the system. Some PWM methods found in the literature minimize some key elements of three-phase systems, however when multilevel converters are considered, little is found. The aim of the paper is to present a simple but powerful approach which allows us to determine optimal zero sequence signals (also called Common Mode Offset, CMO) corresponding to any desired objective for many different topologies. It will be shown that some widely accepted PWM methods as well as new optimal methods are found by this method. These PWM methods will be compared by means of simulation and some CMOs created using our approach are validated by experimental results.

**Keywords**—PWM methods, three-phase inverter, series and parallel multilevel inverters

## I. INTRODUCTION

Three-phase Voltage Source Inverters (VSI) are one of the most common systems found in the industry. When dealing with high bus voltages, multilevel series converters such as the 3-level flying capacitor inverter of Fig. 1a may be used. If the load requires high currents, a better option is to use a parallel converter such as the 3-level parallel inverter of Fig. 1b in which commutation cells are connected in parallel by InterCell Transformers (ICTs). Irrespective of the voltage and current requirements, multilevel converters are a good option for high efficient and compact converters [1].



b) Parallel inverters connected by ICTs (interleaved converter).

Fig. 1. Three-level series and parallel inverters.

Nowadays multilevel converters are a well-established and attractive solution to the industry although we may find in the literature many works related to the improvement of the current ripple [2][3], the THD of the output signals [4][5] or the balancing of the DC capacitor voltage [6][7].

If we take the system containing the parallel inverter of Fig. 1b as the reference for our analysis, we may define an optimized system as the one having all 4 main blocks (input filter, semiconductors, output filter and load) optimized according to a certain objective, such as the minimization of the volume, weight, price or efficiency. Many parameters of the system may influence all 4 blocks in different ways. One of these parameters is the PWM method used to control the commutation cells.

PWM methods may be divided in two different types: carrier-based methods and zero sequence injection methods. We focus in the latter methods although both may be applied to parallel and series multilevel converters. In order to identify which commutation cell will switch at a certain time, a state machine may be used as it is usually done in series multilevel converters to control the voltage balance in capacitors [8]. In parallel converters the state machine would be useful to control, for example, the flux inside the ICT.

We present here an approach to create zero sequence signals (also called Common Mode Offsets, CMO) which are optimal for certain blocks or even for all of them at the same time. The system of Fig. 1b will be used as a reference but the approach may be used in any three-phase system to find optimal CMOs for different objectives. Some of the optimal CMOs found by the developed algorithms were already analytically presented in the literature and this validates the approach proposed here. Other optimal CMOs are new and

they may be used in many different applications. Comparisons of some developed PWM methods with the most famous ones are performed in order to show the gain either in the input filter, semiconductors, output filter or load. Experimental results confirm the analysis presented here.

## II. INJECTION OF ZERO SEQUENCE SIGNALS

A common mode offset may be applied to the references of the three phases of a three-phase system without affecting the load current at the fundamental frequency, in the cases where the neutral point is not connected to the ground or to the middle point of the inverter's DC bus. This degree of freedom was initially used in inverters in order to increase the linearity range of the output voltage [9] and later to reduce the THD of the output current or to reduce switching losses in the converter.

There are some different zero sequence signals which have gained wide acceptance not only in the literature but also in the industry. They are usually separated in Continuous PWM (CPWM) and Discontinuous PWM (DPWM). CPWM modulation waves are always strictly within the boundaries imposed by the triangular carriers while DPWM references can vary outside carrier bands resulting in output voltage clamped to the positive and/or negative DC rail. Clamping can be obtained for at most 120° of the reference wave in each phase without any low frequency distortion of the output voltage.

Zero sequence signals (green lines) considered for comparison are shown in Fig. 2 along with the sinusoidal reference (blue lines) and the reference after the zero sequence injection (red lines), at modulation index ( $M_i$ ) 0.8.

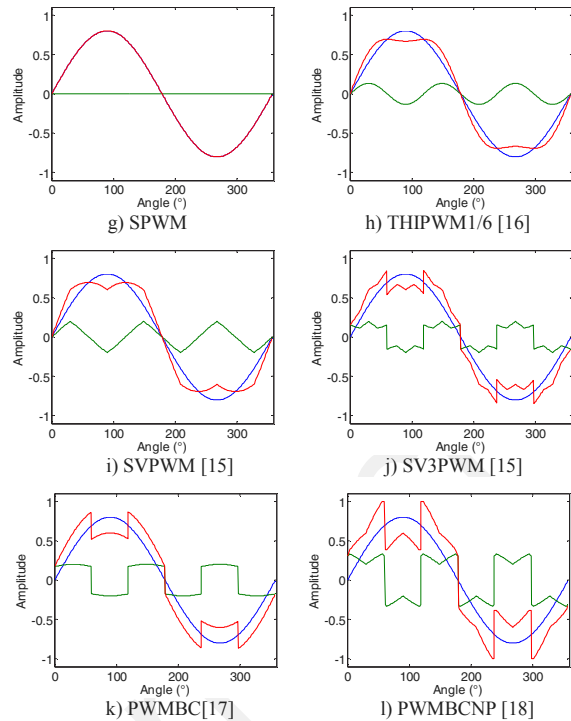
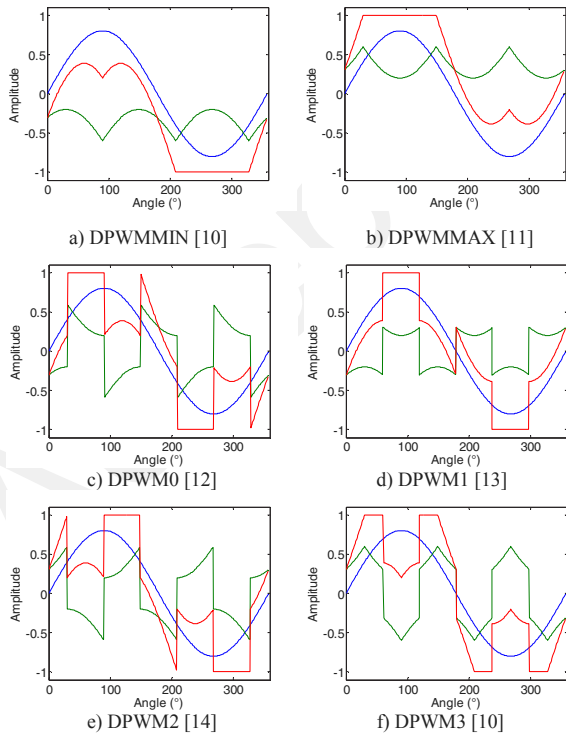


Fig. 2. Zero sequence signal (green lines), sinusoidal reference signal (blue line) and modified reference signal with zero sequence (red lines) for different PWM method, at  $M_i=0.8$ . Methods a) to f) are discontinuous methods while g) to i) are continuous.

As shown in [19], several zero sequence signals have been introduced to match the requirements corresponding to different fields of application and optimize various criteria: simplicity in the implementation, computational efficiency, high voltage linearity range, low output voltage distortion, switching losses reduction and etc. In multilevel converters, zero sequence can be used to reduce the capacitor voltage unbalance (series inverter) [20] or the ICT flux (parallel inverter) [17][18]. As examples of the influence of different CMOs, we show in Fig. 3 the magnetic flux in the ICT of phase U shown in Fig. 1b. In Fig. 4 we show the output current ripple in this phase, for two different CMOs, for a given modulation index ( $M_i=0.7$ ). Note that both the ICT flux and the output current ripple are very different when injecting different zero sequence signals.

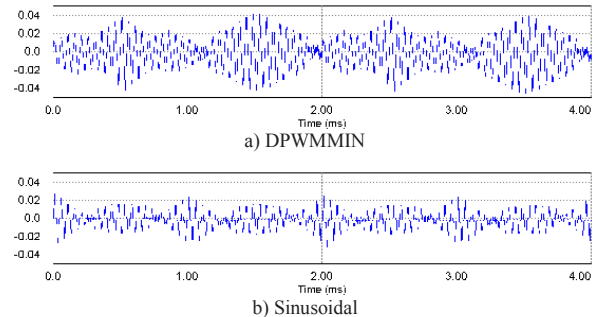


Fig. 3. ICT flux waveform for different CMOs.

Obviously, minimizing the ICT flux will lead to a smaller ICT design the same way that minimizing the output current ripple reduces the losses in three-phase motors. That is why it is important to find an optimal CMO which minimizes one

of these values, or a criterion involving all the design of the system composed by the input and output filters, semiconductors and load. Next section will explain the approach used to create optimal CMOs.

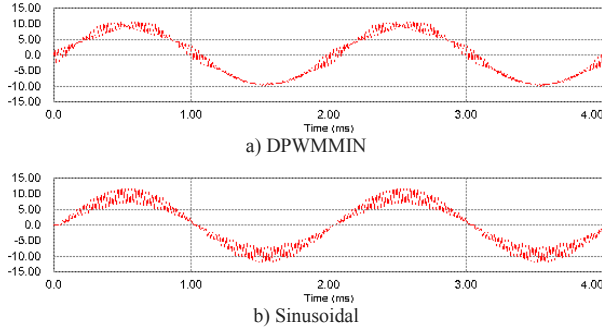


Fig. 4. Output current ripple for different CMOs.

### III. CREATION OF OPTIMAL ZERO SEQUENCE SIGNALS

First we will show how to create an optimal CMO regarding the magnetic flux in the ICT of Fig. 1. Later, the approach will be generalized.

The flux inside this ICT depends basically on the current flowing through each winding of the ICT ( $I_{X1}$  and  $I_{X2}$ , where  $X = U, V, W$ ), the number of turns of each winding ( $N_i$ ) and the core reluctance ( $RelCore$ ). Neglecting the series resistance of ICT windings, the flux will only depend on the integral of the voltage difference between each phase, and also on the mutual and self inductances of the ICT ( $M_{ICT}$  and  $L_{ICT}$  respectively), as shown in equation:

$$\phi_s = \frac{N_i}{RelCore (L_{ICT} + M_{ICT})} \int (V_{X1} - V_{X2}) \quad (1)$$

In order to find the optimal CMO, the idea is to create an algorithm which adds an offset to the 3 reference signals and to calculate the maximum flux ripple in the 3 ICTs for each angle in each modulation index. Only a range of  $120^\circ$  needs to be calculated since it is a three-phase system. By sweeping all possible offsets it is possible to find for each angle the offset giving the lowest value for the maximum peak flux (maximum among the 3 phases), and such an optimal zero sequence can be found by recomposing these offsets for each angle and for each modulation index. The algorithm is schematically presented in Fig. 5.

To precisely find the optimal CMO a great number of points in the carriers is needed as well as a great number of angles and modulation indexes. The number of offsets to be swept is the factor which most limits the accuracy of the resulting CMO. The use of complex optimization routines could improve accuracy and reduce computational time. However, the problem presented here is not computationally heavy since only one variable (offset) is varied for each possible angle and modulation index. This routine must only be run once per criteria to be optimized and thus no complex optimization routine is necessary.

This algorithm applied to the problem of the flux in the ICTs of Fig. 1b gives the optimal CMOs shown in Fig. 6 for modulation indexes from 0.1 to 0.9.

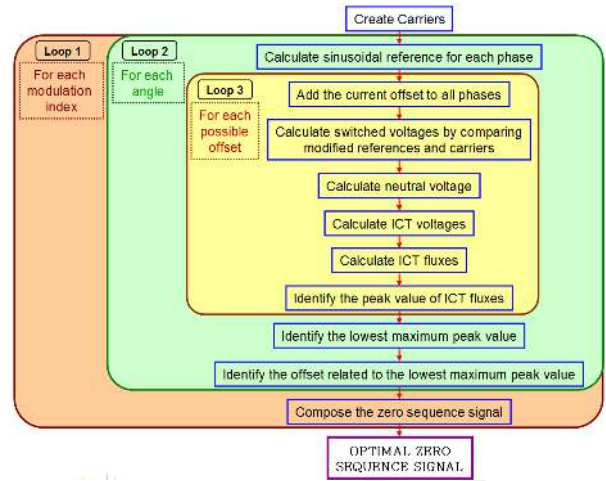


Fig. 5. Scheme of the developed algorithm.

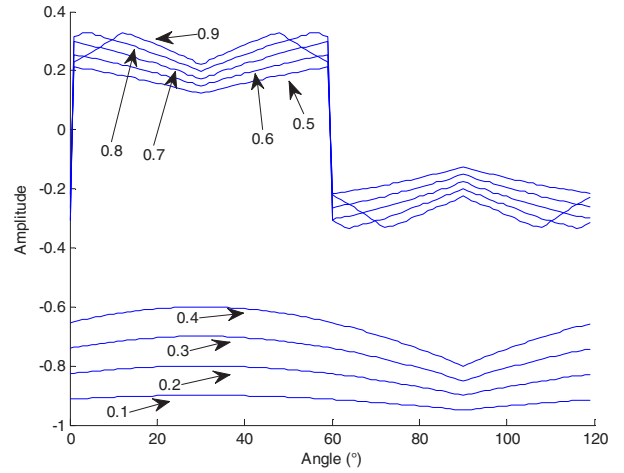


Fig. 6. CMOs minimizing the ICT flux for different modulation indexes.

These curves may look a little strange but they are exactly the same as PWMBCNP, the optimal PWM method shown in [18], which was found by graphical analysis of the ICT flux ripple. For low modulation indexes, the optimal CMO is equal to any DPWM. For high modulation indexes it is equal to half the reference which has neither the greatest nor the lowest absolute value.

#### A. Multiple Optimal CMOs

There are several cases where more than one CMO may be the optimal one. It means that many different offsets may be added to the references and the result is always the maximum reduction of the calculated value (which is the ICT flux ripple in the example above). In these cases, the algorithm proposed in this paper may find very strange zero sequence waveforms because for each angle, it will choose the offset corresponding to the minimum numerical value of the minimization variable. For this reason, a better way to find an optimal CMO is to plot all the offsets which generate a calculated variable very close to the minimum numerical results.

In order to clarify this idea we will use an example based on Fig. 7. In this circuit we have a double three-phase motor fed by 2 three-phase inverters coupled by 3 ICTs. The ICT



flux calculation is a little bit different from equation (1) since it also depends on the integral of the difference of neutral voltages. Using the PD strategy and the algorithm shown in Fig. 5, we may produce the graphs shown in Fig. 8 where we plot, using yellow circles, all offsets which generate a maximum flux ripple smaller than 1.01 times the minimum numerical maximum flux ripple. This is done for different modulation indexes.

This figure shows that for modulation indexes ( $M_i$ ) lying between 0.1 and 0.6, any discontinuous PWM technique can be the optimal one. However, after  $M_i=0.7$ , the minimum and maximum offsets are not anymore the optimal ones. It means that the optimal CMO is either a specific combination of the minimum and maximum offsets, i.e. a specific discrete PWM, or a continuous PWM which crosses the zero line each  $60^\circ$ . Or even no offset at all!

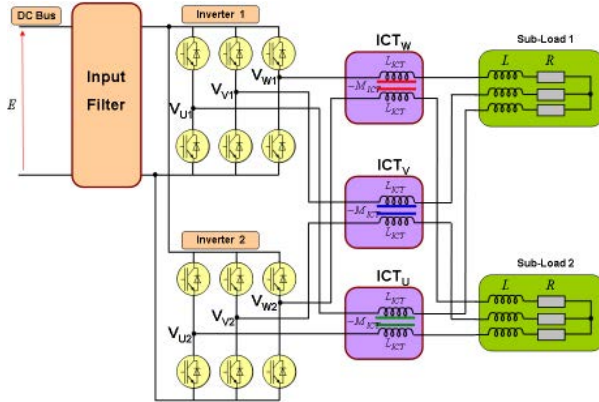


Fig. 7. Double inverter feeding a double three-phase load.

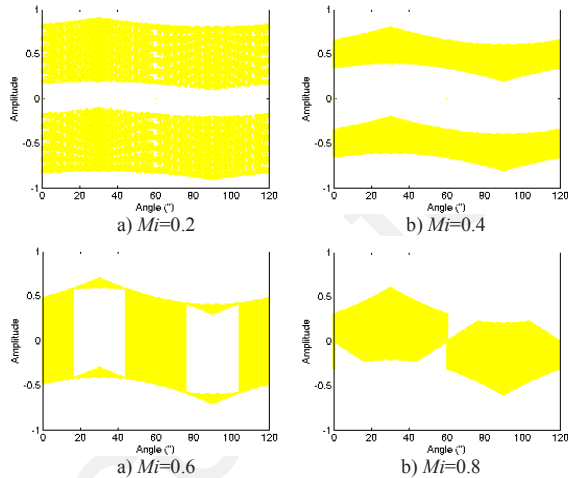


Fig. 8. Offsets where the maximum flux ripple is close (1% difference) to the minimum numerical solution.

#### IV. OPTIMAL ZERO SEQUENCE SIGNALS FOR DIFFERENT CRITERIA

Until now, we have only shown the creation of optimal CMOs with regard to the minimization of the high frequency magnetic flux of ICTs coupling parallel inverters. As mentioned before, the same approach may be used to optimize other criteria, such as the load losses, the semiconductor losses or the input filter size.

#### A. Optimizing Load Losses

It is well explained in the literature that losses in motors fed by inverters can be minimized using Space Vector Modulation (SVM) [21]. Later the equivalence between SVM and carrier-based modulation was demonstrated [21][22][23], for 2-level and multilevel converters. The reduction of the harmonic content of the output current is obtained by using PD strategy associated to specific zero sequence signals, such as those shown in Fig. 2i and Fig. 2j, for the 2- and 3-level cases respectively. Harmonic content is usually evaluated in the literature by the figure of merit called Weighted Total Harmonic Distortion (WTHD). We prefer to evaluate and compare PWM methods by the RMS value of the harmonics of the output current. This concept was already used in [21] and is independent of the switching frequency ( $F_s$ ) and modulation frequency ( $F_{mod}$ ) if we suppose that their ratio ( $F_s/F_{mod}$ ) is high.

In order to find the optimal CMO for this case, the approach described in Fig. 5 may be used with little modification. In the innermost loop, instead of calculating the flux by the integral of the voltage difference, we need only to replace it by the calculation of the integral of the sum of two voltages. The result is the output current ripple. What we need now is to identify, for each angle and each modulation index, which are the offsets minimizing not the peak value of this current, but the peak value of the sum of the currents of the three phases. This guarantees a minimum RMS current of the harmonics for the whole modulation period and modulation index range.

The CMOs found by the algorithm of Fig. 5 applied to the minimization of the RMS harmonic current are shown in Fig. 9. In this figure, we also use yellow circles for all the offsets which generate a RMS current smaller than 1.01 times the minimum numerical RMS current. Note that, even using a coarse resolution (100 possible offsets), these CMOs are very close to the ones found in the literature [21][22][24], which were also plotted for comparison (red lines).

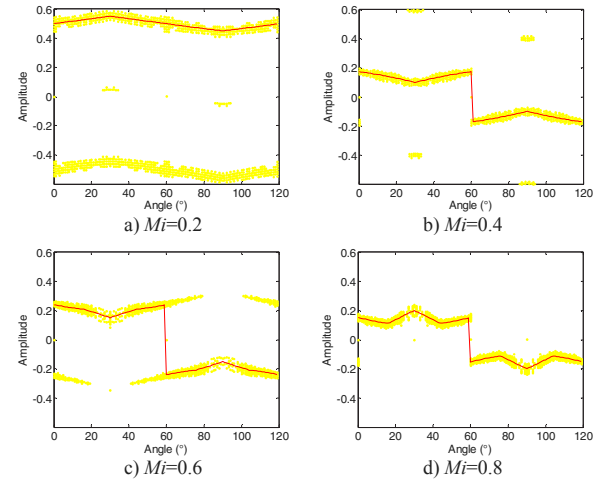


Fig. 9. Optimal CMOs for minimization of load losses.

The gain of using the optimal CMO instead of any other PWM method may be evaluated by calculating the normalized RMS value of the harmonics of the output current ( $I_{hmRMS}$ ) for all methods. The RMS value of the real harmonic current can be calculated as

$$I_{hRMS} = I_{hnRMS} \frac{E}{F_s L} \quad (2)$$

where  $E$  is the DC bus voltage,  $F_s$  is the switching frequency and  $L$  is the load inductance.

Comparison between all methods is shown in Fig. 10. It is clear that SV3PWM produces much less current ripple than any other PWM method. If the load is a motor, copper losses in the winding are reduced as well as magnetic losses.

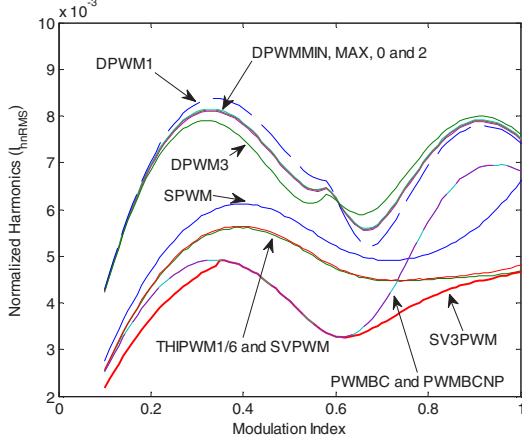


Fig. 10. Comparison between PWM methods with regard to the output current ripple.

### B. Optimizing the Semiconductor Losses

The approach described in Fig. 5 must be further modified to find optimal CMOs reducing switching losses in the semiconductors of the inverters. If the converter is composed by IGBTs, switching losses are calculated by determining the IGBTs' turn-on and turn-off energies ( $E_{on}$  and  $E_{off}$  respectively) and the diode's reverse recovery energy ( $E_d$ ) at each switching instant. Losses are calculated by integrating all the energies over the modulation period. Switching energies are usually calculated by using curves given by manufacturers or by reference values determined by manufacturers at certain conditions and assuming that switching energies are proportional to the switched voltage and current.

Thus, in order to find the optimal CMO, information about the fundamental of the output current is necessary. Actually, for comparison purposes only the phase between the output current and the voltage reference is needed.

Modification of the algorithm of Fig. 5 is made as follows: calculation of the switched voltage is not necessary. For each modulation index and for each angle of the voltage reference (this time from 0 to  $2\pi$ ), we identify the two phases corresponding to the two references having the greatest absolute values. The offset is equal to:

$$Offset = (1 - abs(v_x^*)) \cdot sign(v_x^*) \quad (3)$$

where  $v_x^*$  is the reference corresponding to the phase having the greatest absolute value of the current (among the two phases identified above). With this offset, one phase will be held to the positive or negative rail and, like this, there will

be no switching in the phase which would have the highest losses.

### C. Optimizing the Input Filter

Zero sequence injection can also be used to reduce the size of the input filter, which may be composed by a simple capacitor in the DC bus or a more complicated circuit. Many parameters may influence the size of this filter and so many criteria may be minimized. We will explain here the minimization of the RMS value of the input current, which is a key value to the filter design.

We may use the algorithm in Fig. 5 with little modification. Information about the fundamental value of the output currents is needed since the input current is a combination of the 3 output currents, modulated by the commutation cells. As a consequence, in the inner loop of Fig. 5, instead of calculating the flux by the integral of the voltage difference, we just sum the currents in the 6 phases, each one multiplied by the switching signal of its corresponding phase. The result is the input current waveform, for each angle of the sinusoidal reference and for each modulation index. As made for the other cases, we need to identify, for each angle and each modulation index, which are the offsets minimizing the RMS value of the input current. This guarantees a minimum RMS value of the current harmonics for the whole modulation period and modulation index range.

Since the input current harmonics depend on the output currents, the optimal CMO depends on the phase difference between the output currents and the references. In Fig. 11 we show the result of the algorithm for six different angles ( $\sigma$ ) between the output currents and the references, at modulation index equal to 0.7 and POD strategy.

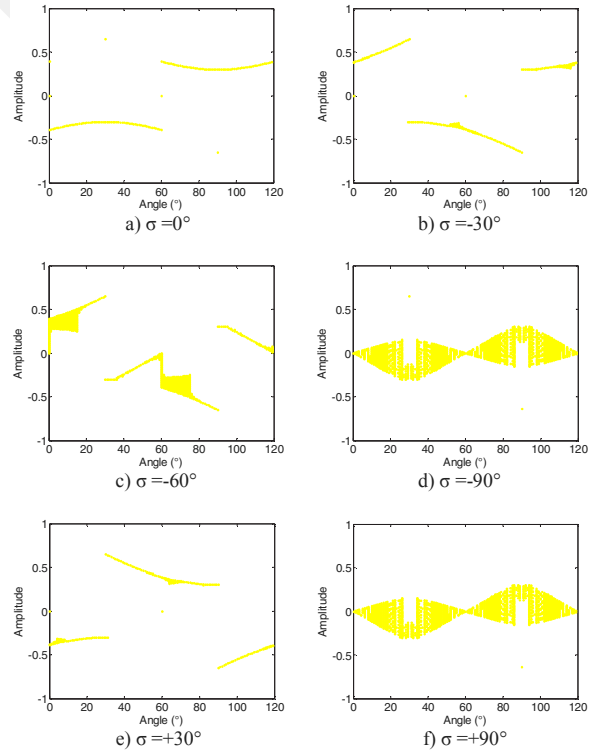


Fig. 11. Optimal CMOs for minimization of input RMS current, at different angles between the output current and references ( $M_i=0.7$ ).

For this example and specifically for the angle  $\sigma = 0^\circ$ , DPWM1 was found to fit inside the optimal CMOs for all modulation indexes.

To show the reduction of the RMS input current by applying the optimal CMOs found by the algorithm, we show in Fig. 12 the RMS value of the input current applying different PWM methods, when the angle between the output current and the reference is equal to  $0^\circ$ . Note that the optimal CMO (DPWM1) gives always the lowest input current, and, as a consequence, it reduces the size of the input filter.

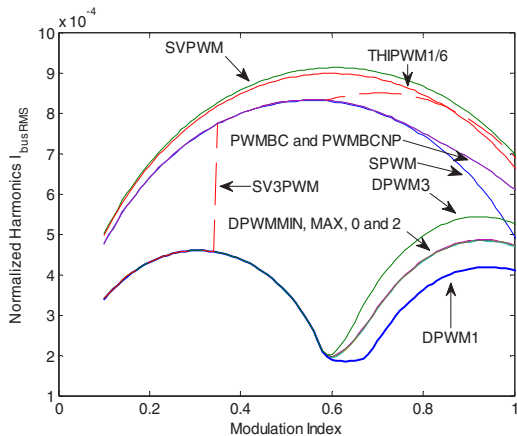


Fig. 12. Comparison between PWM methods with regard to the input current. ( $\sigma=0^\circ$ ).

#### D. CMOs in Tables

It is not always possible to find equations related to optimal CMOs. In our examples, there are equations for the optimal CMOs related to the output current, to the ICT flux and also to the switching losses (formulas derived from equation (2)). For the cases where no simple formulation of the CMO is obtained, such as the case related to the input current, lookup tables can be used.

Nowadays, most of the control of inverters is digitally made by the use of DSPs or FPGAs. Thus, it is simple to set up a table with all the values of the optimal offsets, for each angle and at each modulation index. Obviously, granularity of discretization of angle and modulation index values is important. Using larger increments in each parameter would reduce memory requirements, but could lead to unexpected behavior in hardware implementation. However, a reasonable number of angles and modulation indexes, together with interpolation techniques may result in fast calculation of needed offset and at the same time keep low memory requirements.

#### E. Optimal PWM Method for the Whole System

Until now, algorithms were developed to optimize different criteria: load losses, switching losses, ICT size, or input filter size. When designing a system such as the one in Fig. 1b, designers may be interested in reducing, for example, the size or weight of the entire system. In this case, the algorithm of Fig. 5 must be modified to include the calculation of output current, input current and switching losses. If the designers have analytical models relating these values to the weight of the ICT, the input filter, the load, the semiconductors and the cooling system, an optimal CMO can be found to reduce the global weight.

If there are no analytical models for this calculation and the system is to be optimized, these algorithms may be inserted in the optimization loop.

## V. EXPERIMENTAL RESULTS

Algorithms developed in this paper have created several optimal PWM methods, each one for a different criterion. Optimal PWM methods related to switching loss reduction and output current harmonic reduction are well known in the literature. Thus, an experimental setup was developed in the laboratory in order to validate the operation of the optimal PWM method regarding the ICT flux. The experimental system contains 2 three-phase inverters from SEMIKRON using 1200V SEMIKRON IGBT modules (SKM50GB123D) and driver SKHI 22. Each phase of each inverter is connected as the circuit in Fig. 7, except for the fact that the ICTs were replaced by two 6mH inductors. The load comprises two variable three-phase resistive loads. Each inverter is controlled by a control board composed of an ALTERA ACEX 1K100 FPGA and a TMS320C6713 Texas Instruments DSP. A photo of the whole experimental setup is shown in Fig. 13.

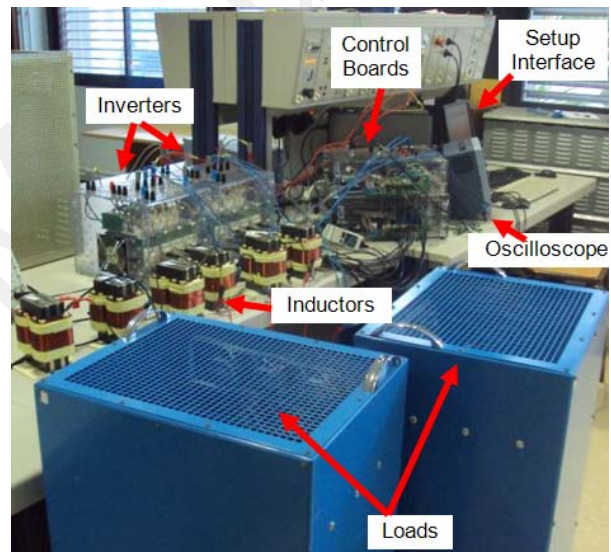


Fig. 13. Experimental setup of a double three-phase inverter to evaluate current difference between paralleled commutation cells.

By equation (1) we can see that the flux inside the ICT is proportional to the current difference between the two commutation cells of each phase, and this is true if the mutual inductance ( $M_{ICT}$ ) is low or equal to zero. Thus measuring the current difference of two inductors connected to the same phase gives us the waveform of the flux in an ICT which would be inserted in the place of these two inductors. This is confirmed by Fig. 14, where we show the simulation of the flux inside an ICT in a system having the switching frequency ( $F_s$ ) equal to 10kHz and modulation frequency ( $F_{mod}$ ) equal to 500Hz. This is compared to the experimental current difference at  $F_s=4kHz$  and  $F_{mod}=50Hz$ . Both simulated and experimental data are shown using PWMBC method.

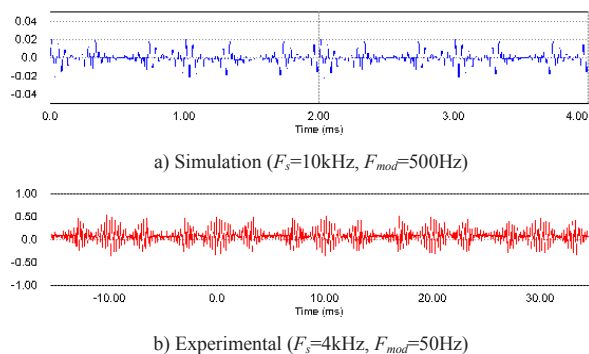


Fig. 14. Simulated and measured flux waveform for the optimal PWM method (PWMBC).

Current difference was acquired for all PWM methods and for several modulation indexes (0.1, 0.2, ..., 1.1). Maximum peak-to-peak value of these current differences is plotted in Fig. 15, where we note that the CMO created by the algorithms developed here (PWMBC) always generates lower current difference (or less flux in an ICT) than other PWM methods.

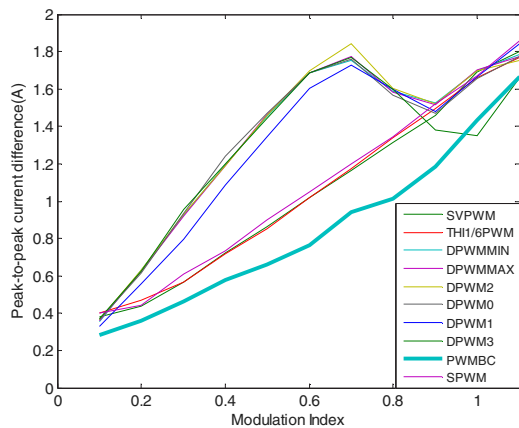


Fig. 15. Comparison of PWM methods: maximum peak-to-peak current difference obtained by experimental results.

## VI. CONCLUSION

Zero order signal injection is a technique which has been used for a long time in three-phase systems using inverters to improve some characteristics such as load voltage excursion, switching losses or output current harmonic content. It may also be used to improve the flux ripple of ICTs in parallel multilevel converters or capacitor's voltage balance in series multilevel converters.

In this paper we have presented a simple approach to generate zero order signals used to optimize any criterion related to three-phase systems. Some of the generated zero order signals were already presented in the literature as they have been analytically developed. Others were presented here for the first time, for a multilevel system composed of two inverters in parallel, connected by two-cell ICTs. Specifically, some of the zero order signals presented here allow to optimize either the input filter or the ICT design.

Since the approach presented here is as general as possible, it is a powerful tool for researchers searching for the optimization of parts of three-phase systems (input or output filter, semiconductors, load losses and etc.) or even of the entire system at the same time.

One of the optimal zero order signals found using the approach presented here was experimentally tested and compared to other PWM methods. In this specific case, it was verified that it always gives the lowest ICT flux. Experimental results match very well results issued from calculation and from simulation.

## ACKNOWLEDGEMENT

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