Demonstration of BEOL-compatible ferroelectric Hf 0.5 Zr 0.5 O 2 scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications

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Demonstration of BEOL-compatible ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications

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***Abstract*—**We demonstrate successful scalability of conventional 100µm diameter TiN/HZO/TiN capacitors down to 300nm by successfully co-integrating them for the first time in the Back-End-Of-Line of 130nm CMOS technology. Excellent performance are reported on those scaled bitcells, such as remnant polarization $2.P_R$ > 40µC/cm², endurance > 10^{11} cycles, switching speeds < 100ns, operating voltages < 4V, and data retention at 125°C. Presented results pave the way to < 10fJ/bit ultra-low power FeRAM for IoT applications.

I. INTRODUCTION

Ferroelectric HfO_2-based materials have been intensively studied since 2011 [1], thanks to their excellent CMOS compatibility and potential for scalability. So far, promising performance have been mostly reported on large area (typically 10000µm²) Metal/Ferroelectric/Metal (MFM) capacitors, with thermal budgets larger than 500°C [2,3]. Therefore, ferroelectricity on sub-1µm² capacitors with low thermal budget are yet to be demonstrated for those promising materials in order to integrate them in the Back-End-Of-Line (BEOL). Indeed, bridging the gap with PZT-based FeRAM arrays [4], for which the technology is mature but not easily scalable, is necessary for ferroelectric HfO_2 to envision practical applications requiring embedded Non Volatile Memories (NVM), Logic-In-Memory (LIM) or neuromorphic circuits. In this paper, ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) BEOL compatibility is investigated from a thermal budget, scalability, and integration perspectives, from single cells to 1T-1C arrays.

II. HZO BEOL THERMAL BUDGET COMPATIBILITY

Large area (Ø100µm) TiN/HZO/TiN capacitors were fabricated on 200mm Si substrates to first assess BEOL thermal budget compatibility. HZO is deposited by ALD with a thickness of 10nm, whereas TiN electrodes are fabricated by PVD with a thickness of 100nm. The bottom electrode is planarized before HZO deposition to ensure a TiN roughness smaller than 0.2nm RMS. The structures are then annealed in a nitrogen atmosphere after top electrode deposition. Grazing-Incidence X-Ray Diffraction (GIXRD) performed on TiN/HZO/TiN blanket stacks clearly demonstrates the appearance of a ferroelectric orthorhombic oIII-phase after 450°C anneal (Fig. 1) [1]. Ferroelectricity is electrically confirmed on capacitors annealed at this temperature as shown in raw P-E plots of Fig. 2. The experimental hysteresis is well reproduced by the time-dependent Preisach model of hysteresis, adjusted to the produced ferroelectric capacitors, for further use in circuit designs. From PUND-corrected [5] P-E plots (Fig. 3), remnant polarization $2.P_R$ and coercive field E_C are systematically extracted along cycling (Fig. 4) for different annealing conditions spanning a temperature range from 520°C down to 350°C, showing state-of-the-art HfO_2-based MFM capacitors performance [2]. Lower thermal budget leads to lower $2.P_R$, but it is worth noting that $2.P_R$ >30µC/cm² performance is still achieved even at 350°C. No impact of annealing on E_C has been found, with extracted E_C values in the range of 1.5MV/cm to 1.75MV/cm (data not shown). Fig. 5 highlights excellent data retention up to 1440min baking time at 85°C for Ø100µm capacitors.

During annealing, the nucleation process can be qualitatively understood in the light of ab-initio simulations, where the stability of each HZO phase and orientation is calculated for different film thickness (Fig. 6). For 10nm HZO, monoclinic P21c (-111) is the most stable phase whereas tetragonal P42nmc with preferred orientation (101) and ferroelectric Pca21 with preferred orientation (-111) are both metastable. Following Ostwald's law: "Thermodynamically metastable phase should nucleate first", the red arrow of Fig. 6 suggests how increasing thermal budget is expected to reorganize the system, from amorphous (high disorder i.e. high in energy) to monoclinic (lower in energy), passing through the tetragonal and orthorhombic phases (intermediate in energy). Starting from an as-deposited amorphous HZO and not a monoclinic stable HZO is therefore key to obtain the orthorhombic phase, as recently demonstrated experimentally by sputtering deposition [6]. In our case, ALD deposited HZO is amorphous with a weak spatial coherence (corresponding to top-left corner of Fig. 6), which can explain the lower temperature required to obtain ferroelectric films compared to the sputtering technique [6,7].

Beyond the satisfactory ferroelectric performance reported at low temperature, a preliminary evaluation of NVM performance has been conducted at material scale. In the following, we mainly focus on Ø100µm capacitors annealed at 450°C for 600s. Fig. 7 shows switching efficiency map of squared-shape programming and erasing pulses (details about

this electrical sequence can be found in [8]). An outstanding 30ns switching capability is demonstrated for both operations and the suitability of ferroelectric HZO for multi-level cell memories is also highlighted. From switching efficiency map, four distinct operation patterns have been selected and used to evaluate their impact on endurance performance (Fig. 8a). In this case, $2.P_{SW}$ is reported instead of $2.P_R$, i.e. the polarization really switched by square signals which can be considered as the Memory Window (MW). As already reported for HfSiO [8], proper signal engineering allows to finely tune HZO endurance/performance compromise. In particular, applying 2V instead of 4V for same pulse width leads to an endurance gain of several order of magnitudes while dividing the polarization by less than two. Fig. 8b highlights this clear dependency between the maximum $2.P_{SW}$ and the maximum number of cycles before breakdown (CBD).

III. HZO FERAM INTEGRATION IN 130NM CMOS BEOL

Based on the above results, TiN/10nm-HZO/TiN capacitors with diameters ranging from 600nm down to 300nm were then integrated in the BEOL of 130nm node 200mm CMOS technology, in various design environments ranging from single 1C bitcells up to 16kbit 1T-1C arrays. Fig. 9 shows a simplified integration overview of the scaled HZO capacitors integrated between M4 and M5. The highest thermal budget used in this BEOL integration for HZO crystallization, 450°C for 80s, is shown to have no detrimental impact on front-end transistor, as shown in the I_D-V_G characteristics of nMOS and pMOS in Fig. 10.

Scanning Electron Microscope (SEM) observations have been performed on 16kbit 1T-1C arrays (Fig. 11 and Fig. 12), revealing front-end circuitry, M1 to M5 BEOL and MFM capacitors. In-depth Scanning Tunneling Electron Microscope characterization confirms the first reported 1T-1C integration of a Ø300nm HZO capacitor in BEOL, with a perfect layer integrity as revealed by EDX images of Fig. 13. High Resolution Transmission Electron Microscopy (Fig. 14) confirms HZO crystallization with BEOL-compatible thermal budget, with crystallite sizes of 10nm and ~20nm for out-of-plane and in-plane, respectively. This crystallite size anisotropy is confirmed by the In-Plane and the GIXRD peak width analysis (Fig. 15). Moreover, the offset between the out-of-plane and the in-plane oIII lattice spacing of the orthorhombic phase (deduced from 2Theta position) suggests a tensile stress of +3.3GPa in the HZO layer according to elastic constant from [9].

As analog electrical measurements performed on single bitcells with diameter <600nm might rise experimental challenges, the performance of BEOL-integrated MFM bitcells was first evaluated on dedicated test structures consisting in 339 Ø550nm bitcells routed in parallel, corresponding to an equivalent total area of 80µm². Fig. 16 confirms excellent ferroelectric behavior along HZO cycling, consistently with results reported above on large area capacitors (~10000µm²). Extracted ferroelectric peaks per bitcell with currents in the nA range in the I(V) characteristics, points towards extremely low programming power (<10fJ/bit) at the FeRAM bitcell level (Fig. 17). Despite the very low displacement current signal, single 1T-1C bitcells with capacitor area of 0.12µm² were successfully measured for the first time with PUND technique. Fig. 18 shows that the polarization charge scales with the surface between 550nm and 400nm diameter capacitors and that the introduction of the 1T transistor selector does not modify the 1C behavior. Switching efficiency map of single Ø600nm (0.27µm²) MFM capacitor is reported in Fig. 19, highlighting excellent operating speeds as low as 30ns and multi-level programming capability. This good agreement with 10000µm² area capacitor results of Fig. 7 confirms the scalability of this technology. Together with operation speed, excellent endurance performance is also reported in Fig. 20 with an optimized 4V 100ns pattern, demonstrating for the first time $>10^{11}$ cycling capability for a BEOL-integrated HZO memory bitcell. Data retention was assessed on scaled capacitors test arrays showing no information loss after 1000min at 125°C for both programming operations (Fig. 21).

IV. 16KBIT 1T-1C HZO ARRAY FIRST DEMONSTRATION

16kbit 1T-1C arrays (Fig. 22) with capacitors of different sizes were programmed and erased by voltage pulses and read out by means of an integrated sense amplifier (SA). In this first demonstration, the SA was designed in a generic way and not specifically for 1T-1C FeRAM, thus explaining the relatively small Memory Window reported in the following. For the read out, a positive voltage pulse with the same level as the programming pulse is used. Hence, program switching voltage V_{PRG} does not show any signal coming from ferroelectric switching. On the contrary, when the cells are erased (negative pulse) and read out (positive pulse), the erase switching voltage V_{ERS} on single capacitors includes a ferroelectric switching component. Fig. 23 shows the measured V_{PRG} and V_{ERS} switching voltage at SL for 16kbit 1T-1C arrays with different capacitor sizes. Reported data have been averaged over the entire array. V_{ERS}-V_{PRG} corresponds to the memory window, which, as expected, decreases when capacitor area shrinks from 0.3µm² down to 0.1µm². Given the excellent ferroelectric material properties reported at bitcell scale, one can expect larger MW on a 16kbit with optimized SA design, which is highly promising for NVM and LIM applications.

V. CONCLUSION AND PERSPECTIVES

Successful integration of ferroelectric TiN/HZO/TiN MFM capacitors in 130nm node BEOL is demonstrated for the first time, up to 16kbit 1T-1C array integration. Excellent performance is reported for capacitors down to 300nm diameter, notably 30ns operation speed together with outstanding $>10^{11}$ cycling capability and promising data retention at 125°C. HZO is found to exhibit excellent ferroelectric properties even at low thermal budget, with state-of-the-art $2.P_R$ reported values.

ACKNOWLEDGMENT

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HZO material study for BEOL thermal budget compatibility

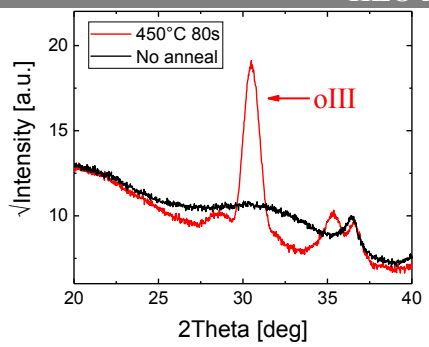

Fig. 1: GIXRD spectra on TiN/HZO/TiN stacks with and without 450°C 80s anneal performed after TiN top electrode deposition, highlighting the appearance of orthorhombic oIII-phase for low thermal budget.

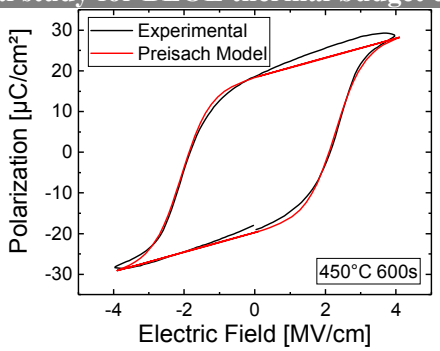

Fig. 2: Raw P-E plot on Ø100µm TiN/HZO/TiN capacitor annealed at 450°C 600s and corresponding simulated curve derived from the Preisach-based model for accurate circuit simulations.

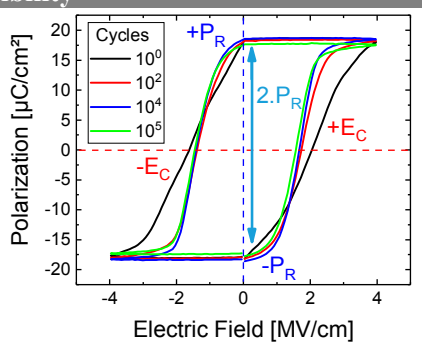

Fig. 3: PUND-corrected P-E measured at 10kHz +/-4V on Ø100µm TiN/HZO/TiN capacitor annealed at 450°C 600s, to derive accurately $2.P_R$ values. Cycling has been performed with a 100kHz +/-4V triangular signal.

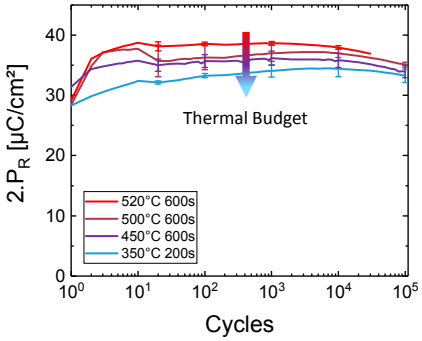

Fig. 4: $2.P_R$ values (mean and stand. dev.) reported along triangular cycling (4V/100kHz) for 10 TiN/HZO/TiN capacitors (Ø100µm) after various anneals. HZO is demonstrated to be ferroelectric down to BEOL compatible thermal budgets with a minor decrease of $2.P_R$.

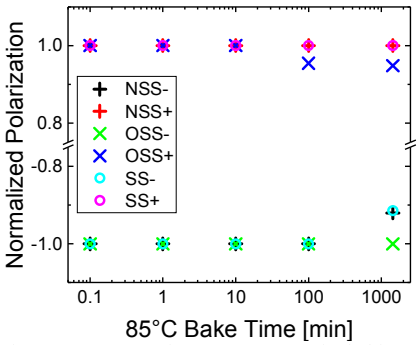

Fig. 5: Data retention up to 1440min baking time at 85°C on Ø100µm capacitors measured with state-of-the-art FeRAM reliability characterizations [10].

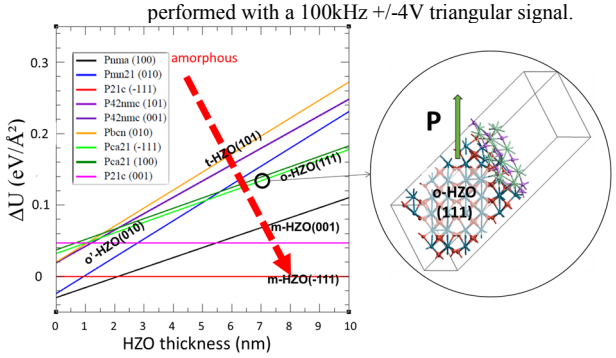

Fig. 6: Ab-initio simulations (DFT GGA/PBE calculations in Siesta) where ΔU(P)/S is computed for various phases and orientations in HZO for thickness in the (1-10)nm range. ΔU(P)/S is the difference in internal energy per surface unit, between a set P={phase,orientation} of HZO and the {monoclinic, (-111)} of reference of equivalent thickness.

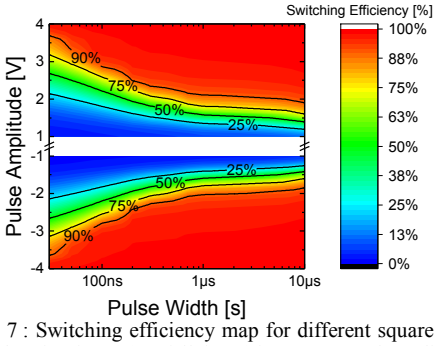

Fig. 7 : Switching efficiency map for different square pulse widths (rise time (tr) & fall time (tf) = 100ns) and amplitudes, with a PUND $2.P_R$ as reference, on a Ø100µm 450°C 600s annealed TiN/HZO/TiN capacitor, revealing programming conditions compatible with memory operations.

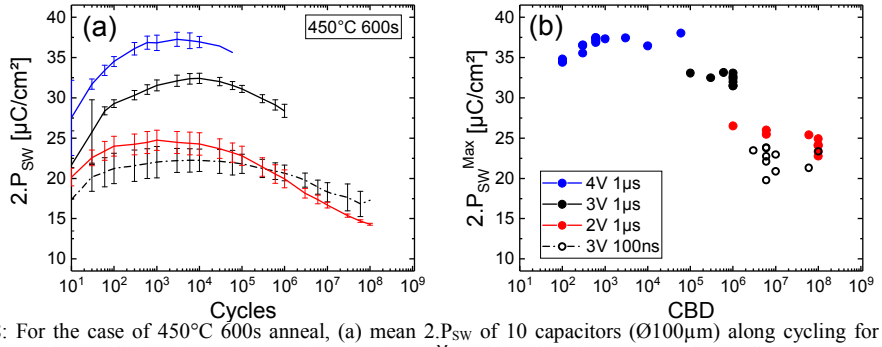

Fig. 8: For the case of 450°C 600s anneal, (a) mean $2.P_{SW}$ of 10 capacitors (Ø100µm) along cycling for four different pulse conditions (tr & tf = 100ns) and (b) $2.P_{SW}^{Max}$ achieved during square pulse cycling as a function of the corresponding die's CBD, illustrating the trade-off between switched polarization values and maximum endurance reached upon programming conditions.

1T-1C integration of HZO capacitors down to 300nm diameter in the BEOL of 130nm CMOS node

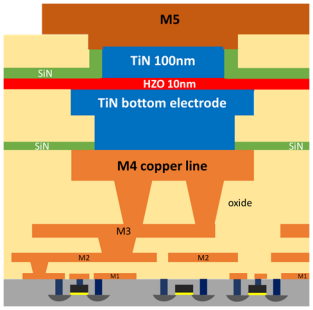

Fig. 9: Schematic cross section of TiN/HZO/TiN MFM capacitors integrated between M4 and M5 of 130nm CMOS technology.

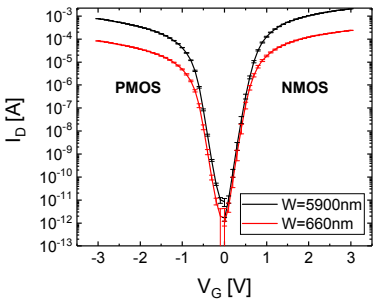

Fig. 10: I_D-V_G transfer characteristics of CMOS transistors with different gate widths after 1T-1C HZO integration, showing neither V_T dispersion nor I_{ON} reduction (mean and sigma, 55 dies tested at wafer scale).

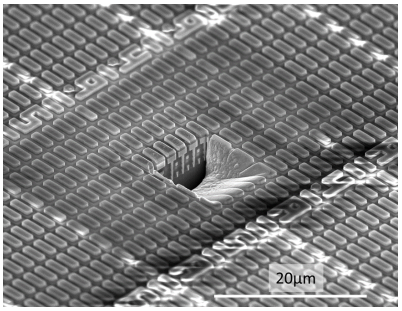

Fig. 11: SEM tilted view of a 16kbit 1T-1C TiN/HZO/TiN array post M5 with a FIB cut unveiling the CMOS and metal levels from M1 to M5.

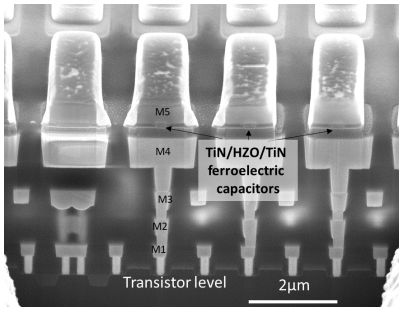

Fig. 12: SEM cross section showing the transistor level, the different metal lines, and Ø300nm ferroelectric capacitors TiN/HZO/TiN integrated between M4 and M5.

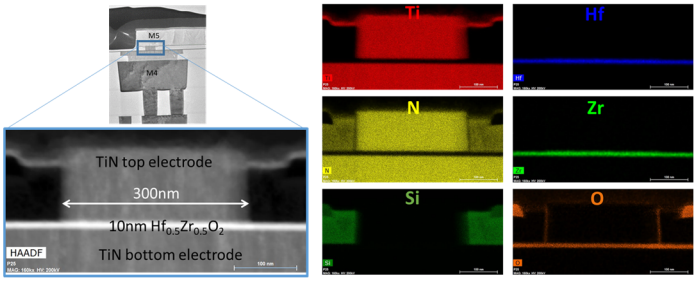

Fig. 13: High-Angle Annular Dark-Field (HAADF) Scanning Transmission Electron Microscope (STEM) cross-section image of a Ø300nm TiN/HZO/TiN ferroelectric capacitor and corresponding energy dispersive X-ray (EDX) images.

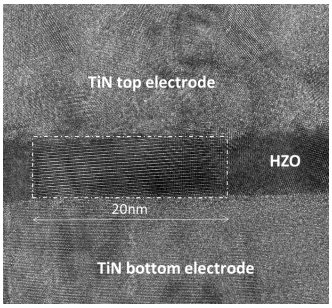

Fig. 14: HRTEM image detail of a Ø300nm TiN/HZO/TiN FE capacitor with 20nm crystallite size (in-plane).

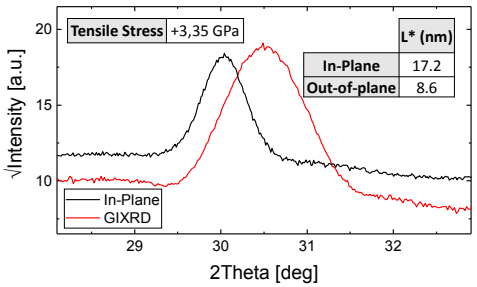

Fig. 15: From the GIXRD and the in-plane XRD patterns, the crystallite sizes (L*) and the layer stress are extracted from the oIII peak widths and positions, respectively.

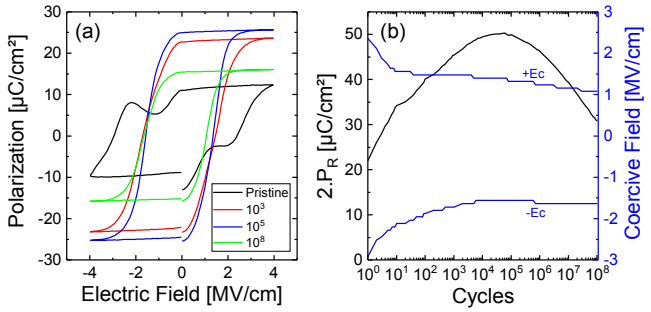

Fig. 16: (a) PUND-corrected P-E curves on 339 Ø550nm bitcells routed in parallel at various cycles and (b) corresponding $2.P_R$ and E_C during triangular cycling (4V/100kHz).

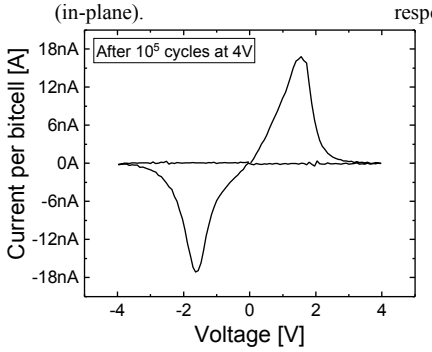

Fig. 17: Typical PUND-corrected current per Ø550nm bitcell VS voltage extracted from Fig. 16, demonstrating extremely low programming power (<10fJ/bit) at the FeRAM bitcell level.

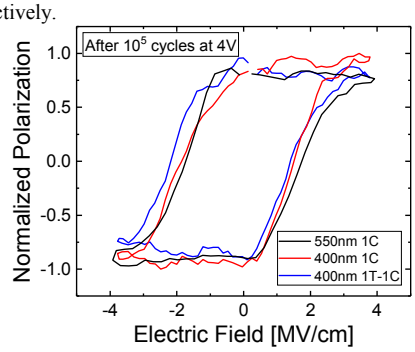

Fig. 18: Normalized polarization measured on BEOL integrated single 1C (Ø550nm and Ø400nm) and 1T-1C (Ø400nm) through an open transistor (V_G=5V).

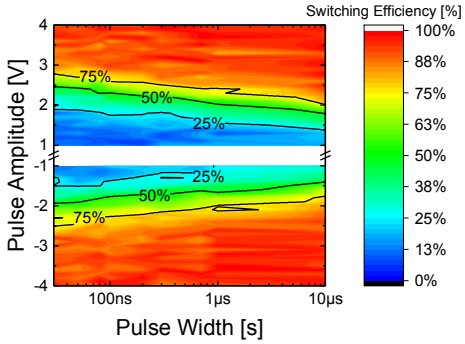

Fig. 19: Switching efficiency map on Ø600nm capacitor (tr & tf = 100ns) with a PUND $2.P_R$ as reference. PUND and Domains Check (see Fig. 9 of [8]) are averaged multiple times to take into account the challenge of measuring nA displacement currents.

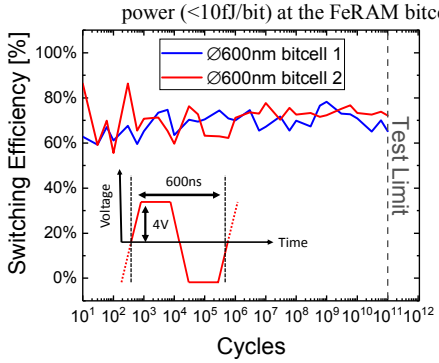

Fig. 20: Ferroelectric switching efficiency measured on two Ø600nm single capacitors with optimized pattern (+/-4V, 100ns, tr & tf = 100ns) along cycling. No bitcell breakdown is observed before 10^{11} (i.e. experimental limitation).

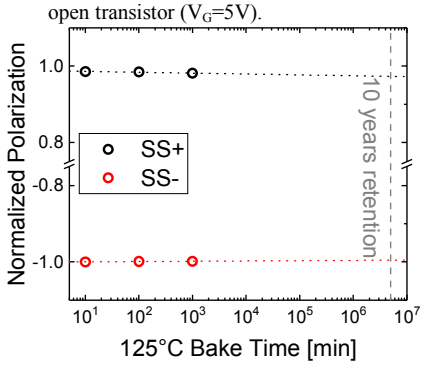

Fig. 21: Same State (SS) with positive (SS+) and negative (SS-) programming condition (see [10]) data retention at 125°C measured on bitcells routed in parallel.

16kbit design and first array demonstration

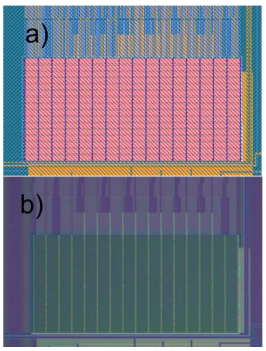

Fig. 22: (a) layout and (b) optical microscope view of a 1T-1C 16kbit array with TiN/HZO/TiN capacitors diameters of 300nm.

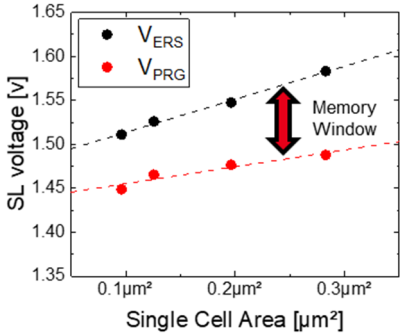

Fig. 23 : V_{PRG} and V_{ERS} switching voltages applied at Source Line (SL) for 1T-1C HZO 16kbit arrays with capacitor diameter ranging from 600nm down to 300nm, illustrating the memory window decrease with size.

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