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Abstract

This paper deals with data analysis of long term (2 years) accelerated stress test of a 65nm ASIC dedicated to cryptographic applications. Several stress conditions have been applied by combining both thermal and electrical overvoltage stresses. At the end of the ageing test, frequency drifts analysis indicates the presence of NBTI. Two statistical calculation methods have been considered in estimating the mean or median time to failure, each one relying on a different failure criterion. We confirm reliability of 65 nm technologic node even in complex architecture.

1. Introduction

In many industrial areas, reliability is a critical issue. In most cases, designers use data provided by manufacturers. However, most manufacturers rely on highly accelerated stress tests during only a couple of weeks to qualify their products. Next, they adjust their estimated failure rates based on field experience.

The purpose of this paper is to compare these results to our long stress time results. Indeed, silicon dies' lifetime decreases after each technologic node shrink and with the current COTS trend. Life profile of recent commercial components is targeted to be short (a couple of years). Nevertheless, in some fields such as military programs, these lifetimes are expected to be as long as 20 years.

The ASICs under assessment are manufactured according to the 65 nm technologic node. Embedded is complex native architecture, including multicore processor, cache memory, ethernet interface, DDR interface, etc.

2. Test plan

The initially planned ageing duration was 2 years and it was chosen to implement a functional architecture. No Design for Reliability (DFR) rules have been applied in this design for test.

2.1. Functional ageing test

Each ASIC embeds functional structures to self-stress and self-test internal blocks. These structures activate SRAM blocks, PLL clock generation, processor, logic block, RNG (Random Number Generator), processor and DDR interface.

Regarding RAM blocks, activation is done at two frequencies of write/read operations. Nevertheless, some addresses remain in the same state during ageing. So, to enhance probabilities of observing a NBTI mechanism, at least one PMOS of these SRAM stands in the worst possible configuration.

Moreover, many parameters are monitored continuously while ageing. The errors recorded concern: read RAM error, write RAM error, RNG statistical analysis error compared to setup values, Ethernet communication error, PLL frequency

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check, CPU executing error, etc.

2.2. Test Matrix

The test matrix applies to 78 DUTs (Device Under Test) which are dispatched as described in Table 1. Two devices are used as reference to correct any external skews, during ageing or readouts.

Three ageing temperatures have been selected from 25°C to 125°C. In addition three overvoltage values ranging from 110% to 140% of nominal power supply values have also been applied.

Another stress parameter is the operating frequency during ageing which is supposed to influence degradation at low temperatures and high voltages in regards to HCI.

Table 1
Test table for the 76 ASICs under evaluation

Ageing temperature	Ageing voltage			
	Vnom+10%	Vnom+20%	Vnom+40%	
25°C	5	5	4	*4*
85°C	/	/	4	*/*
125°C	25	25	4	*/*
Device aged at Fnom = 445.5 MHz				
Device aged at Fmin = 54 MHz				

2.3. Readout operations

At planned steps, readouts are performed during which many DUT parameters are measured in regulated room between 18°C and 22°C. Time duration between these steps increases geometrically.

Firstly, continuity is checked (using ESD protection diode) between each pin and VCC, and between each pin and GND. Leakage currents of input pins are measured in both logical states. Output pins VOL and VOH voltages are also captured. The measurement of consumption is done in "standby" as well as in running modes. In both cases, internal configuration is controlled in order to always measure under the same conditions.

Secondly, functional tests are conducted starting by checking whether DUTs are still able to perform an errorless boot sequence. Activation and locking of PLLs are tested. Classical SCAN chains are used to check integrity of design after ageing.

Components' logical paths of DUT are evaluated at low frequency to detect any that could be stuck at '1' or '0'. These paths are tested with an increasing frequency until faults occur and the maximal frequency is recorded. It represents the limit when delay (propagation time between two successive flip-flops) of the critical path is exceeded.

RAM gets tested by the use of a BIST (Built-in self-test) which writes and reads SRAM content on a static range of addresses. If read data mismatches written data, it means the frequency used by the BIST (including SRAM) is out of bound regarding propagation times.

3. Results

The last step (and thus the ageing) ends after 16 000 hours for each device. Neither the monitored parameters (power supplies, monitoring during ageing, VOL, VOH, etc.) nor the cryptologic functions significantly shifted after the ageing period. Only the maximum frequency of errorless running test decreases.

In this paper, frequency drift is defined as:

$$vf(t) = \frac{f(t)-f(0)}{f(0)} \quad (1)$$

The maximum supported frequency by logical blocks reveals the worst drift case (up to 16.5%), followed by the maximum frequency of SRAM tests (up to 5%).

The negative drift is slightly higher for high temperature and significantly higher for high voltage as it is shown on Fig. 2.

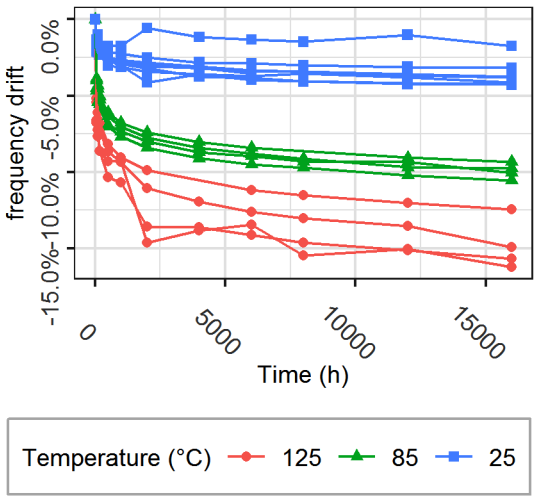

Fig. 1. Frequency drift of DUT aged at 1.4V

4. Frequency drift analysis

Propagation delays across logical elements increase while ageing. This is mainly the result of transistor threshold voltage shifts.

According to literature, observed frequency drifts fit well to power law time dependence. As it

can be noticed on Fig. 2, in a plot using logarithmic scales, measurementslie in a straight line. However, measurementsat low temperatures and low voltages are very close to noise.

The higher the ageing temperature the higher the degradation. Subsequently, the higher the overvoltage during ageing, the higher the degradation. The remaining question lies in extracting the acceleration factors involved.

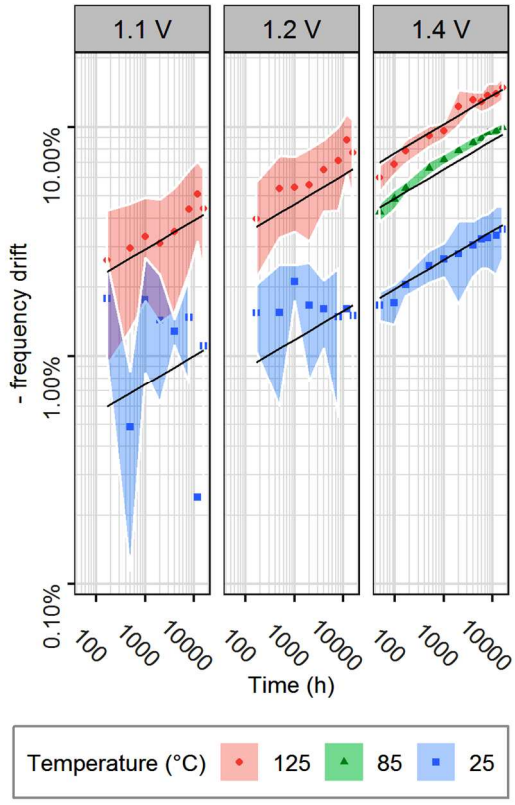

Fig. 2. Evolution of the mean percentage of frequency drifts for each stress condition. Error envelopes are the empirical unbiased standard deviation. And solid black line is the fitted model.

Fitted equation is the following:

$$vf = A_0 . V^{\alpha_{drift}} . exp\left(\frac{-E_{a_{drift}}}{k_b . T}\right) . t^n \qquad (2)$$

vf is the relative frequency drift
t is the stress time in hours
A_0 is a technology dependent constant
$E_{a_{drift}}$ is the apparent activation energy of frequency drift in eV
k_b is the Boltzmann constant
T is the temperature in Kelvin
V is the voltage in Volt
α_{drift} is the electrical acceleration exponent of frequency drift
n is the exponent of the temporal power law

The values of these parameters have been estimated by minimization of the Sum of Squares Error (SSE) and are given in Table 2. These values and the ageing conditions indicate clearly a NBTI signature [1] [2] [3]. HCI degradation does not seem to be implicated in this test. Causes are probably a frequency not high enough and a lowest ageing temperature not low enough. Indeed, for a BTI effect, papers found exhibit parameter values in the same range for the same law (see Eq. 2)) [4] [5].

Table 2
Parameters estimation of the power law

Parameter	Value	Value extracted from other papers (NBTI)
n	0.1836	0.15 to 0.29
$E_{a_{drift}}$	0.1349	0.01 to 0.4
α_{drift}	5.478	3 to 5

5. Statistical analysis

5.1. Definition of a failure

Before starting any estimation of time to failure, it is very important to clearly define what the failure criterion is. Either the failure can be defined as a cataleptic (or catastrophic) failure; or it can be defined as a limit of degradation concerning the most critical parameter.

The first one corresponds to a fault (or even a total destruction of circuit behavior) occurring mainly in the bottom (second part) of the famous bathtub curve. This phase corresponds to the component's service. The failure rate follows an exponential failure distribution law, and so is constant.

The second one rather describes the wear out of component which corresponds to the third part of the bathtub curve. DUT readout characterizations allow us to observe regular parameter degradations, and thus focus on the worst parameter. If the maximum drift allowed until circuit fault is known, this point of view is right. But, in practice, the typical value of 10% of maximum frequency drift is used even if this is not a mirror of the design reality.

5.2. Zero failure analysis

Whatever the accelerated stress test conditions used in these experiments, up to VCC=40%,

Tj=125°C, no functional, neither parametric failure, has been observed. Only limited drifts under more than 16000 hours have been noticed. This is an outstanding result for a complex Asic (45 mm²) with a multicore architecture and a lot of memory blocks. The behavior is much better than expected considering the reliability tests performed on manufacturer's PCM (Process Control Monitor). From a customer point of view, the JEDEC 122 [6] standardized models can be used to extrapolate the relevant end of life (MTTF) depending on mission profiles. In this case, for the most severe military applications (duty cycle =100%, Tj=55°C, VCC+10%), taking into account the most conservative acceleration parameters coming from experimental data (Ea= 0,4 eV and α=18), the extrapolated MTTF is greater than 1977 years. One can notice that Ea and α parameters are more pessimistic than values provided by maximum likelihood estimations (see 4.4.2).

In terms of failure rate (λ) estimation, we can apply the Khi2 law with 0 failure during all these ageing tests: $\lambda \approx$-Ln(β)/TTT with β is the level of confidence and TTT the cumulative components hours (cp.h) [7] [8]. TTT is defined by applying the relevant acceleration factors for each ageing conditions (see Table 1) versus the military mission profile with the same Arrhenius and Eyring law parameters as described above (TTT $\approx 10^8$ cp.h). Thus, the upper estimation for the failure rate is 15 Fits (1 Fit= 1 failure per 10^9 component hours), which is definitely a good value for such an Asic.

5.3. Data processing

In our current study, drifts have been observed and even modelled. Nevertheless, only some of the DUTs aged in the worst conditions have reached the 10% limit. For the others, it is inappropriate to simply consider them as right-censored.

The idea to reduce the "censure rate" is to use as much collected informations as possible to predict the time to failure of each DUT. If DUT measurementsdo follow a power law time dependent with a coefficient of determination (also called R^2) of at least 0.90, the 10% of drift time value will be extrapolated. If not, the data remains right-censored. The parameters of power law are calculated individually for each DUT.

5.4. Statistical distribution choice

5.4.1. Lognormal

In the silicon world, the most useful distributions are "Weibull" and "lognormal". Weibull distribution is particularly interesting thanks to its capability to model the entire bathtub curve depending on its shape parameter.

However, in this context of parameter drift, lognormal law provides better fit than Weibull law in accordance with literature.

The cumulative distribution function (CDF) of this distribution is:

$$F(t) = \Phi\left(\frac{ln\left(\frac{t}{\mu}\right)}{\sigma}\right) \quad (3)$$

F is the cumulative distribution function
t is the time
Φ is the CDF of the standard normal distribution
μ is the median of t
σ is the standard deviation of the logarithm of t

In order to integrate the two acceleration factors (thermal stress and electrical stress), we have used the following form:

$$\mu(T,V) = \mu_0 . V^{-\alpha_{stat}} . exp\left(\frac{Ea_{stat}}{k_b . T}\right) \quad (4)$$

μ_0 is a technology dependent constant
Ea_{stat} is the apparent activation energy in eV of statistical analysis
α_{stat} is the electrical acceleration exponent of statistical analysis

The alternate electrical acceleration factor used for older technological node is an exponential law as described in Eq. 5.

$$\mu(T,V) = \mu_0 . \exp\left(-\gamma_{stat} . V\right) . exp\left(\frac{Ea_{stat}}{k_b . T}\right) \quad (5)$$

γ_{stat} is the parameter of acceleration factor in exponential

A comparison between a power law and an exponential law has been done and, while exhibiting close results, the power law provides a better fit.

5.4.2. Maximum likelihood estimation

The method used to estimate parameters is the maximum likelihood estimation (MLE). This is the most precise way to estimate parameters with a minimum of skew. MLE takes into account censored data. The principle is to search parameter values where the jointed probability of the observed results is the highest.

$$L(t,X,Y) = \left(R(t_M)\right)^Y . \prod_{j=1}^{X} \left(F\left(t_{2,j}\right) - F\left(t_{1,j}\right)\right) \quad (6)$$

L is the likelihood function
X is the number of failing sample
Y is the number of unfailing sample during t_M
$t_{2,j}$ is the first readout time when sample j is fail
$t_{1,j}$ is the last readout time when sample j is still good
t_M is the last readout time of ageing (16 000 h)
F is the cumulative distribution function
R is the survival function

Once optimization of likelihood functions is done, choosing the best model is done using the highest value. All tested model are described in Table 3. As it can be highlighted, log-normal distribution fits better than Weibull distribution in our case [9]. Nevertheless, scores of MLE between the electrical acceleration factor with a power law and an exponential law are close.

Results of this model are plotted in Fig. 3. Visually, points' alignment for each stress condition is satisfying. Moreover, acceleration factor calculation reports good prediction with black lines compared to real measurements.

Table 3
Log-likelihood value for each model (AF + distribution)

AF		Distribution	
Thermal AF	Electrical AF	Weibull	Log-normal
$\exp\left(\frac{Ea_{stat}}{k_b.T}\right)$	$\exp(-\gamma_{stat}.V)$	-461,78	-454,06
$\exp\left(\frac{Ea_{stat}}{k_b.T}\right)$	$V^{-\alpha_{stat}}$	-461,98	**-453,72**

The likelihood-ratio test does not detect a significant variation of the shape parameter of the log normal law across every stress condition with 5% of error risk. This fact indicates the presence of the same mechanisms of degradation for every stress conditions, and so validity of model produced.

Table 4
Estimation of the distribution parameters

Parameter	Value	Standard error
σ	3.3	0.27
Ea_{stat}	0.87	0.083
α_{stat}	29	4.1
μ_0	-9.8	2.8

We could find in literature, concerning NBTI effect, standard deviations between 0.1 and 0.3 [9]. Our standard deviation is estimated at 3.3, which is above transistor level test values from other papers. This mismatch could be due to extrapolation of drift on devices showing slight measured drift. Moreover, if we calculate the standard deviation of logarithm of Eq. 8, we obtain about 0.24. This result is below the standard deviation estimated by maximum likelihood estimation.

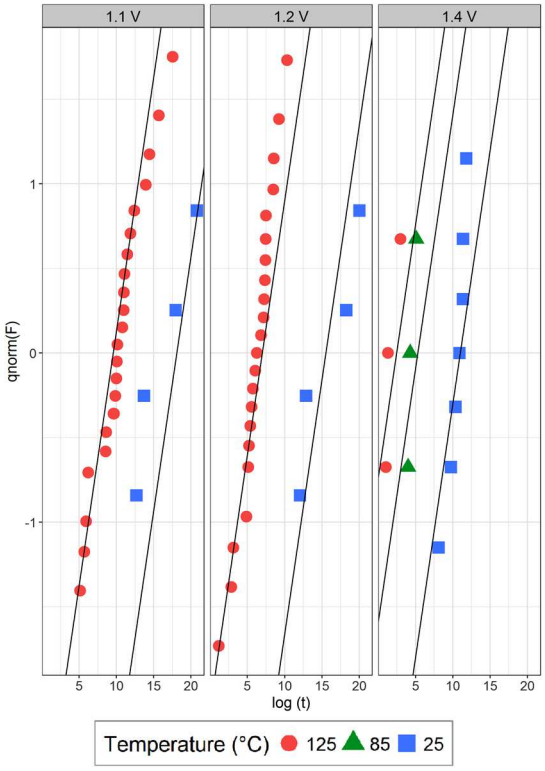

Fig. 3. Cumulative failure plot in log-normal scale

5.4.3. Evolution of AF parameter with failure criteria

In order to confirm our acceleration factor parameters, we have recalculated them for several failure criteria (3%, 3.5%, 4%, 5%, 8% and 10%). The goal of this operation is to reduce the extrapolation skew. Indeed, if the failure criterion is reached for many pieces, no extrapolation is needed.

The evolution of the energy of activation is shown Fig. 4. The value of parameter Ea_{stat} remains between 0.84 eV and 0.88 eV. The value of exponent α_{stat} varies from 28 to 34 (see Fig. 5).

This approach highlights robustness in our global methodology to extract acceleration factor parameters.

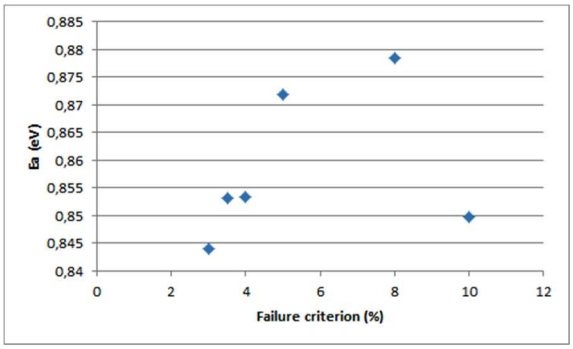

Fig. 4. Evolution of the apparent energy of activation with several failure criteria

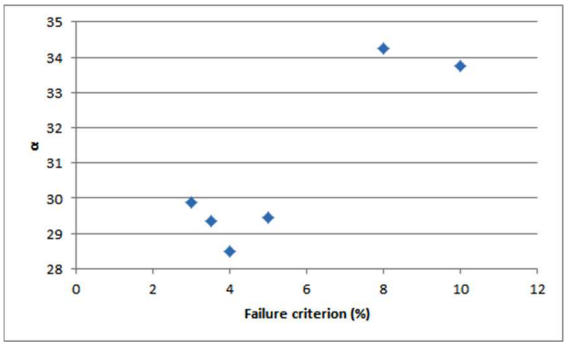

Fig. 5. Evolution of alpha exponent in power electrical acceleration factor with several failure criteria

5.4.4. Link with frequency drifts model parameters

It is possible to obtain the ageing time t_{lim} when frequency drifts reach an arbitrary limit named vf_{lim} from Eq. 2.

$$t_{lim} = \left(vf_{lim} . \frac{1}{A_0} . V^{-\alpha_{drift}} . exp\left(\frac{E_{a_{drift}}}{k_b . T} \right) \right)^{\frac{1}{n}} \quad (7)$$

And with some shaping:

$$t_{lim} = V^{\frac{-\alpha_{drift}}{n}} . exp\left(\frac{E_{a_{drift}}}{n . k_b . T} \right) . \left(\frac{vf_{lim}}{A_0} \right)^{\frac{1}{n}} \quad (8)$$

And through identification:

$$\begin{cases} E_{a_{stat}} = \frac{E_{a_{drift}}}{n} \\ \alpha_{stat} = \frac{\alpha_{drift}}{n} \end{cases} \quad (9)$$

Where $E_{a\ stat}$ is the apparent energy of activation estimated in distribution model [10], and $E_{a\ drift}$ is estimated in frequency drift model.

Applied to our results, both values calculated are coherent. We found $E_{a_{drift}}/n = 0.73\ eV$ and $\alpha_{drift}/n = 29.8$.

5.4.5. Lifetime estimation in operational condition

From these parameter estimations, and our statistical distribution choice, for operating conditions of life of Vcc+10% and 125°C, we are able to estimate a median time to fail, called *t50*, of up to 274 years ! The confidence interval of *t50* with 10% of risk is from 117 years to 640 years.

This result is better than manufacturer values (they cover at least 10 years even for dies extracted from wafer corner and worst case life profile). However, ASICs used in our study were extracted from the center portion of a same wafer.

Now the distribution is estimated, the cumulative distribution function (called CDF) can be easily plotted in Fig. 6. Compared to exponential distribution, failure probability of log-normal distribution is lower at the beginning, and becomes higher near the MTTF.

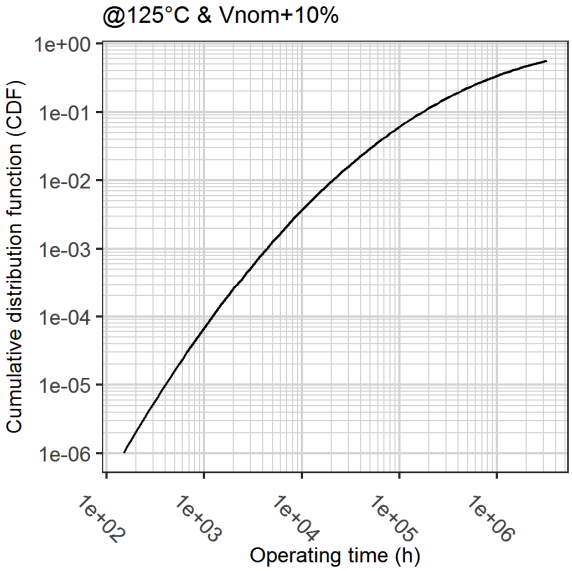

Fig. 6. Failure probability versus operating time for devices at 125°C and Vnom+10%.

In the zero failure calculation, we assume that failures follow an exponential distribution with lambda parameter of 15 FIT at 55°C and Vnom+10%. In the same conditions as in Fig. 6, we obtain 180 FIT using section 5.2 parameters. The associated CDF after 16 000 hours is about $2.9*10^{-2}$. It is consistent with maximum likelihood estimation projection.

6. Conclusion

This paper presents data analysis of a 65nm

ASIC dedicated to cryptographic application. After 2 years of ageing stress, we have demonstrated presence of NBTI on PMOS as prior mechanism of degradation. Analyses of results are according to state of the art in terms of failure mechanism. Nevertheless, results exhibit much slower drifts contrary to some pessimistic previous Deep Sub Micron reliability data coming from our literature survey. Otherwise statistical lifetime estimation has been conducted. This study validates estimations realized by manufacturer which applies a completely different process based directly on ring oscillators in wafer level. Not only extracted we typical values of parameters with our system approach and long ageing test, but also we confirmed the reliability of this technologic node even on complex die architecture with an estimated lifetime over every expected application.

Acknowledgements

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