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Loss-Based Design for Natural Balancing in a 12-FC's cells Converter Using Vectorized Models

Jaime W. Zapata*, Thierry A. Meynard*, Guillaume Gateau* and Didier Ferrer†

*Institut National Polytechnique de Toulouse, University of Toulouse, Toulouse, France

†CIRTEM, 4 Avenue Louis Blériot, ZA Val de Saune, 31570 Sainte-Foy d'Aigrefeuille, France

Abstract—The inherent features of the Multicell Flying Capacitor (FC) converters, allow a voltage natural balance under phase-shifted pulse width modulation (PS-PWM) techniques. Nevertheless, an external balance booster is required under certain operation conditions, i.e. when the voltages in the capacitors vary between the commutation cells. This paper validates the methodology to design balance booster, based on vectorized models using a 12-FC's cells converter. The trade-off between balancing speed and power losses, presents an important challenge for the design of a balance booster speed requirements. In addition, if the loss constraints are checked afterwards it may result in a very long iterative process. Therefore, a loss-based design, followed by a speed evaluation is a much simpler process. This methodology is illustrated in this paper working with different types of balance boosters. Some simulations results obtained in PLECS® are provided to enhance the benefits of the vectorized model for power electronic circuits, and an experimental test-bench is built in order to validate the proposed approach.

I. INTRODUCTION

A multicell topology is typically formed by a number of n_S -commutation cells $n_S = \{1, 2, \dots\}$, which are connected forming an inverter leg or a chopper circuit [1], [2]. These commutation cells are capable to block an input voltage v_{HV} using devices with reduced blocking voltage ratios [3]. The generated voltage waveform is made by steps of amplitude v_{HV}/n_S , and the output frequency is n_S times the switching frequency of a single cell, which allows an inductor filter reduction by a ratio of n_S^2 . Moreover, the generated output voltage can be greatly optimized by using interleaving signals $2\pi/n_S$ for the different cells [4]. The FC converter is quite attractive in high power applications because of its performance when the number of levels increases. However, there are some issues to overcome such as the initial charging process, and balancing of the flying capacitors [5]. In the literature it is possible to find many techniques developed to ensure a balanced operation, many of them are based on variations of the pulse width modulation [6], active voltage balancing techniques and closed control loops [7]. Using passive components it is possible to balance the cells in two different ways: The first one is connecting passive components in parallel with each commutation cell. In that case, the most charged capacitor will supply more energy which tends to discharge it until balance is reached. The disadvantage is the increase of losses due to the pure resistances. The other mechanism, described as natural balance, is an inherent feature of the system which involves the AC current harmonics [8], [9]. The convolution of these harmonics with the chopping

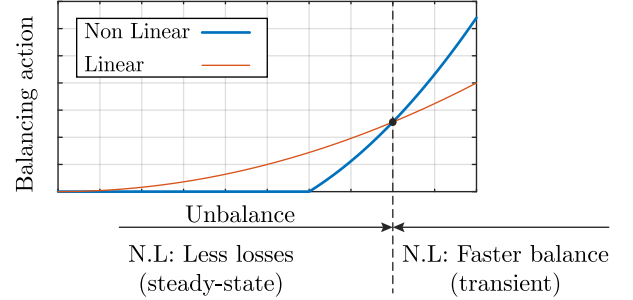


Fig. 1. Importance using non-linear balance boosters.

signals harmonics generate DC currents [8]. However, this effect can be weak and some balance boosters must be added to increase this effect. Several papers have presented the use of RLC networks connected in parallel to the load to limit the unbalance [10]–[12].

There is a trade-off between balancing strength and power consumption: the faster the balancing speed, the more losses. However, it is possible to improve this trade-off by using non linear circuits (NL). They can be designed to have a stronger effect for higher unbalance, and less losses for lower unbalance as depicted in Fig. 1.

This work validates the methodology designing a balance boosters for a 12-FC's cells Converter. It is based on vectorized models approach which was presented in [13]. Due to the complexity of balancing mechanisms, it is difficult to design directly a balance booster for a given balancing speed. For that reason in this proposed work, the experimental balance booster design is based on power consumption, and the different types of balance boosters are compared on the basis of equal losses using simulation results.

II. BALANCE BOOSTERS BASED ON PASSIVE COMPONENTS

A. Linear circuits

1) *Internal balance boosters*: The most simple way to balance the commutation cells is by adding parallel resistors R_{int} across each switch as depicted in Fig. 2 (a). In that case, a voltage is induced in the cell which also induces losses. But, it is also possible to use a $R_{int}C_{int}$ network in order to balance the commutation cells, relying on transition induced losses. It should be noted that, the performance of both techniques can be similar. However, when the converter is not operating or when the duty cycle is saturated, only the first technique operates and the effect of transition-induced losses disappears.

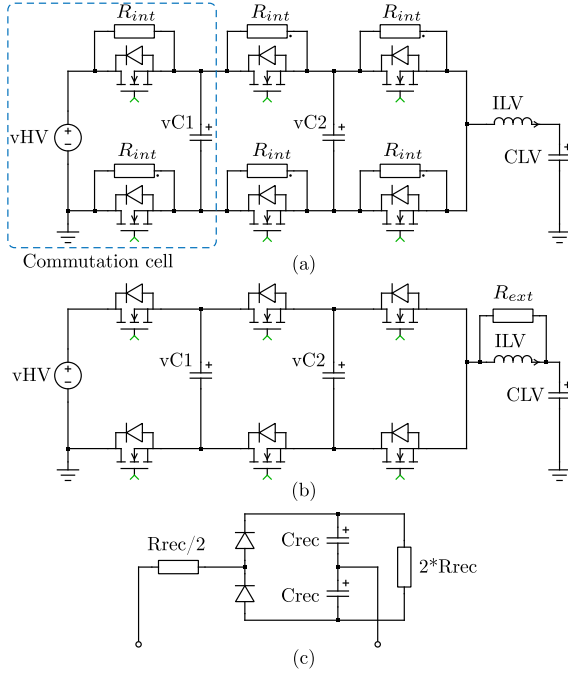


Fig. 2. Balance boosters. (a) Internal balance booster using level-induced losses. (b) External balance booster using level-induced losses. (c) Rectifier-based external balance booster.

It is possible to calculate the average power taken from a cell considering a level-based booster when only resistors are connected:

$$P_{int_{lb}} = \frac{v_{cell}^2}{R_{int}} \quad ; \quad v_{cell} = v_{HV} - v_{C1} \quad (1)$$

When the capacitor is included for the transition-based method, the power can be approximated as:

$$P_{int_{tb}} = 2C_{int}v_{cell}^2f_{sw} \quad (2)$$

2) *External balance boosters*: Another way to balance the voltage in the commutation cells is by lowering the impedance at the switching frequency, on the current source at the low voltage side [9]. It is possible to find some solutions based on passive networks and several filters. However, the simplest way to achieve the balancing is by an external resistor R_{ext} as depicted in Fig. 2 (b), and the average power dissipated in the balanced condition is:

$$P_{ext_{lb}} = \frac{1}{R_{ext}} \left(\frac{v_{HV}}{2n_S} \right)^2 \quad (3)$$

It is also possible to obtain a balancing effect using the transitions, and using a RC network connected in parallel with the smoothing inductor. In that case the power consumption can be calculated as:

$$P_{ext_{tb}} = C_{ext} \left(\frac{v_{HV}}{n_S} \right)^2 n_S f_{sw} \quad (4)$$

But in general terms it is not easy to find the best solution, because the speed of the balancing depends on many factors such as the phase of current harmonics, duty cycle and number of cells. The drawback using these techniques is that it will

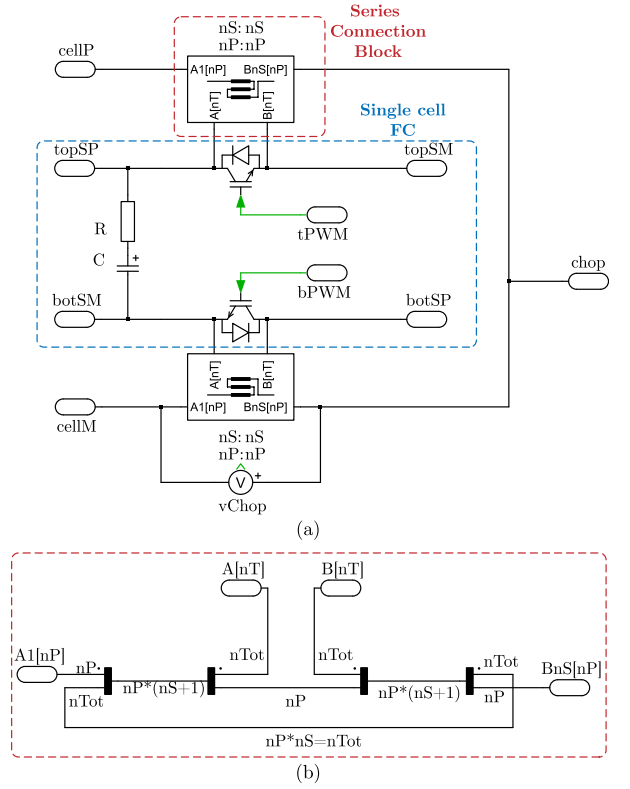


Fig. 3. (a) Vectorized model of the flying capacitor topology. (b) Vectorized model of a series connection.

take time until the last cell is charged, e.g. with a high number of cells. Another option allowing all cell voltages to increase together is by using a circuit with some storage and a rectifier as depicted in Fig. 2 (c). In that case, the resistors limit the amplitude of current pulses, and they can be designed to absorb a given amount of losses in balanced steady-state [14].

B. Non-Linear circuits

It is possible to improve the loss-speed trade-off by reducing the losses at steady-state, and increasing the reaction in case of strong imbalance.

1) *Internal balance boosters*: A simple non-linear solution is by using a zener diode or a device with a similar feature. As depicted in Fig. 1, depending on the voltage unbalance it is possible to control the required action. It can be modeled as a zener with a series resistor, and in the case of the transition-based model, a RC network with two back-to-back zener diodes can be connected.

Considering the circuit based on the zener voltage V_z and its series resistance R_z , the power taken from the cell is:

$$P_{intNL_{lb}} = \max \left(0; v_{cell} \left(\frac{v_{cell} - V_z}{R_z} \right) \right) \quad (5)$$

On the other hand, considering the RC network, the power can be approximated as:

$$P_{intNL_{tb}} = v_{cell} C_{int} (v_{cell} - V_z) f \quad (6)$$

2) *External balance boosters*: It is also possible to connect an external balance booster at the output side, by using a zener diode in series with the resistance. In that case, considering the worst case when the equivalent duty cycle ($D_{eq} = 50\%$) the power consumption under balanced voltage can be calculated as:

$$P_{extNLtb} = \frac{V_{HV}}{2n_S R_{ext}} \left(\frac{V_{HV}}{2n_S} - V_z \right) \quad (7)$$

If the RC network is considered, connected with the zener diodes, the power is expressed as:

$$P_{extNLtb} = \frac{V_{HV}}{n_S} C_{ext} \left(\frac{V_{HV}}{n_S} - 2V_z \right) n_S f_{sw} \quad (8)$$

And also the power losses of the rectifier circuit can be calculated as:

$$P_{rect} = \frac{\frac{V_{HV}}{n_S} \left(\frac{V_{HV}}{n_S} - v_{zrec} \right)}{4R_{rec}} \quad (9)$$

III. DESIGN OF THE MODEL BASED ON LOSSES

As was already discussed, there is a trade-off between the power losses and the speed of the balancing behavior. However, due to the complexity of models describing the balancing speed, it is necessary to define another parameter as the point of reference for the balance booster design. Therefore, a convenient input parameter is the power consumption P_{loss} , by the balance booster. Based on this criteria, it is possible to impose the same level for all the configurations and compare their balancing behavior and speed over the same evaluated profile.

In steady-state the voltage on a FC cell can be calculated as:

$$v_{cell} = \frac{V_{HV}}{n_S} \quad (10)$$

Moreover, in order to generalize the models the coefficient of non-linearity K_{NL} is also included. In that way, it is possible to include in the same equation both, the linear and non-linear approach considering that $K_{NL} = [0 - 1]$ for respective linear and non-linear circuits system.

A. Design of internal balance booster

For the level-based model, the most relevant considerations for the design are:

$$\begin{cases} vz_{intlb} = K_{NL} \frac{V_{HV}}{n_S} \\ R_{intlb} = \frac{n_P V_{HV} \left(\frac{V_{HV}}{n_S} - vz_{intlb} \right)}{P_{loss}} \end{cases} \quad (11)$$

By the same considerations, it is possible to derive the parameters for the transition-based model:

$$\begin{cases} vz_{inttb} = K_{NL} \frac{V_{HV}}{n_S} \\ C_{inttb} = \frac{P_{loss}}{2n_P V_{HV} \left(\frac{V_{HV}}{n_S} - vz_{inttb} \right) f_{sw}} \\ R_{inttb} = \frac{1}{10n_S C_{inttb} f_{sw}} \end{cases} \quad (12)$$

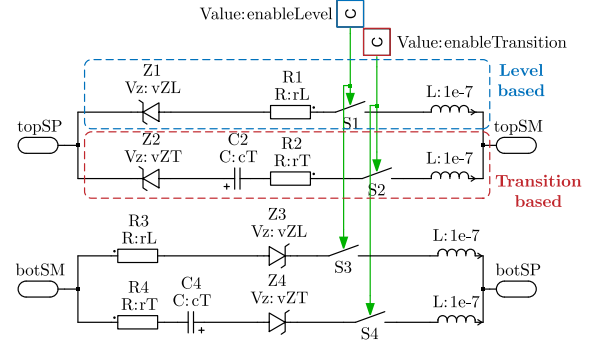


Fig. 4. Internal balance booster.

B. Design of external balance booster

Considering the case of the external balance booster, the equations for the design of the level-based balance boosters are:

$$\begin{cases} vz_{extlb} = K_{NL} \frac{V_{HV}}{2n_S} \\ R_{extlb} = \frac{n_P \frac{V_{HV}}{2n_S} \left(\frac{V_{HV}}{2n_S} - vz_{extlb} \right)}{P_{loss}} \end{cases} \quad (13)$$

It is also possible to derive the parameters for the transition-based model:

$$\begin{cases} vz_{exttb} = K_{NL} \frac{V_{HV}}{2n_S} \\ C_{inttb} = \frac{P_{loss}}{2n_P \frac{V_{HV}}{2n_S} \left(\frac{V_{HV}}{2n_S} - vz_{exttb} \right) 2n_S f_{sw}} \\ R_{exttb} = \frac{1}{10n_S C_{exttb} f_{sw}} \end{cases} \quad (14)$$

And finally for the rectified model:

$$\begin{cases} vz_{extrec} = K_{NL} \frac{V_{HV}}{n_S} \\ R_{extrec} = \frac{n_P \frac{V_{HV}}{n_S} \left(\frac{V_{HV}}{n_S} - vz_{extrec} \right)}{4P_{loss}} \\ C_{extrec} = \frac{1}{n_S R_{extrec} f_{sw}} \end{cases} \quad (15)$$

IV. VECTORIZED MODELS OF POWER CONVERTERS

One of the main features of the multicell converters is the high modularity, which allows designing one commutation cell and replicating it depending on the desired application. Not only the power commutation cell can be expanded but also the control scheme to operate the cell. It allows to make a general model and expand it to p-cells, which can be useful at the moment to evaluate and make a comparison of the converter performance. Especially, it can be a powerful tool when a new design or control method will be tested and it is necessary to get a first approach of the converter behavior. The basic cell of a FC converter is made by a pair of semiconductors and a flying capacitor. A n -level FC converter can be understood as a series connection of $n_S + 1$ -single FC cells ($n = n_S + 1$). This idea can be extended to an arbitrary vector of cells connected in series n_S and parallel n_P as depicted in Fig. 3 (a). In order to obtain this vectorized model of a series connection, the simulation scheme depicted in Fig. 3 (b) is implemented.

With this vectorized model of the FC converter, it is possible to verify the behavior of balance boosters. Considering that the internal balance boosters, depicted in Fig. 4, are connected

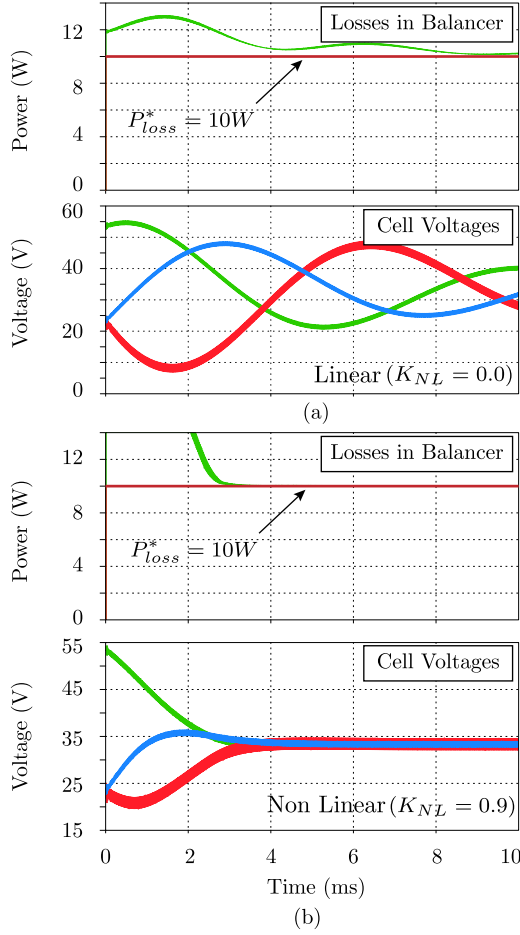


Fig. 5. Balancing waveforms for a level-based balance booster. (a) Linear ($K_{NL} = 0.0$). (b) Non-Linear ($K_{NL} = 0.9$).

on each commutation device, it is not necessary to create a vectorized model of this circuit. So that, the series model will also create the n_S internal balance boosters for the top device $topSP$, and bottom device $botSM$.

A. Internal balance booster model

Using the circuits depicted in Fig. 4 it is possible to test both the linear and non-linear internal balance boosters using the level-based and transition-based models. The results for some particular cases of linearity ($K_{NL} = 0$ and $K_{NL} = 0.9$) are depicted in Fig. 5. It is easy noticing that it was designed for a 3-cell FC converter and the action of the balance booster is operating as was expected.

It should be noted that the design allows maximum power losses of $P_{loss} = 10W$, and with the non-linear method not only the power losses reaches the reference faster than the linear circuit depicted in Fig. 5 (a), but also balance action presents a higher dynamic response.

B. External balance booster model

In the same way, it is possible to evaluate the external balance boosters using the same methodology based on vectorized models as depicted in Fig. 6 (a). However, in this case it is

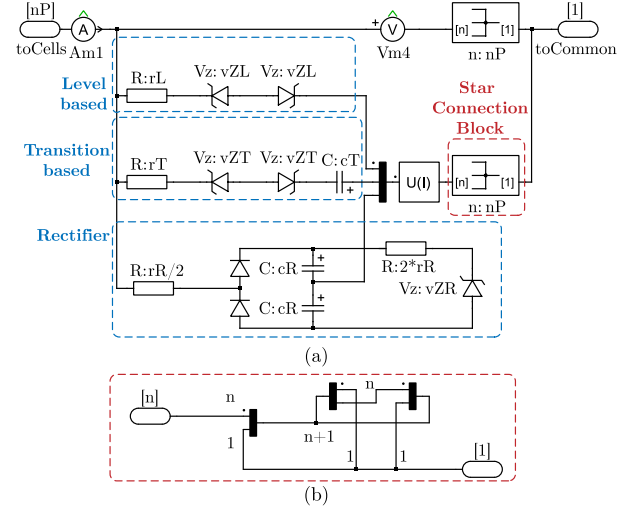


Fig. 6. (a) Model of the external balance booster. (b) Vectorized model of a star connection.

important to consider that the vectorized model of the FC converter can be made by series connection n_S of single cells, or by a parallel association of n_P cells. Considering the case when there are more than one cell $n_P \neq 1$, each cell will be connected to an individual inductor filter, which means that it will be required individual external balance boosters. For that reason, the vectorized model depicted in Fig. 6 (b) is required in order to create the star connection. The idea is to make an input vector of the electrical connection which share a common node. It is useful to evaluate configurations with many n_P parallel connections.

In the same way, it is possible to evaluate the different external balance boosters for the desired n_S and n_P commutation cells.

The results of the different balancing boosters are depicted in Fig. 7. In that case the reference of the allowed losses are $P_{loss} = 10W$, and as can be seen in all cases the values oscillate around this limitations. Moreover, depending on the design of the balance booster, the speed of the balancing can be adjusted. However, as was already mentioned it is not easy to find a general equation which allows controlling this parameter, and that is the motivation of the utilization of case-by-case evaluation.

V. EVALUATION CASE

The evaluation case is a non-isolated dc-dc bidirectional converter, which is composed of 12-FC's cells. The high-voltage side is connected to a regulated dc-bus with a nominal voltage of 650V. The low-voltage side can be connected to a lithium battery, super-capacitors or solar photovoltaic panels. This converter was developed for a french project focused on the integration of renewable sources, and storage systems. This project is explained in detail in [15]. The topology is used to filter the fluctuations in the dc-bus generated by the renewable energy sources, instead of filtering in the inverter side. The experimental prototype reaches an efficiency higher than 99.3%, and the main parameters are listed in the Table I.

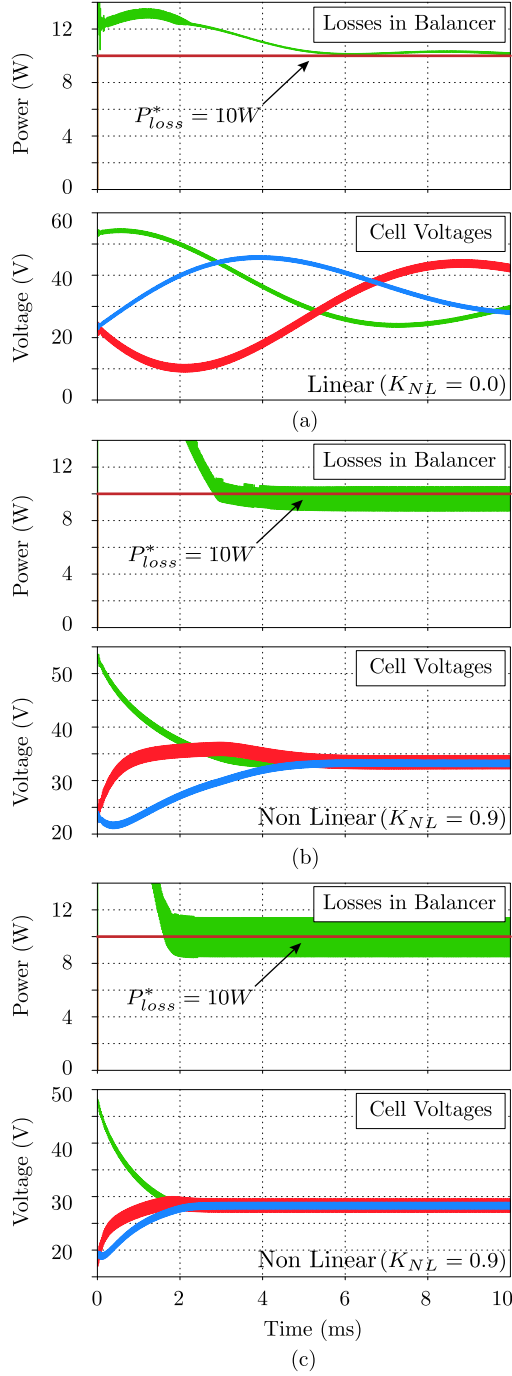


Fig. 7. Balancing behavior with different designs. (a) Linear external balance boosters (b) Non-linear external balance boosters (Transition based). (c) Non-linear external balance boosters (Rectifier based).

A. Simulation Results

A simplified circuit scheme of the evaluation case is presented in Fig. 8. The commutation cell is composed by 12-FC's cells, which can be described as a vectorized FC cell in the software PLECS® 16. The first step of the design of a Rectifier-based external balance booster, is made using the approach described above.

Under balanced conditions, the voltage across the inductor L_o is the difference between the chopped voltage, with a peak-

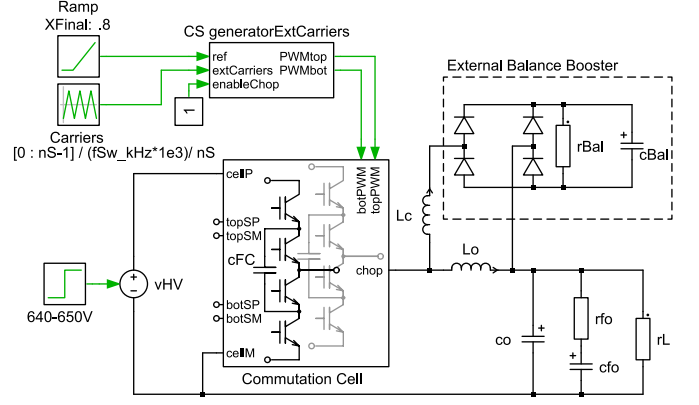


Fig. 8. Schematic diagram of the presented evaluation case.

peak amplitude of $\approx 54V$, and the output voltage equal to the average of the chopped voltage. Depending on the apparent duty cycle of the chopped voltage, the voltage across r_{Bal} can vary between $v_{rBal} = 27V$ (half the peak-peak value when apparent duty cycle 50%) and $v_{rBal} = 54V$ (if c_{Bal} has a very high value, L_c is negligible and apparent duty cycle is close to 0% or 100%). As a consequence, taking $r_{Bal} = 400\Omega$ it guarantees that steady state power consumption remains less than $7W$, and should be most of the time much lower.

The simulation results are presented in Fig. 9. A High-side voltage step change (640V-650V) is made at time $t=0.1s$. Without a balance booster circuit, the voltage cells oscillate but tend to remain unbalanced for quite a long time as shown in Fig. 9 (a). By contrast, connecting the external balance booster, as can be seen in Fig. 9 (b), the worst voltage unbalance is reduced and the 12-FC cell voltages tend to balance rapidly. The balance speed depends on the allowed losses in the external balance circuit. The chopped and load voltage are depicted in Fig. 9 (c), they vary depending on the apparent duty cycle. In addition, in this figure the resistor voltage in the balance booster is also shown, and we can see that it is, as predicted, lower than $54V$. The power consumption in the balance booster depicted in Fig. 9 (d), is much lower than $7W$.

With a balanced system, the inductor voltage v_{L_o} is a square wave with an amplitude equal to v_{HV}/n_S , a frequency $n_S f_{Sw}$ and a duty cycle $mod(n_S D, 1)$. This result is depicted in Fig. 10 (a) for a voltage $v_{HV} = 640V$. It is possible to check the peak-peak amplitude $v_{L_o} = 53.3V$ and period $8.33\mu s$. On the other hand, when no balance action is included, the voltage oscillation presents a behavior as shown

TABLE I
MAIN PARAMETERS OF THE EVALUATION CASE

Parameter	Name	Value
High side voltage	v_{HV}	650V
Switching frequency	f_{SW}	10kHz
Number of series cells	n_S	12
Flying capacitor	c_{FC}	60 μF
Balance cell capacitor	c_{Bal}	1 μF
Output inductance	L_o	100 μH

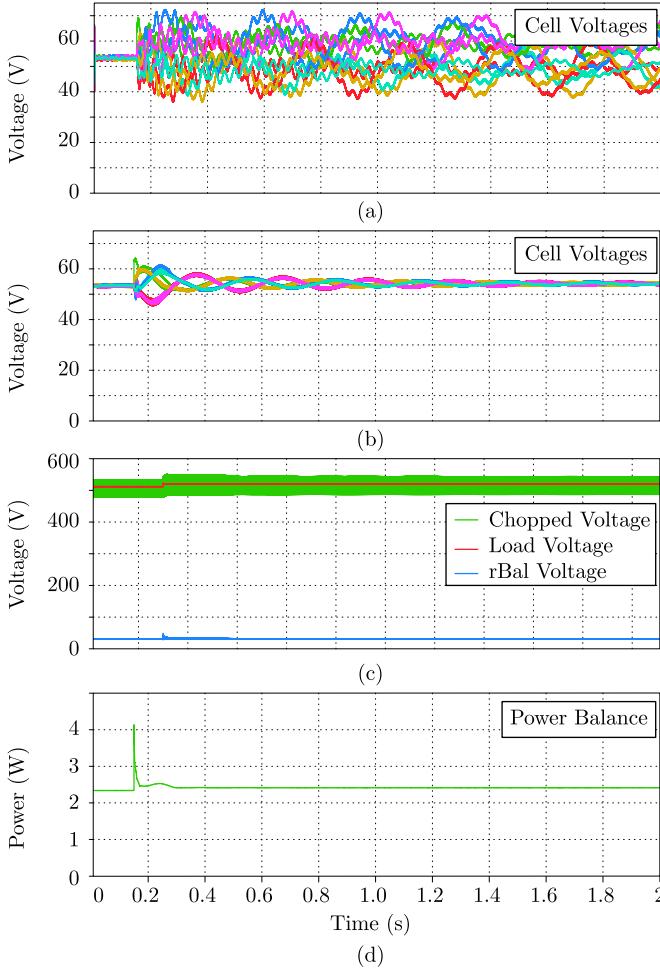


Fig. 9. Simulation results, high-side voltage step at $t=0.1s$. (a) Unbalanced cell voltages. (b) Rebalancing of cell voltages. (c) Chopped voltages. (d) Power losses in the balance booster.

in Fig. 10 (b). The voltage levels are different and the period is $100\mu s$. This behavior will last until the FC's cells reach the balanced voltage.

When a close-loop regulator is included, the modulation index changes after the high-side voltage step. It tends to balance faster the voltage on the FC's cells as can be seen in Fig. 11 (a). Moreover, the maximum voltage during the balancing operation is reflected on the envelope waveform of the inductor voltage as depicted in Fig. 11 (b).

B. Experimental Results

The proposed approach was validated with the experimental test-bench shown in Fig. 12 (a). The topology is the 12-FC's cells Converter, and the circuit is the same depicted in Fig. 8. The circuit parameters were listed in the Table I, and the power switch are (Mosfets IPB025N10N3 100V@180A) from Infineon supplier. Lab test are run using the control platform RTBOX from Plexim, which not only can be used as a HIL unit but also as a control platform due to its high fidelity PWM signal generator. The Mosfet driver, shown in Fig. 12 (b), receives the 10kHz pulses then it controls the turn-on and turn-off with the inner devices.

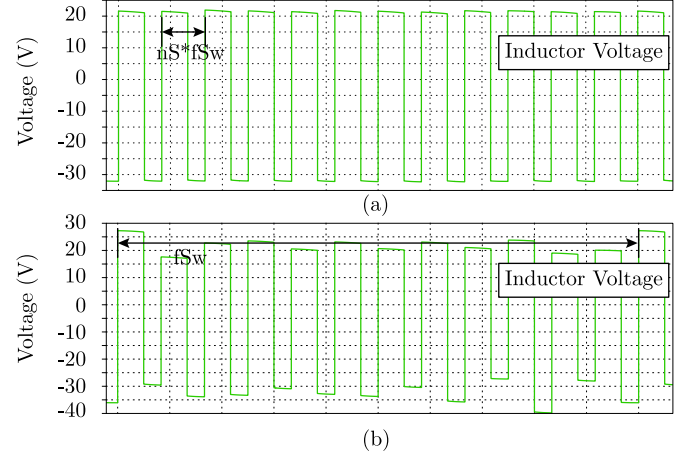


Fig. 10. Inductor voltage from simulation. (a) Balanced condition at $v_{HV}=640V$. (b) Unbalanced condition at $v_{HV}=650V$.

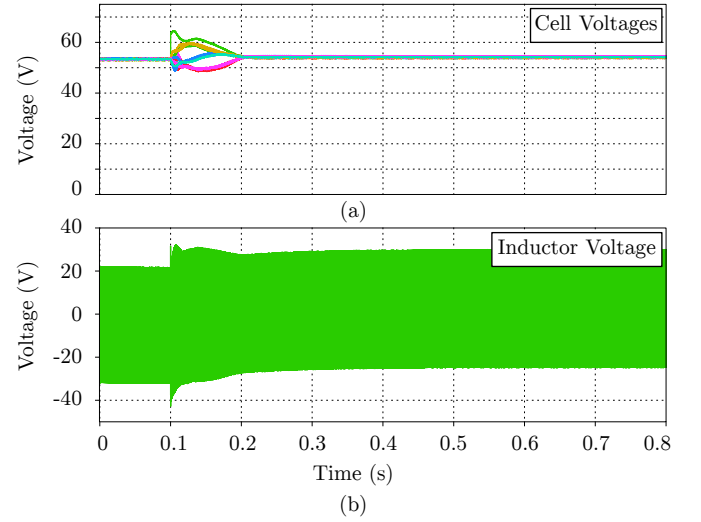


Fig. 11. Simulation results with a current close-loop control. (a) Rebalancing of cell voltages. (b) Inductor voltage.

The LV-side magnetic device is depicted in Fig. 13. It is possible to contrast the results with the simulation analysis. In case of balanced operation, Fig. 13 (a). The voltage levels are the same $v_{Lo} = v_{HV}/12$, only a difference in ripple of the top and bottom levels of the waveform can be noted. On the other hand, when a voltage step is made from $v_{HV}=640V$ to $650V$ the voltage levels are different as can be seen in Fig. 13 (b), it last until the voltage reaches the balanced condition. In Fig. 13 (c) it is possible noticing the envelope waveform of the inductor voltage. Due to the close-loop current control, the waveform presents a similar behavior as the simulation result, with a faster voltage balance action. The difference in the voltage amplitude in contrast with the simulation result shown in Fig. 11 (b), is due to the ripple in the top voltage seen in Fig. 13 (a).

VI. CONCLUSIONS

This work validates the proposed conceptual approach, by designing an external balance booster for an experimental

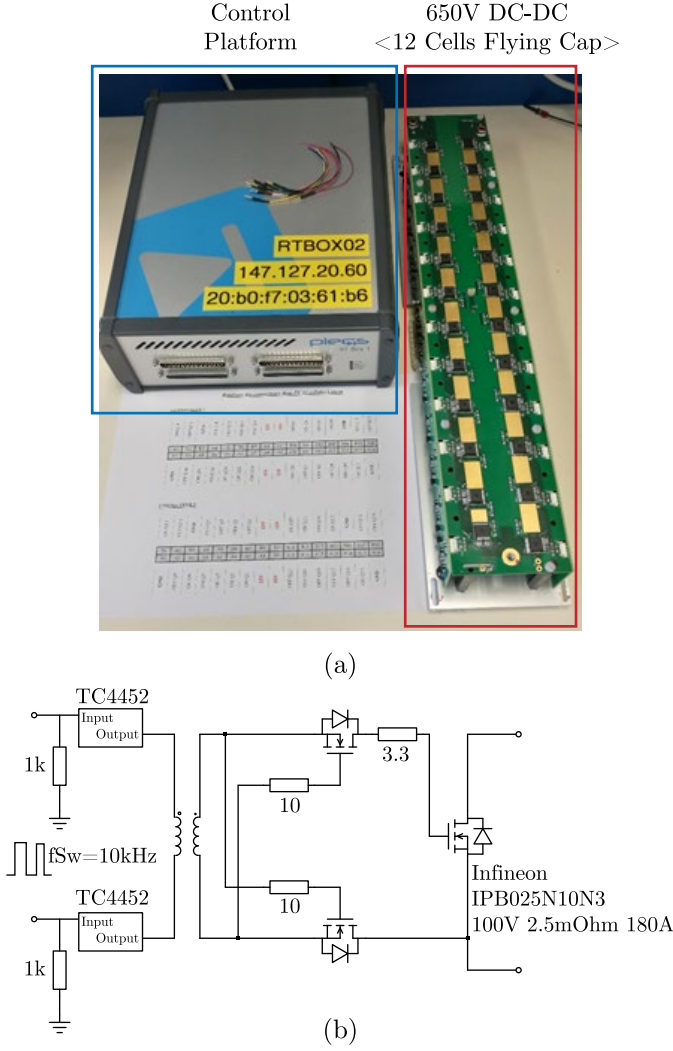


Fig. 12. Experimental test-bench. (a) Control Platform and 12-FC's cells Converter. (b) Mosfet Driver.

12-FC's cells Converter. The natural balance is an inherent behavior of the flying capacitor converter, however in order to reinforce the effect we may want to include some external boosters. In this work, the power consumption by the balance booster is set as the reference parameter, and based on this criteria the different balance boosters are designed and compared in simulations. From the simulation results, it is possible noticing that it would be better to use both internal and external balance boosters. The internal booster acts even when the converter is not switching. However, an external circuit have a significant balancing speed. In almost all designs a free external balance booster is included, so that core losses can be modeled as a paralleled resistor connected with the inductor. This effect must be reinforced with an external balance circuit, and this was the evaluation case in this work. In order to simplify the analysis, the vectorization concept of power circuits has been implemented in this paper. Finally, the evaluation of natural balance in multicell converters can be checked online at [16], and a fast and accurate comparison can be achieved.

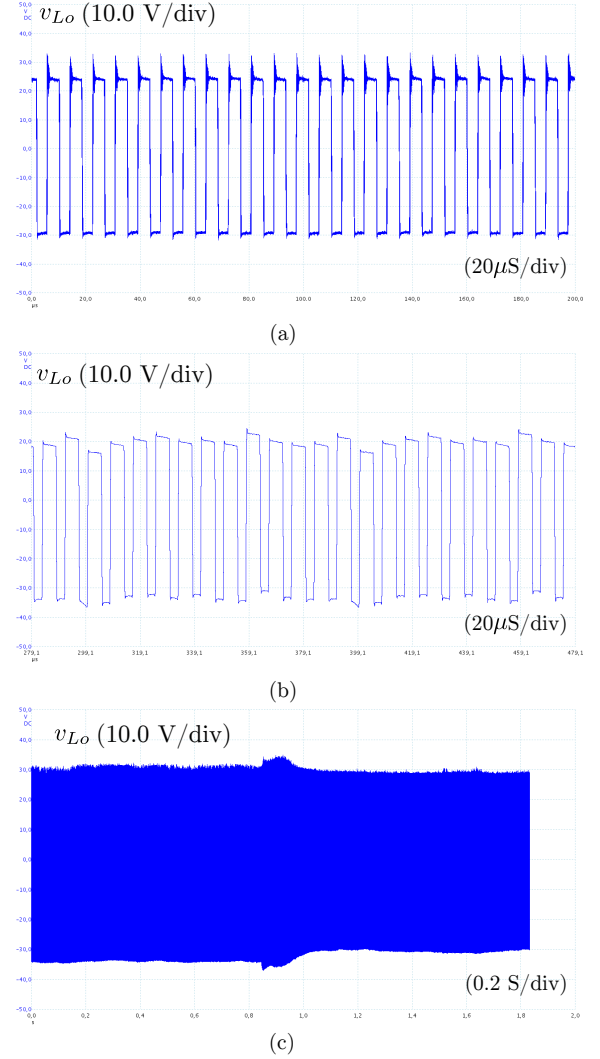


Fig. 13. Experimental Inductor voltage. (a) Balanced condition at $v_{HV}=640\text{V}$. (b) Unbalanced condition during the transition. (c) Inductor voltage.

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