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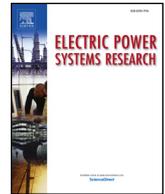
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A generalized open-end winding conversion system using flying capacitor cells

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ABSTRACT

Over the years, industrial processes, renewable energy systems and electrification of transport systems have been pushing power electronics equipment towards higher power ratings, quality and faster dynamics. In this context, several multilevel converter structures were developed and became popular, such as neutral-point-clamped, flying capacitor and cascaded half-bridge. This paper presents a generalized n -level converter using the multicell flying capacitor structure in an open-end winding configuration. A mathematical analysis shows that the proposed system presents the same output voltages as a traditional Δ/Y structure, but with less energy storage in the flying capacitors. The correlation with the traditional structure allows the use of an optimized modulation technique developed for the flying capacitor converter. It results in a voltage output with optimized harmonics, keeps the losses evenly distributed among the switching devices, and balances the voltages in the flying capacitors. Experimental results from a three-level conversion system and simulation results from a five-level structure demonstrate the features of the proposed topology.

1. Introduction

Over the last decades, several multilevel converter topologies were developed in order to achieve superior power, energy quality or dynamics over the traditional two level structure. Generally, they consist in different forms of connection between the switching devices and capacitive elements, producing multiple voltage steps at the converter output. A significant variety of topologies exist, each one with specific characteristics: number and ratings of switches, capacitors, necessity of isolated supplies, modularity, etc. The authors bring in [1], along with their own proposed topology, a comparison of several structures regarding the number of switches and capacitors. The neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB), nevertheless, were the ones that achieved higher acceptance and became widely known [2].

Another form of producing multilevel voltages in a drive system is the open-end winding (OEW) connection, first presented by Guggenbach and Stemmler in 1993 [3] and illustrated in Fig. 1. In this configuration, the load is not Y or Δ connected; instead, each side of the windings is fed by a converter. These can either be two-level or multilevel converters such as NPC or FC. At the grid side, a transformer isolates the two converters in order to avoid the circulation of common-mode currents through the circuit. One of the main advantages of this structure is the lower device count compared to a traditional Δ/Y

system with the same topology and number of levels. An OEW drive using dual three-level NPC converters, for example, presents the same voltage levels than a traditional five-level NPC, uses the same number of active switches, but less clamping diodes.

OEW structures have been reported for various applications, such as electrical and hybrid vehicles [4], aerospace [5], water pumping solar systems [6,7] and wind power [8,9], to name a few. Also, the combination of power converters with different number of levels [10,11] and topologies [12–14] have been proposed.

Along with the variety of structures, several modulation techniques were developed specifically for OEW systems, as the sub-hexagon strategies in [15–17], the carrier based in [18–20] and those with predefined switching sequences in [21,22]. Most of these techniques, however, propose an alternating role between the converters: while one of them is effectively switched, the other one is clamped at a certain switching state. With those strategies, the current ripple has the frequency of the converter switching, making them less attractive for high power devices, that switch at low frequencies. Some strategies are particular for a specific converter configuration, not being easy to be adapted for a different number of levels. Others lead to a poor distribution of losses between the switches, which can affect the converter life-time.

In this work, a generalized n -level OEW structure that employs flying capacitor cells is presented. It features some important

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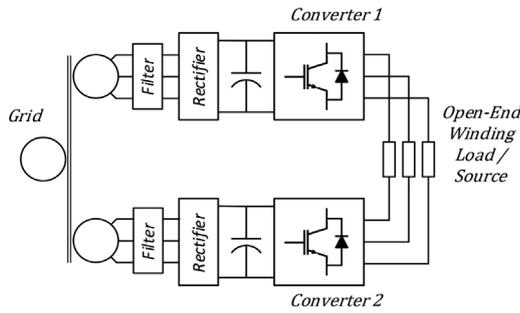


Fig. 1. Three-phase open end winding drive.

advantages:

- with FC multicell construction, increasing the voltage and/or the number of output levels is easily achievable by increasing the number of power cells;
- all switching devices (of both converters) present the same blocking voltage, which is a fraction of the voltage applied at the output;
- the total required energy storage of the flying capacitors is significantly lower than that of a traditional Δ/Y system;
- it employs the centered space vector pulse width modulation (CSVPWM) with state machine decoder [23,24], that lead to optimal harmonic content with an even distribution of losses among the devices, and is easily adaptable to different number of output levels.

Rather than the system proposition itself, which is formed by the combination of the well known FC and OEW technologies, the main contribution of this paper is the original mathematical description that correlates an OEW and a traditional multilevel structure: it is shown that, by directing the command signals to the proper devices in the OEW topology, the voltage output is exactly the same as it would be in a Δ/Y connected system, independently on the number of levels. This important observation makes it possible to the presented OEW structure to use optimized modulation techniques originally developed for traditional FC drives, such as the CSVPWM with state machine decoder.

Besides that, a novel analytical comparison of the energy stored in the flying capacitors is presented, concluding that the multilevel FC configuration in an OEW fashion demands less storage than the corresponding Δ/Y system.

The development of these mathematical expressions are presented in Section 2. In Section 3, the CSVPWM with state machine decoder is described. Finally, Sections 4 and 5 present simulation results of a five-level structure and experimental results from a 2 kW test bench in a three-level configuration, respectively, demonstrating the features and feasibility of the structure.

2. System modeling

In this section, the output voltage equations of the proposed OEW system is presented as a function of the switching command signals. First, the analysis is developed for a three-level system, comparing the OEW structure with a traditional FC converter in order to show the equivalence between both topologies. Then, the system is generalized for a n -level OEW structure. Finally, a mathematical analysis of the energy stored in the flying capacitors evidences its important reduction on the OEW system compared to the traditional structure.

2.1. The three-level converter

The analysis begins by resuming the voltage equations of the traditional three-level flying capacitor, shown in Fig. 2. The DC-link and the flying capacitors are charged with a $v_{dc}/2$ voltage and the load is an equilibrated impedance ($Z_a = Z_b = Z_c$). n' is the DC-link midpoint and n

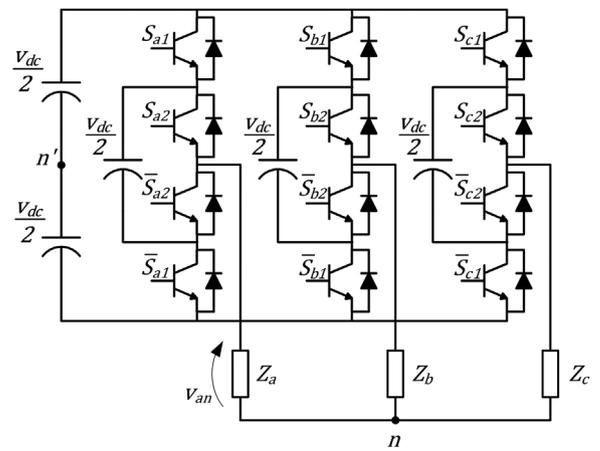


Fig. 2. Three-level flying capacitor power structure.

is the common point of the star-connected load. The command signals of the top switching devices are $S_{xj} \in \{1, 0\}$, and for the bottom switches the complementary \bar{S}_{xj} , where $x \in \{a, b, c\}$ and $j \in \{1, 2\}$.

The equations for the phase voltages in this system are

$$\begin{aligned} v_{an} &= v_{an'} - v_{nn'} \\ v_{bn} &= v_{bn'} - v_{nn'} \\ v_{cn} &= v_{cn'} - v_{nn'} \end{aligned} \quad (1)$$

The converter output voltage for any of the phases, $v_{xn'}$, can be written as a function of their respective command signals and the DC-link voltage:

$$v_{xn'} = -\frac{v_{dc}}{2} + \frac{v_{dc}}{2}(S_{x1} + S_{x2}) \quad (2)$$

From (2) it can be seen that the output voltage can assume three different levels ($0V, \pm v_{dc}/2$), with two redundant switching states producing the zero value.

Once the points n and n' are isolated, there is no path for circulation of zero-sequence currents. The voltage $v_{nn'}$ can, then, be expressed as

$$v_{nn'} = \frac{v_{an'} + v_{bn'} + v_{cn'}}{3} \quad (3)$$

Now, a similar analysis is carried out for the three-level OEW drive shown in Fig. 3. The winding voltages equations are

$$\begin{aligned} v_{aa'} &= v_{ao} - v_{a'o'} - v_{o'o} \\ v_{bb'} &= v_{bo} - v_{b'o'} - v_{o'o} \\ v_{cc'} &= v_{co} - v_{c'o'} - v_{o'o} \end{aligned} \quad (4)$$

The individual output voltages of the converters are

$$\begin{aligned} v_{x_o} &= -v_{dc}/4 + v_{dc}/2(S_{x1}) \\ v_{x'o'} &= v_{dc}/4 - v_{dc}/2(S_{x2}) \end{aligned} \quad (5)$$

and their subtraction leads to the total output voltage

$$v_{out_x} = v_{x_o} - v_{x'o'} = -\frac{v_{dc}}{2} + \frac{v_{dc}}{2}(S_{x1} + S_{x2}) \quad (6)$$

Considering that there is no connection between points o and o' , no common-mode currents circulate in this system. Thus, the voltage $v_{o'o}$ can be written as

$$v_{o'o} = \frac{(v_{ao} - v_{a'o'}) + (v_{bo} - v_{b'o'}) + (v_{co} - v_{c'o'})}{3} \quad (7)$$

A direct comparison shows that (6) = (2), i.e. $v_{x_o} - v_{x'o'} = v_{xn'}$. That is achieved by directing the S_{x1} command signals to the TOP switches of converter 1 and the S_{x2} signals to the BOTTOM switches of converter 2 in the OEW structure, as depicted in Fig. 3.

That way, $v_{o'o} = v_{nn'}$ ((7) = (3)) and, therefore, it is possible to note that both topologies produce the same voltage pattern (4) = (1). This observation leads to the conclusion that modulation techniques

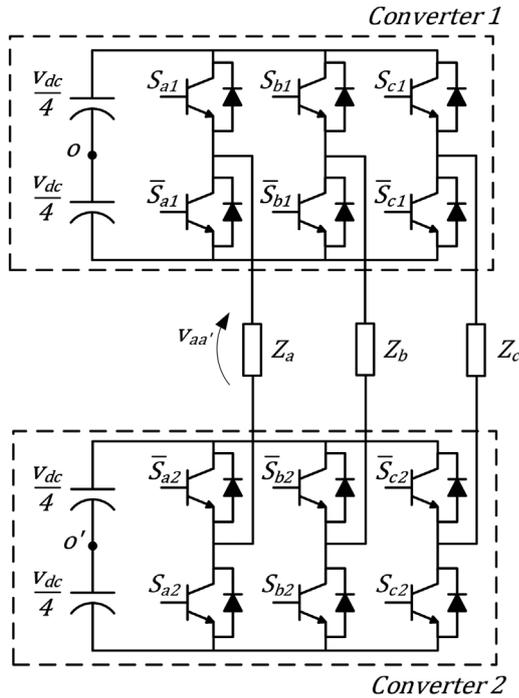


Fig. 3. Three-level open end winding power structure.

developed for three-level FC converters can be directly employed in a OEW system, leading to similar voltage waveforms.

2.2. An n-level converter

As the previous analysis showed the equivalence between three-level OEW drives and FC converters, this section presents the mathematical generalization for a n-level system. Fig. 4 shows the power structure for one phase of a generalized n-level multicell flying capacitor converter. It is composed of (n - 1) = m power cells, and the kth cell has a DC voltage of (k/m)v_{dc} across its flying capacitor. With such configuration, the blocking voltage of the semiconductor devices is v_{dc}/m [25].

The output voltage of such converter can be expressed as

$$v_{xo} = -\frac{v_{dc}}{2} + \frac{v_{dc}}{m} \left(\sum_{k=1}^m S_{xk} \right) \quad (8)$$

These FC cells can be employed in a three-phase OEW configuration, leading to the system presented in Fig. 5. Converter 1 uses m₁ cells and converter 2 uses m₂ cells per phase. The DC-link voltages are proportional to the number of cells of each converter:

$$\begin{aligned} v_{dc1} &= v_{dc} \left[\frac{m_1}{m_1 + m_2} \right] \\ v_{dc2} &= v_{dc} \left[\frac{m_2}{m_1 + m_2} \right] \end{aligned} \quad (9)$$

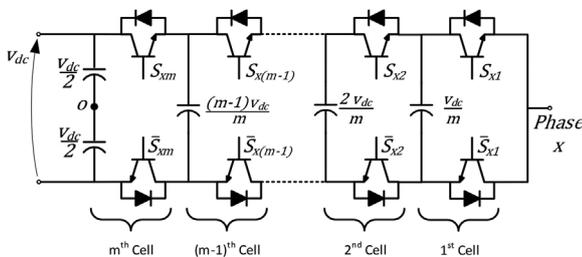


Fig. 4. n-level flying capacitor converter (one phase shown).

The converters output voltages can be written as

$$\begin{aligned} v_{xo} &= -\frac{v_{dc}}{2} \frac{m_1}{m_1 + m_2} \\ &+ \frac{v_{dc}}{m_1} \frac{m_1}{m_1 + m_2} \left(\sum_{k=1}^{m_1} S_{xk} \right) \\ v_{x'o'} &= \frac{v_{dc}}{2} \frac{m_2}{m_1 + m_2} \\ &- \frac{v_{dc}}{m_2} \frac{m_2}{m_1 + m_2} \left(\sum_{k=1}^{m_2} S_{x'k} \right) \end{aligned} \quad (10)$$

which lead to the output voltage expression

$$\begin{aligned} v_{outk} &= v_{xo} - v_{x'o'} \\ &= -\frac{v_{dc}}{2} + \frac{v_{dc}}{m_1 + m_2} \left(\sum_{k=1}^{m_1} S_{xk} + \sum_{k=1}^{m_2} S_{x'k} \right) \end{aligned} \quad (11)$$

By comparing (11) with (8), one can see the correlation between this OEW system and a traditional (Δ/Y) flying capacitor drive with (m₁ + m₂) cells. Both systems have the same number of switches, with equal switching states redundancy and all switching devices have the same blocking voltage, which is v_{dc}/(m₁ + m₂) volts.

This is a very interesting feature, as it allows the OEW drive to use modulation techniques originally developed for FC converters. Section 3 presents a modulation strategy that provides a voltage output with optimized harmonic distortion and evenly distribute the commutations between the switching devices in both FC and OEW systems.

2.3. Flying capacitors stored energy

One of the main advantages of the OEW configuration compared to the traditional one is presenting lower energy storage on the flying capacitors.

First, let's consider a traditional Δ/Y system employing a FC converter with m cells. The capacitance of the flying capacitors is determined according to the admissible voltage ripple on the switching devices Δv_{sw}. Being I_{max} the maximum current and f_{sw} the switching frequency [25]:

$$C_{fc} = \alpha \frac{I_{max}}{\Delta v_{sw} f_{sw}} \frac{1}{m} \quad (12)$$

The α variable is introduced to represent different conditions:

- m = 1 → α = 0: No flying capacitors are employed (two-level converter);
- m = 2 → α = 1: There is one flying capacitor per phase. The DC-link, with its high capacitance value, normally presents a voltage ripple much lower than that of the FC. That being considered, we can assume that Δv_{sw} corresponds to the FC voltage ripple;
- m > 2 → α = 2: There are at least two flying capacitors per phase. In this case, a switching device placed between two FCs can be submitted to twice their voltage ripple. That is why the capacitance is doubled: to ensure that their ripple is lower than Δv_{sw}/2.

The voltage in the kth cell is v_k = (k/m)v_{dc}, so the total stored energy in the flying capacitors is

$$\begin{aligned} W_{fc} &= \sum_{k=1}^{m-1} \left(\frac{1}{2} C_{fc} v_k^2 \right) \\ &= \frac{1}{2} \alpha \frac{I_{max}}{\Delta v_{sw} f_{sw}} \frac{1}{m} \frac{v_{dc}^2}{m^2} \sum_{k=1}^{m-1} k^2 \end{aligned} \quad (13)$$

Now let's assume the equivalent OEW structure, which employs dual converters of m/2 cells and v_{dc}/2 DC-link voltage. Keeping the same design parameters, the capacitance of the flying capacitors is given by

$$C_{oew} = \beta \frac{I_{max}}{\Delta v_{dc} f_{sw}} \frac{1}{m} \quad (14)$$

where β also has the purpose of representing the different constraints

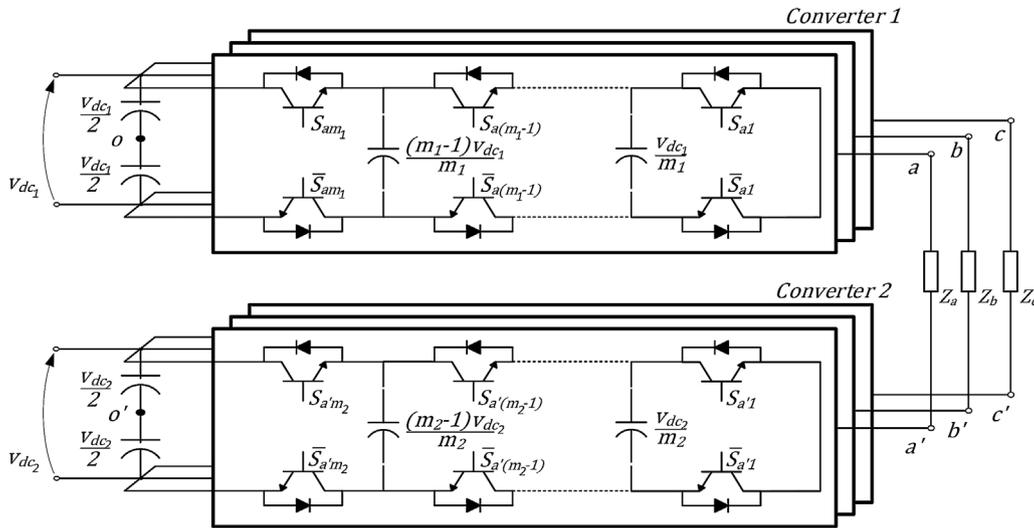


Fig. 5. n-level open-end winding converter based on flying capacitor cells.

related to the number of cells:

- $m = 2 \rightarrow \beta = 0$: No flying capacitors are employed (dual two-level converters);
- $m = 4 \rightarrow \beta = 1$: There is one flying capacitor per phase per converter (dual three-level converters), so Δv_{sw} corresponds to the FC voltage ripple;
- $m > 4 \rightarrow \beta = 2$: There are at least two flying capacitors per phase per converter. The capacitance is doubled to ensure that their ripple is lower than $\Delta v_{sw}/2$.

Taking into account their voltages, the total stored energy become

$$W_{oew} = \frac{1}{2} C_{oew} \left[2 \sum_{k=1}^{(m/2)-1} \left(\frac{k}{m/2} \frac{v_{dc}}{2} \right)^2 \right] = \frac{1}{2} \beta \frac{I_{max}}{\Delta v_{fc}/f_{sw}} \frac{1}{m} \frac{v_{dc}^2}{m^2} \left[2 \sum_{k=1}^{(m/2)-1} k^2 \right] \quad (15)$$

Finally, by dividing (13) for (15), the relation between the stored energies in the two systems is found:

$$\frac{W_{fc}}{W_{oew}} = \left[\frac{\alpha}{\beta} \right] \left[\frac{\sum_{k=1}^{m-1} k^2}{2 \sum_{k=1}^{(m/2)-1} k^2} \right] \quad (16)$$

The term in the first brackets of (16) is related to the capacitance values, while the second term is due to the voltage values across the flying capacitors. Fig. 6 presents the values of this relation for systems with 4 to 30 cells (for 2 cells, the OEW configuration have no flying capacitors).

One can observe that a 4-cell (five-level) OEW structure needs 14 times less energy storage in the flying capacitors than the traditional FC converter, and, although this relation decreases as the number of cells is increased, for 30 cells a relation of over 4 times still remains. An important improvement in power density can be achieved by using the

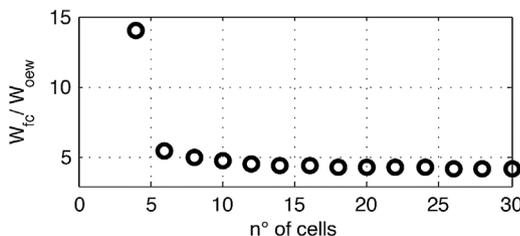


Fig. 6. Relation between the stored energy in the flying capacitors of a traditional FC system compared to an OEW system.

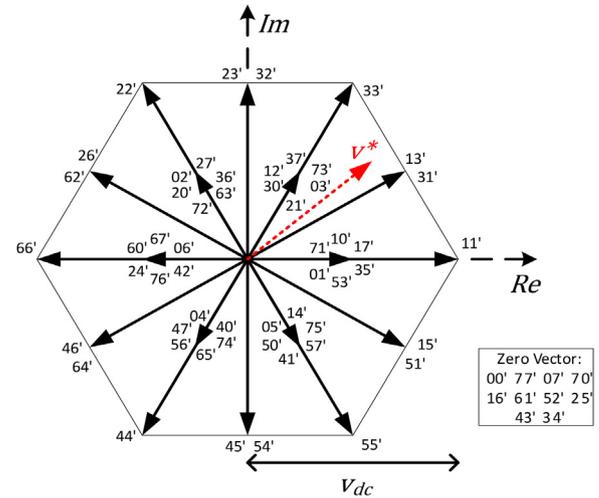


Fig. 7. Voltage space vectors produced by an OEW three-level conversion system.

OEW configuration.

3. Modulation technique

Fig. 7 shows the voltage space vectors produced by the three-level OEW converter of Fig. 3. It shows also an instantaneous reference voltage vector. The switching states that produce each vector are represented by a two-digit number xy' , where the first digit x refer to the switching state from converter 1 and the second digit y' refer to the state from converter 2. As an example: the state $12'$ stands for $S_{c1}, S_{b1}, S_{a1} = 001$ and $S_{c2}, S_{b2}, S_{a2} = 010$.

It is well known that in order to achieve the best modulation performance with respect to the output harmonic distortion, the three nearest voltage space vectors must be used to synthesize the voltage reference [26]. The vectors application times are calculated in order to achieve an average value that corresponds to the reference vector [27] and the application time of redundant vectors must be evenly distributed along one switching period [28]. This modulation technique is known as space-vector modulation (SVM).

The SVM, although efficient, is a difficult technique to be implemented when compared to carrier-based strategies [29]. Fortunately, it has already been shown by [30] (for two-level) and [23] (for multilevel converters) that the same modulation profile from SVM

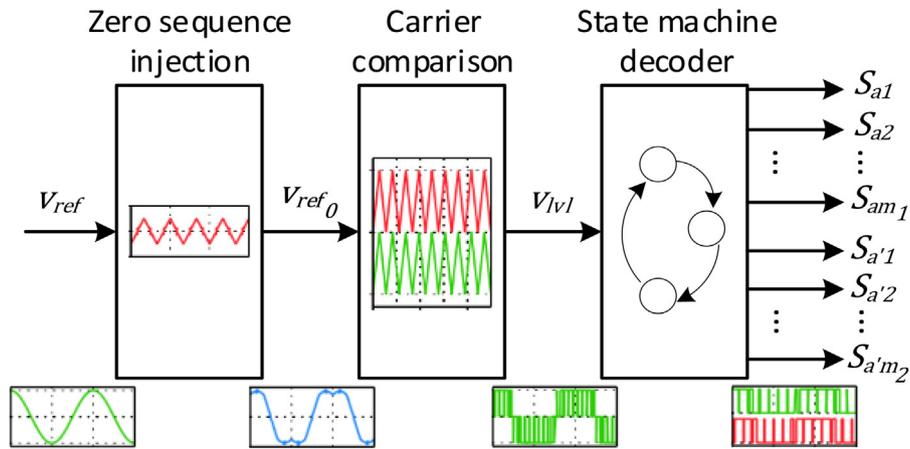


Fig. 8. Block diagram of the CSVPWM with state machine decoder.

can be achieved with carrier-based PWM, if the correct common mode voltage is added to the three-phase sinusoidal references.

Fig. 8 presents a block diagram of the modulation technique used in the proposed OEW configuration. It is called centered space vector pulse width modulation (CSVPWM) with state machine decoder [24].

The first block in Fig. 8 is the calculation of a zero-sequence signal that is added to the original references in order to evenly distribute the space vectors in the switching period. This signal is calculated through ((17)–(19)), as described in [23], being v_a, v_b and v_c the voltage sinusoidal references and $i \in \{a, b, c\}$:

$$v'_i = v_i - \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \quad (17)$$

$$v''_i = \left[v'_i + (n - 1) \frac{v_{dc}}{2} \right] \bmod (v_{dc}) \quad (18)$$

$$v_i^* = v'_i + \frac{v_{dc}}{2} - \frac{\max(v''_a, v''_b, v''_c) + \min(v''_a, v''_b, v''_c)}{2} \quad (19)$$

Fig. 9 presents the original voltage references, the zero sequence

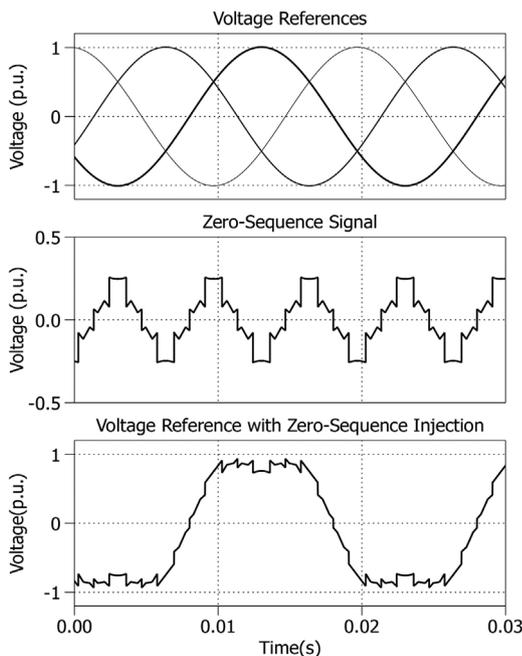


Fig. 9. Waveforms concerning the first stage of the CSVPWM with state machine decoder for a five-level system: original voltage references, zero-sequence signal and resulting voltage reference.

signal and the resulting voltage reference (v_i^*) for a five-level converter.

Those resulting reference values (v_i^*) are then compared to triangular carriers in the second block of Fig. 8. $n - 1$ carrier waveforms are disposed vertically between the voltage levels, with the same phase, and their frequency correspond to the switching frequency multiplied by $(n - 1)$. The outcome of this comparison is the theoretical converter output voltage. Following the five-level converter example, the reference-carrier comparison and its resulting signal are presented in Fig. 10.

Based on the voltage levels that result from the carrier comparison, the command signals for the switching devices must be determined. This is not a simple task for multilevel converters, as different switching combinations can result in the same voltage level at the output, and this redundancy grows as the number of levels of the converter is increased.

In [24] the authors proposed the use of a state machine decoder to determine the signals to command the switches in a FC structure. Fig. 11 shows the example of the decoder for a three-level system: the states are the voltage levels, represented in the circles with their corresponding switching combinations in brackets, and the arrows depict the transitions between levels.

The state machine is built in such a way that the redundant states are used to avoid uneven distribution of commutations and narrow pulses, equally distributing the losses among the switching devices and

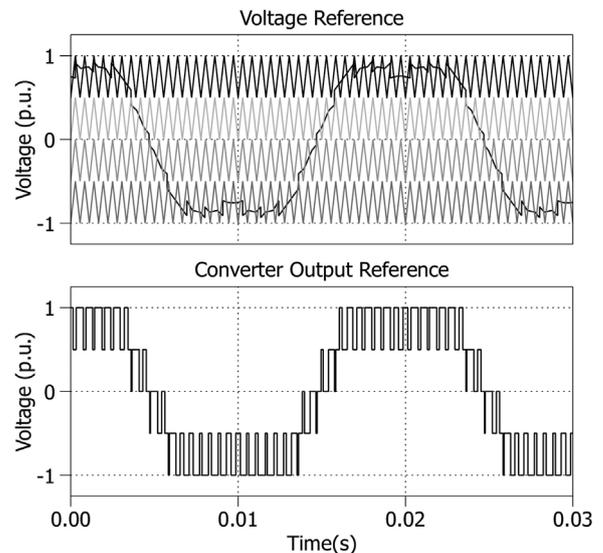


Fig. 10. Waveforms concerning the second stage of the CSVPWM with state machine decoder for a five-level system: voltage reference-carrier comparison and theoretical converter output voltage.

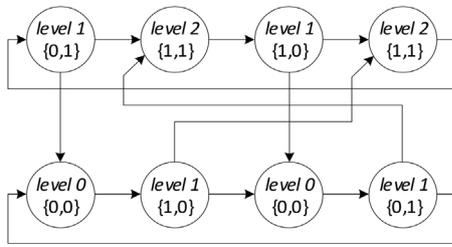


Fig. 11. State machine decoder for a three-level FC converter.

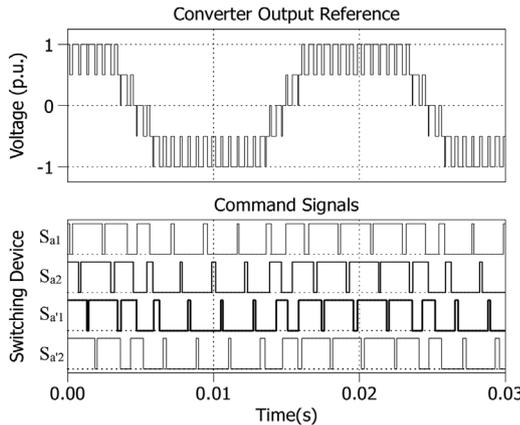


Fig. 12. Waveforms concerning the third stage of the CSVPWM with state machine decoder for a five-level system: converter output voltage reference and state machine resulting command signals.

keeping the flying capacitor voltages balanced. It grows in size as the number of levels (and redundancy) increase, as the example for a five-level system in [24], but its principle can be generalized for n -levels for a digital implementation. Fig. 12 brings again the converter theoretical output voltage together with the resulting command pulses. These are the input and output, respectively, of the third and final block in Fig. 8.

As shown in the previous section, the voltage output equations of the proposed OEW structure are equivalent to those of the FC topology, which permits using the same state machine decoder. One must pay attention, however, to the fact that the first m_1 command signals are addressed to the TOP switches of converter 1, and the other m_2 signals are addressed to the BOTTOM switches of converter 2.

4. Simulation results

In order to exemplify the discussion presented on Section 2, two systems were simulated and compared: a five-level flying capacitor traditional drive and its equivalent OEW structure. Their circuits are illustrated in Fig. 13 and their parameters are presented in Table 1. Simulation was carried out using Plexim's PLECS®.

There are certain aspects of these systems which are important to highlight:

- They are commanded by the same signals S_{xj} but, in the OEW system, S_{x3} and S_{x4} are directed to the bottom devices of converter 2;
- The loads are the same (RL circuit);
- Following Eqs. (12) and (14), the traditional five-level structure demands two times the flying capacitance compared to the OEW configuration;
- Once the purpose of these simulations is to evaluate the general functioning of the systems, fixed amplitude voltage references were directly used for the modulation strategy, i.e. no control technique is employed;

- The modulation depth is determined by the relation between the peak of the reference phase voltage and the DC-link voltage: $m_d = v_{pk}^*/(v_{dc}/2)$

Fig. 14 presents the load phase voltages produced by these systems (using the same command signals): v_{an} for the traditional FC and $v_{aa'}$ for the OEW. One can observe that the two systems produce the same load voltage, as stated in Section 2 by Eqs. (11) and (8).

With the same load values, and producing the same voltage, the resulting currents for both systems is also the same. For the OEW system under rated condition, the output current is presented in Fig. 15 and its harmonic spectrum is depicted in Fig. 16. The frequency of the main current ripple is 3600 Hz. This is eight times the switching frequency, a relation that comes from the combination of two effects of the CSVPWM with state machine decoder: first, by taking advantage of the redundant switching states the resulting voltage has $(n - 1)$ times the switching frequency; secondly, by centering the voltage space vectors in the switching period, the first commutation harmonic of the voltage is highly compensated between phases [31].

A comparison between the voltage ripple in the flying capacitors of both systems is presented in Fig. 17. The shown values correspond to the capacitors connected between switches S_{a1} and S_{a2} , which are charged to $v_{dc}/4$. Once the traditional configuration employs twice as much capacitance, it naturally presents half the voltage ripple in the capacitors.

The main concern during design, however, is the blocking voltage of the switching devices rather than the ripple of the capacitors itself. By looking at the voltage on the switch S_{a2} for both systems, presented in Fig. 18, one can see how their maximum values are practically the same, even though the ripple on the capacitor voltages are different. The point here is that the switching device, in the traditional structure, stands between two flying capacitors; therefore it can be submitted up to twice their ripple. In the five-level OEW configuration, on the other hand, no switching device is placed between two flying capacitors, so their blocking voltages have the same ripple as the capacitors. This example illustrates the discussion presented in Section 2.3, showing that it is possible to achieve the same voltage output, with the same power, but with less energy storage in the flying capacitors on the OEW structure compared to the traditional one.

The voltage balancing and stability among the flying capacitors is very important to guarantee that the switching devices are not submitted to above rated voltages. For traditional FC systems, it has been already shown that the CSVPWM ensures the natural balancing of these voltages [24]. In order to show that this is also true for the OEW structure, two simulated events are presented: a start-up with unbalanced charged capacitors and a modulation depth step. The response to these events is presented in Fig. 19.

At the start-up, the flying capacitors of converter 1 are charged to 90% of its nominal value, and those from converter 2 are charged to 110%. This is an abnormal condition, as the capacitors are normally precharged to their operating values, but the analysis is useful in the sense that it demonstrates how the voltages converge over time to their target values. Several precharge methods have been presented in the literature for FC converters [32–34] and could be applied to OEW systems based on FC cells. They consist in different forms of commanding the switching devices and external contactors, in order to charge the capacitors using resistors to limit the current.

The second simulated event was a step of the modulation depth, from 1.0 to 0.5, at the instant depicted in Fig. 19. Once again, the disturbed voltages converge back to their operating values, demonstrating that the CSVPWM with state machine decoder is able to maintain the natural balance of the flying capacitors after a reference voltage transient.

Another important feature achieved by using this modulation technique in the traditional structure is the equilibrated power distribution between the switching devices. In order to evaluate if this is

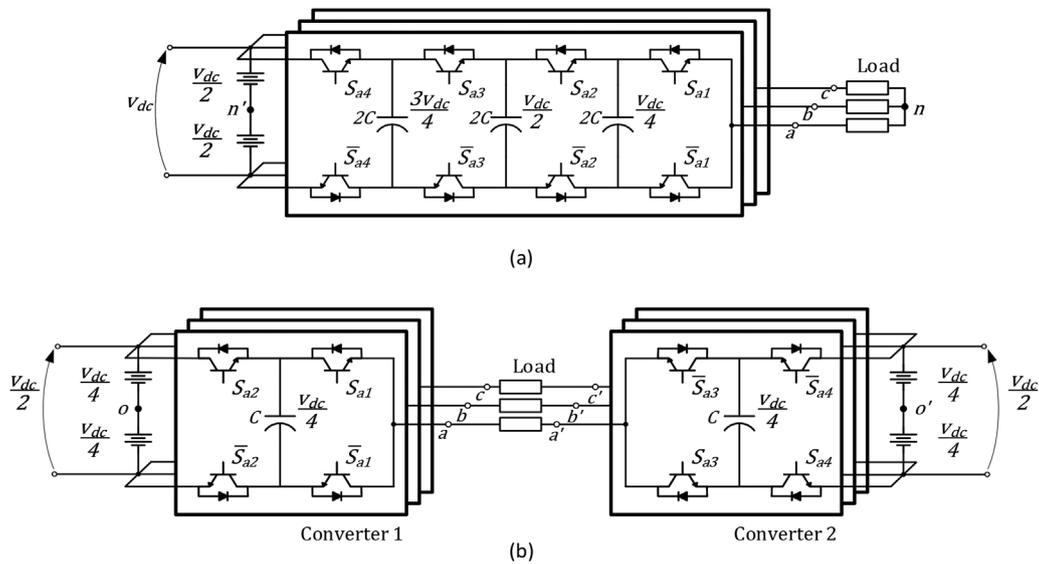


Fig. 13. Five-level simulated circuits: (a) traditional flying capacitor and (b) its OEW equivalent structure.

Table 1
System simulation parameters.

Parameter	Value
Total DC-link voltage (v_{dc})	3600 V
Load RMS current	500 A
Load RMS phase voltage	1328 V
Load frequency	50 Hz
Load power	2 MVA
Load power factor	0.95
Switching frequency	450 Hz
Switching devices voltage ripple	1% v_{dc}
Base flying capacitance (C)	11.5 mF

also valid for the OEW system, the losses of its switching devices were calculated, according to the modeling presented by [35]. Conduction losses are determined using the transistor's collector-emitter voltage vs.

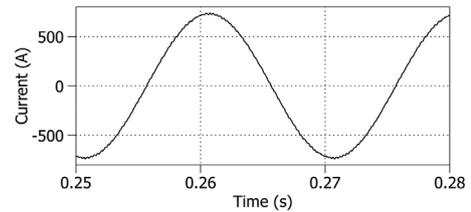


Fig. 15. Simulated load current of the five-level OEW configuration under rated conditions.

collector current curve and diode's forward voltage vs. forward current curve, supplied by the manufacturer. Instantaneous power dissipation is calculated and then averaged over one fundamental period. Switching losses are computed from the transistor's turn-on and turn-off energy curves and diode's reverse recovery energy, both functions of the conduction current. The energy is then integrated over one fundamental

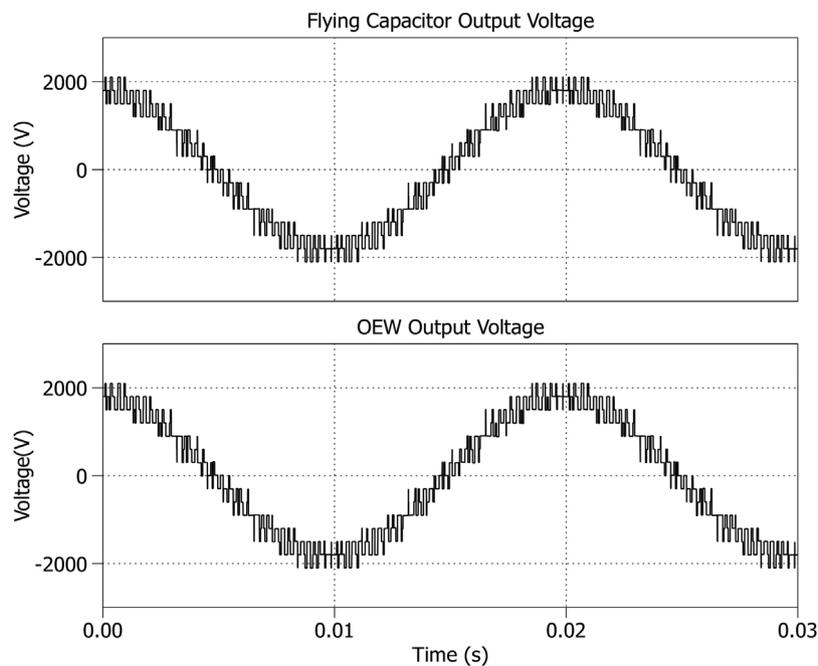


Fig. 14. Simulated load phase voltage for the traditional (v_{an}) and OEW systems ($v_{aa'}$).

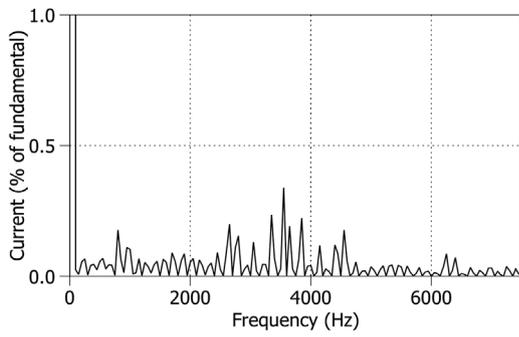


Fig. 16. Harmonic spectrum of the simulated current in the five-level OEW configuration.

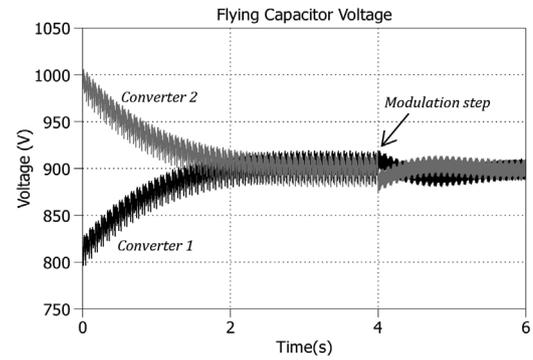


Fig. 19. Flying capacitors voltage in the five-level OEW system.

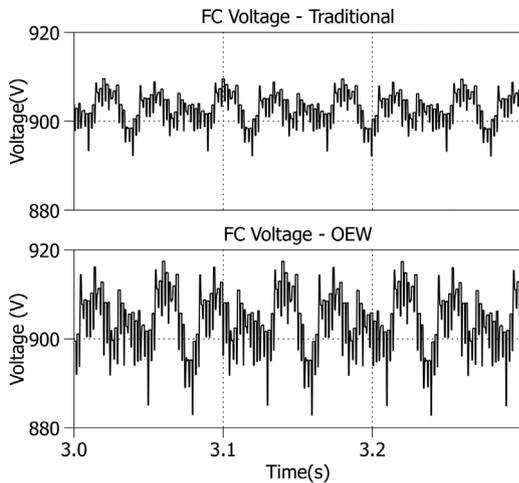


Fig. 17. Flying capacitor voltage ripple comparison between the traditional and OEW systems.

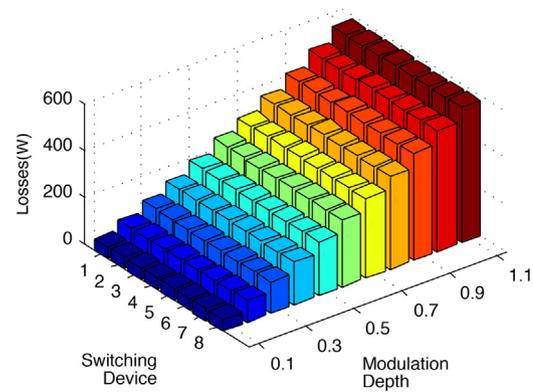


Fig. 20. Simulated losses per IGBT of the phase *a* of the five-level OEW system.

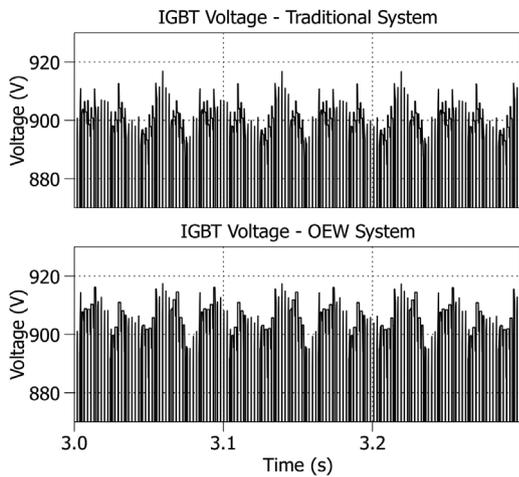


Fig. 18. S_{a2} IGBT blocking voltage on both traditional and OEW systems.

period resulting in an average switching power loss.

For this study, the *CM600HA-34S* device, from *Mitsubishi Electric*, was selected. Results are presented in Fig. 20, which brings the resulting power dissipation per device (the sum of conduction and switching losses for transistor and diode). One can observe that the losses are equally distributed between the devices for all modulation depth range: a very interesting feature for a practical converter. It allows using the same modules for all the switches, which is logistically desirable and avoids overrating components.

A similar calculation was also carried out for the equivalent FC

converter, using the same device model data. It revealed that, for the entire modulation range, there is a difference under 0.002% on the total semiconductor losses between the traditional and OEW systems i.e., the losses dissipated by both structures are practically equal.

5. Experimental results

A three-level OEW converter system was tested with the purpose of verifying that the CSVPWM with state machine decoder could be successfully used in an OEW system, as discussed in the previous sections. Its power circuit is depicted in Fig. 21, where it can be seen that such system does not employ flying capacitors: Eq. (12) results in zero capacitance. DC-links are fed by isolated DC power supplies, and the converters are connected to an RL load. The modulation strategy was programmed in PLECS® RT Box, and system parameters are presented in Table 2.

Fig. 22 shows the waveforms of the phase voltage and current, measured under rated conditions. One can observe the nine levels present in the phase voltage ($v_{aa'}$) for this system: $v_{dc}[0, \pm 1/6, \pm 2/6, \pm 3/6, \pm 4/6]$. With a commutation frequency of 450Hz, the resulting current presents a 1800Hz ripple, evidenced in its harmonic spectrum shown in Fig. 23. This is in accordance with the previously stated effect provided by the modulation strategy: the voltage output is switched at $(n - 1)$ times the devices commutating frequency and the first switching harmonic is highly attenuated.

A good measure of a system's performance with respect to the harmonic distortion is the current total demand distortion (TDDi), as defined by [36]. It relates the harmonic content of the current with its fundamental nominal value. Fig. 24 shows the TDDi of the output current according to the modulation depth value, with constant fundamental frequency (50 Hz). The continuous curve was obtained from a simulation using the same parameters as the experimental setup, while the dots were obtained directly from the experimental measurements.

One can observe that the experimental results corresponded to the

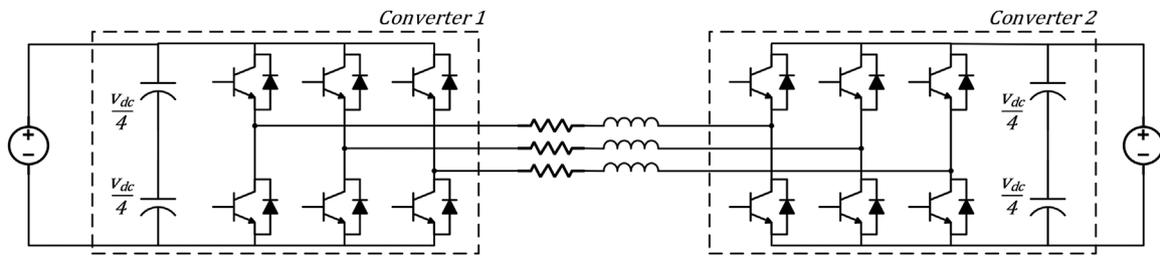


Fig. 21. Power circuit of the dual two-level experimental setup.

Table 2
Experimental setup parameters.

Parameter	Value
Total DC-link voltage (v_{dc})	200 V
Load RMS current	10 A
Load RMS phase voltage	72 V
Load frequency	50 Hz
Load power	2.17 kVA
Load power factor	0.95
Switching frequency	450 Hz

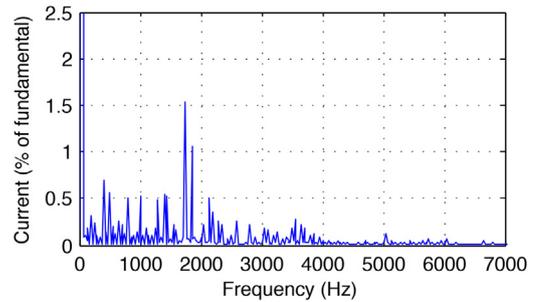


Fig. 23. Harmonic spectrum of the current on the three-level system, under rated condition.

theoretical, and a current with TDDi under 3% is obtained even for such a small switching frequency as 450 Hz.

6. Conclusion

In this paper, a generalized OEW n -level converter using the multicell flying capacitor structure was presented. A mathematical comparison with the traditional Δ/Y structure showed that they can

produce identical voltage outputs with the same command signals. This correlation allowed the use of the CSVPWM with state machine decoder, an optimized modulation technique originally developed for traditional FC converters, in this OEW structure.

Simulation results from a five-level structure demonstrated that the

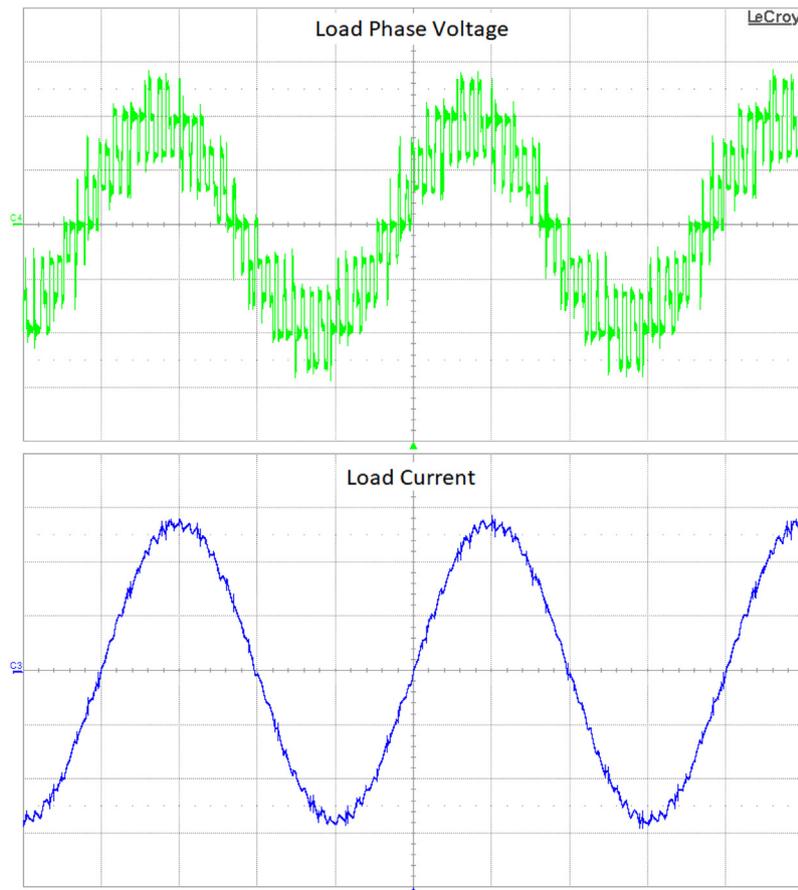


Fig. 22. Above: phase voltage (50 V/div). Below: load current (5A/div). Measured on the three-level system, under rated condition. Time base: 5 ms/div.

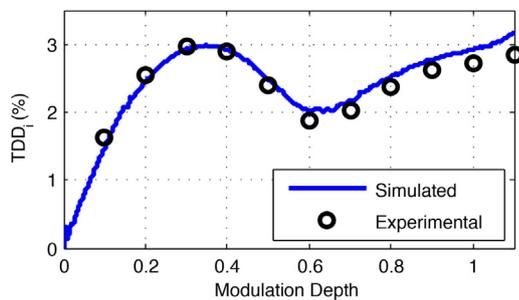


Fig. 24. Total demand distortion of the current on the three-level system: simulated and experimental data.

proposed topology provides an output with great harmonic performance, while keeping the losses evenly distributed among the switching devices. Experimental results from a three-level system showed the feasibility of a practical implementation of this system, while corroborating the simulated results of current harmonic distortion.

Compared to a traditional FC converter with the same number of levels, the presented OEW system employs the same number of switching devices, with equal blocking voltages and dissipated losses. Its main drawback lies in the need for isolated DC-links in order to avoid the circulation of common-mode currents, thus complicating the realization of a *transformerless* drive. On the other hand, it has been shown that the OEW configuration demands considerably less energy storage from flying capacitors, leading to a potential reduction in volume and cost. In this context, the structure presented in this paper arises as a valuable alternative for designers of high power drive systems.

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