

Impact of the Frequency Dependence of the Parasitic Admittance on the Diffusion Noise of a Diode Junction at Low Bias

J. Graffeuil, L. Escotte and J.G. Tartarin

Abstract— In this paper, we report for the first time that the well-established diffusion noise can be apparently increased in large proportions, and that such a situation can be very common at some specific frequencies in p-n junction structures operating at a very low direct bias current. Noise theories and associated measurement techniques are a major issue for emerging semiconductor technologies, the development of accurate CAD models and the designing of low noise circuits and systems. The conventional shot noise model usually satisfactorily describes the p-n junction noise in solid-state devices, such as diodes and transistors. It has proven to be very efficient for many different conventional and advanced semiconductor technologies. However, alterations may sometimes be needed as previous works indicate scenarios where this so-called shot noise exhibits deviations from the theory, which translates into some noise *suppression*. In this paper we report on alterations that look like low frequency diffusion noise *enhancement* (unexpected noise increase). It occurs at low current levels, for many generic commercially available diodes and the p-n junctions in transistors. Therefore, we proposed appropriate electrical noise model that satisfies both the low frequency noise experimental data and the electrical behavior of the devices observed from impedance spectroscopy. We also evaluated this model as the ambient temperature is varied. Finally, it is discussed how this model can be connected to the conventional van der Ziel shot noise model and a better insight on the possible origin of such diffusion noise enhancement is provided.

Index Terms—Low Frequency Noise, shot noise, p-n junction, normalized diffusion noise factor, impedance spectroscopy, activation energy, CCD sensors, dark current.

I. INTRODUCTION

IN almost every electrical system, the actual signal and the noise must be considered together, since noise sets the limit of detection of an electrical signal. Noise theories have been largely developed and substantiated by the association of mathematical formalisms and electrical noise measurements since the early 20th century. These theories are widely accepted, since no inconsistencies are exposed by mathematical studies or by experimental investigations. Among the largely used and proven theories on noise, the contribution given by Walter Schottky [1] one century ago is still hugely applicable to electronic devices such as diodes and transistors. In his theory, formulated in 1918, concerning the noise in electronic devices,

W. Schottky stated that in ideal vacuum tubes, that is an equivalent device where spurious noise sources had been eliminated, and more precisely in the absence of 1/f flicker noise contributors, two types of diffusion noise contributors still remain [1]. The first diffusion noise contributor is known as the Johnson-Nyquist or thermal noise, which originates from the thermal motion of the electrons and occurs in any resistive material featuring a resistance R . The second diffusion noise phenomenon, which is usually referred to as shot noise, can also be seen as resulting from the discrete nature of electric charges and hence the flow of current.

Van der Ziel has specifically addressed this noise in solid-state diodes. He has established [2]-[4], using both a corpuscular approach and the more fundamental collective theory, that the shot noise expression at higher frequencies and moderate injection levels involves the frequency dependent conductance of the junction G_j , and G_0 its static (low frequency) value (Nyquist expression contribution at near zero DC current) and becomes :

$$S_i = 4k_B T G_j - 2qI = 2q(I + 2I_s) + 4k_B T(G_j - G_0) \quad (1)$$

where T is the ambient temperature (in Kelvin) and k_B the Boltzmann's constant.

In most situations, $G_j = G_0$ in a large frequency range. Hence $S_i = 2q(I + 2I_s)$ and the diode normalized noise can be expressed as $\gamma = S_i / (2q(I + 2I_s))$. Therefore, as long as the diode noise is only shot noise, γ should be one. However, some deviations can possibly occur either as a consequence of a non-ideal diode exponential characteristic [5,6] or as the consequence of the presence of recombination centers in the diode space charge region (SCR) firstly investigated in [7]. It usually results in a γ below 1 ($0.5 \leq \gamma < 1$, noise suppression).

We report, for the first time, low current, low frequency noise spectra featuring a frequency dependent $\gamma > 1$ that can be regarded as an apparent diffusion noise enhancement or, equivalently, as a noise performance degradation. Various p-n junctions have been investigated over a large number of bipolar transistor models. These frequency and biasing conditions fit applications such as in some telecommunication applications (low phase noise oscillators operating at low DC energy), or optical detection systems where active pixel sensors in imaging

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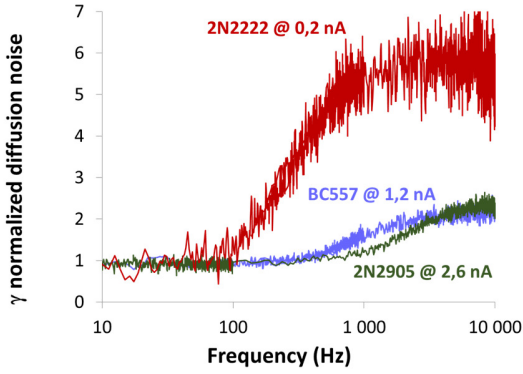


Fig. 1: Evidence of the diffusion noise floor increase at low frequencies (deviation of the normalized representation γ from unity), for three various silicon technologies. *Note: emitter-base diodes (collector open) are investigated.*

systems can operate at very low currents due to device scaling. The application of the $S_i \approx 2q(I+2I_s)$ formulation could seriously underestimate the dark leakage noise current of CCD or PPD devices and hence the minimum detectable signal.

Following this first introductory paragraph, the second section of this paper provides the experimental evidence of this frequency dependent variation of the low frequency diffusion noise occurring at very low biasing conditions. In the third section, we propose an electrical model that assesses the noise frequency dependent behavior reported in the first section. We compared our model with the theory developed by van der Ziel [3]. Interpretations of the observed data are discussed in the fourth section.

II. EXPERIMENTAL EVIDENCE OF NOISE DEGRADATION

Low frequency noise measurements require a particularly accurate and careful control of the experimental setup; the selection of the measurement apparatus, shielding conditions, cables, biasing circuits and signal (noise) amplifiers are of prime importance since they limit the measurement bandwidth and the noise floor for investigations. Choosing either a voltage or a current-voltage (transimpedance) amplifier is very critical since it depends on the device under test (DUT) impedance, that is, in this work, on the junction I value. Additionally, correction parameters, obtained from a very careful preliminary characterization of the noise parameters of the amplifier, are used to extract the low frequency noise characteristics of the DUT. Moreover, the amplifier input impedance can have an impact on the overall gain of the measurement set-up and must also be de-embedded. It must further be noticed that the frequency dispersion of the DUT impedance is also considered for the previous correction.

Various commercial devices (emitter-base or collector-base of npn or pnp junction transistors as well as high frequency bipolar devices, silicon diodes or Schottky diodes) have been measured from 1 Hz to 1 MHz over a large biasing range. At medium and elevated current ($I > 1 \mu\text{A}$) up to 100 kHz, no deviation from the $S_i \approx 2q(I+2I_s)$ spectral density is observed. However, the noise degradation phenomenon under investigation is observed at low current ($I < 1 \mu\text{A}$) for most of

the measured p-n silicon junctions (diodes and transistors). Figure 1 depicts the observed variation of the normalized γ expression of the noise floor (not referred to as Fano factor in this work, because of a different origin of the observed phenomenon in spite of the same analytical representation), for three different p-n junctions. The γ factor deviates from unity at a specific corner frequency f_{low} , and then reaches a plateau P_i ; either the corner frequency (or also considering the half frequency f_{half} as defined later) and the plateau magnitude depend on the biasing current I . In this work, a focused analysis on the 2N2222 silicon bipolar device is proposed.

Figure 2 shows the normalized γ factor variations versus frequency f ($10 \text{ Hz} < f < 1 \text{ MHz}$), with I as a parameter ($0.18 \text{ nA} < I < 1 \mu\text{A}$), for the emitter-base junction (open collector) of a very common 2N2222 npn bipolar silicon transistor. These data have been obtained from spectral FFT measurements achieved through a very low noise, fully shielded, battery powered current-voltage (transimpedance) amplifier. To assess the DUT noise de-embedding process, passive parallel R_{test} - C_{test} networks were used as reference devices. For this purpose, R_{test} and C_{test} feature similar magnitude values to those of the junction dynamic resistor and parallel capacitance (including test-set capacitance) respectively. Then, it can be verified in Fig. 2 that the normalized measured current noise $S_i/(4kT/R_{test})$ of the R_{test} - C_{test} networks is close to unity over the entire frequency range as expected (within the accuracy of the workbench). Test 1 (grey plot) uses a 100 k Ω resistor in parallel with 7 pF capacitor, whereas Test 2 (red plot) uses a 3.3 M Ω resistor in parallel with 52 pF capacitor.

Moreover, it must be pointed out that a current-voltage amplifier features a low pass behavior with a greatly reduced maximum operating frequency as it is operated under higher gain and lower noise conditions (gain-bandwidth relationship due to feedback). Since the very low I measurements under consideration in this paper correspond to very low noise levels, therefore high gain and low noise conditions are required for

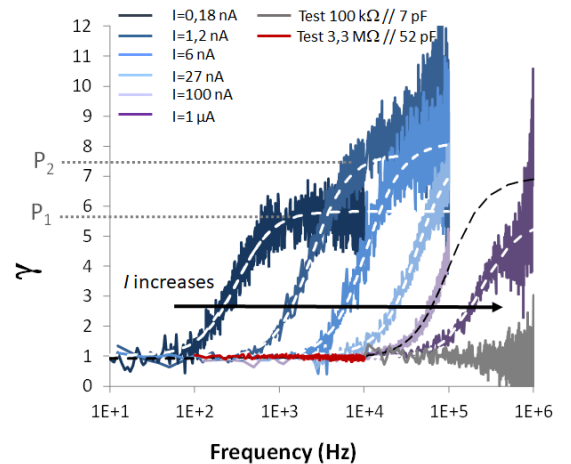


Fig. 2. Normalized noise spectra γ factor variations versus frequency) of the 2N2222 bipolar transistor emitter-base junction operating at very low direct currents ($I = 0.18 \text{ nA}$ to 1000 nA). The normalized measured noise spectra of two R-C parallel networks are presented in order to assess the noise measurements accuracy (red and grey plots featuring $\gamma=1$). The meaning of the dashed lines is described in the modelling section.

the amplifier. Consequently, the noise measurements above a given frequency limit become intractable. For our amplifier, this limit is between 1 kHz (I current in the nA range) and 1 MHz (I current in the μ A range). Hence, even if various setups involving a single voltage preamplifier or two current preamplifiers for cross-correlation measurements [8] have been successfully compared with the single current-voltage preamplifier, all the presented data in this work are obtained with a single current-voltage preamplifier as in [9]. This allows to investigate the DUT within a wider biasing range of current I .

The measured noise data displayed in Figure 2 show that for any low bias current, the normalized noise factor γ is always close to one in the lowest frequency range (<100 kHz), as expected. However, and very surprisingly, γ begins to increase above a given corner frequency f_{low} that rises as I increases. Above a second corner frequency f_{high} , γ remains constant with P_i values higher than 1 and below 10 for the tested device in Fig. 2 (P_i values greater than 10 have been measured for some other npn tested devices). A noise plateau of amplitude P_i is therefore established. However, due to statements in the previous section relative to measurement frequency limitations and increased measurement uncertainties in the higher frequency range or similarly for the highest I , we are unable to precisely determine whether this plateau will end above a certain frequency and if γ will return to unity, i.e. $S_i \approx 2q(I+2I_s)$.

We have observed a similar behavior in most (but not all) of about a dozen different types of commercial npn and pnp BJT's or junction p-n diodes, even when the observed plateau was usually lower than those of the many 2N2222 measured devices as shown in Fig. 1.

Finally, Fig. 3 shows the variation of P_i versus I , and Fig. 4 the variation of the specific frequency $f_{half} = (f_{high}-f_{low})/2$, defined as the frequency where $\gamma = (P_i + 1)/2$, as obtained from Fig. 2. From Fig. 3, P_i features an inverse U-shape with $\log(I)$, even if the model is not fully reliable for the higher DC current range as previously stated. The variation of f_{half} with I features a linear regression (or exponential with V_{be}). We observed similar behaviors when considering the base-collector junction, instead of the base-emitter junction as proposed in Fig. 1 and Fig. 2.

At this point, we would like to comment further on the possible reasons why this phenomenon has never been reported before. Without doubt, very stringent experimental conditions are required in order to be able to observe this phenomenon. As previously stated, measurements are not easily tractable for any I larger than about 0.1 μ A (as f_{low} is usually higher than 100 kHz and a measurement bandwidth well above 1 MHz is necessary). Nevertheless, in order to observe some noise floor increase at "low" current (less than 1 μ A), measurements below 100 kHz are enough. This low current range is of interest for photodetectors (as dark current in silicon p-n junctions are typically between 0.001-100 nA [10]). A γ featuring a plateau P_i higher than unity has never been previously reported; it represents a major issue for devices modelling, since their noise floor is usually appreciated considering a γ factor of one. According to our findings, the lowering of bias level associated with the size reduction in new silicon technologies should

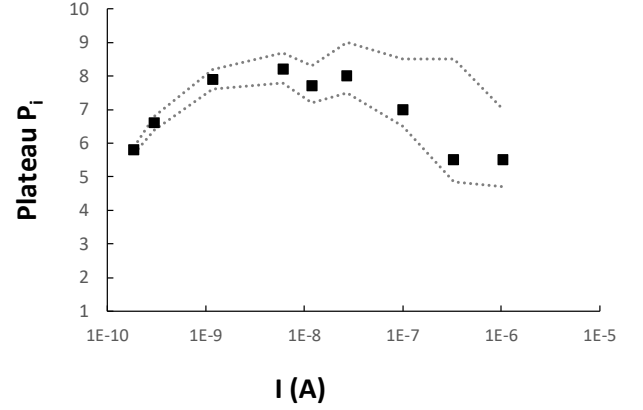


Fig. 3. P_i variations versus I obtained from data of Fig. 2. Dashed lines define the uncertainty of extraction for the plateau 'best value extracted' symbol ■. Y-axis starts at 1 to appreciate the magnitude of deviation from the theory.

render obsolete the conventional diffusion noise approach in these devices.

III. DIODE ELECTRICAL AND NOISE MODELLING

The electrical variation of the frequency f_{half} versus I or V_{be} , shown in Fig. 4, is evaluated next by means of the junction impedance spectroscopy and noise electrical modelling based on the electrical equivalent network depicted in Fig. 5.

In this network C_d and R_d stand for the conventional junction small signal capacitance (transition + diffusion) and dynamic resistance ($R_d = 1/G_0 = nU_t/[I+I_s]$ where n is the junction non-ideality coefficient and U_t the thermal potential). i_d is the conventional junction low frequency equivalent diffusion noise current generator featuring the spectral density $S_{id} = 2q(I+2I_s)$.

In order to account for the noise floor increase and for the plateau, a simple additional series $R_{add}-C_{add}$ network has been associated in parallel with the junction equivalent network in Fig. 4. Consequently, we must also consider the thermal noise generator e_{add} of R_{add} that features a voltage spectral density $Se_{add} = 4k_B T R_{add}$. This generator is responsible for the observed noise (γ) increase of Fig. 1 and Fig. 2 above the frequency f_{low} that depends on the product $R_{add}C_{add}$. The dashed lines of Fig. 2 represent the calculated γ (ratio $S_{is}/(2q(I+2I_s))$) from Eq. 2 where S_{is} is the measured short-circuited current noise spectral density of the Fig. 5 network. S_{is} is given by Eq. 2, as:

$$S_{is} = S_{id} + \frac{(C_{add}\omega)^2 \cdot Se_{add}}{(1+(R_{add}C_{add}\omega)^2)} \quad (2)$$

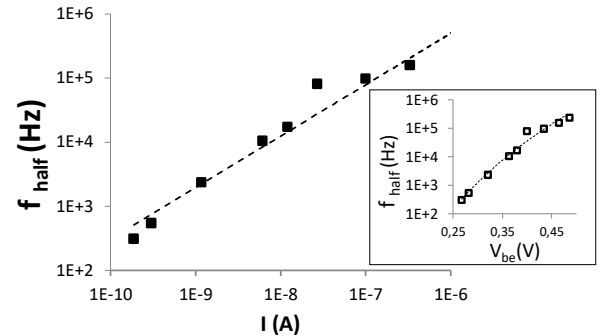


Fig. 4. (Log) f_{half} variations versus (Log) I (or versus V_{be} in the inset) obtained from data extracted from Fig. 2.

The model provides an excellent agreement with the measured data of Fig. 2 for every direct current I , provided that the R_{add} and C_{add} values are correctly taken for each I value according to Eq. 2.

In this equation, the second term accounts for the excess noise under consideration in this study, with a plateau value of $S_{i_s} = S_{i_d} + 4kT/R_{add}$ for higher frequencies (or its normalized form $P_i = 1 + U_i/(I.R_{add})$ in Fig. 2). Thus, the values of R_{add} and C_{add} that provide the best fit to the measured noise dispersion versus I are reported in Figure 6 and 7 respectively.

Additionally, we have performed junction admittance spectroscopy measurements $Y(f)$ at a similar range of current values I as those used for noise measurements, and we have de-embedded the R_{add} and C_{add} values from $Y(f)$ according to the network of Fig. 5. The R_{add} and C_{add} values, obtained either from noise or admittance spectroscopy measurements, are compared in Fig. 6 and Fig. 7. A good agreement is observed. It substantiates our finding that the observed junction noise increase is the result of a series R_{add} - C_{add} network that, under certain circumstances, connects in parallel with the conventional junction equivalent network. Hence the R_{add} diffusion noise impacts on the overall junction noise at a given frequency f , as long as f is higher than f_{low} that scales with $1/(2\pi R_{add} C_{add})$. Hence the physical origins of f_{low} (and f_{high}) are the same than the ones of R_{add} and C_{add} and will be addressed in the last section.

The computed values of f_{half} obtained from R_{add} - C_{add} are consistent with the extracted values from Fig. 3 as expected (i.e. power law of f_{half} versus the DC current I).

Moreover in Eq.1 the $G_j(f)$ frequency variation is needed. It can efficiently be obtained from junction admittance spectroscopy measurements. Substituting $G_j(f)$ from its measured DC value in Eq.1, provides a good agreement between calculated and measured γ as illustrated with the dotted plots proposed in Fig. 2, as well as with the LFN model proposed in Fig. 5. However, in previous van der Ziel's studies, no such plateau featuring $\gamma \gg 1$ is mentioned; this is discussed in the next section.

IV. DISCUSSION

The Fig. 5 electrical and noise schematic of a low frequency, low current operated p-n junction, has been validated by two different characterization techniques (noise spectroscopy from Fig. 2 and impedance spectroscopy). This simple electrical and noise model is efficient for an accurate representation of noise, and then can be used to analyze the phenomenon responsible for the observed γ enhancement.

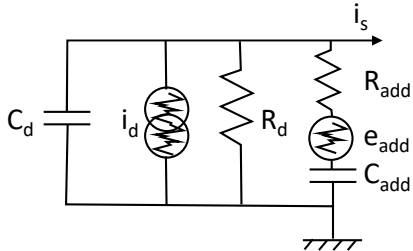


Fig. 5. Electrical representation of the diode (parallel R_d - C_d) with its shot noise current source (i_d) and with the low frequency noise increase (e_{add}) associated to the electrical cell (serial association R_{add} - C_{add}).

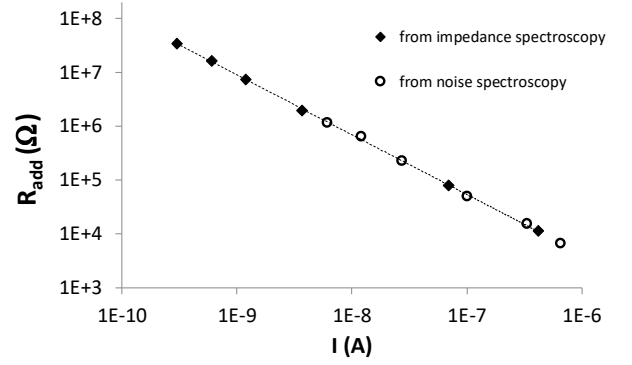


Fig. 6. Comparison of R_{add} variations either derived from noise (data from Fig. 2) or from impedance spectroscopy data.

We therefore focus on the discussion of Fig. 5 model. Three hypotheses, possibly correlated, may be proposed in order to substantiate this model:

- the first scenario considers R_{add} - C_{add} as a trapping-detrapping process (i.e. featuring a time constant).
- the second one is based on the minority carriers flowing in the long p-n junction (i.e. the lateral section as depicted in Fig. 9. a).
- the third one relates these electrical elements to technological (physical) layers or zones of the junction under study.

In the first scenario, a possible answer originates from the findings of J. Vedde and P. Viscor [11][12]. They have established that the presence of deep level impurities within the space charge region affects the junction impedance in the same way as a parallel connected RC series circuit (as illustrated in Fig. 5). This is contradictory to the fact that the RC network of Fig. 5 involves a noisy resistance, and cannot actually be associated with a time constant. Moreover, in order to characterize the possible deep trap that could be involved in the 2N2222 device presently investigated, we have achieved some admittance spectroscopy measurements versus temperature. We have therefore obtained the Arrhenius plot shown in Fig. 8. An activation energy of about 0.9 eV is extracted in our study case, but featuring a large capture cross-section of $\sigma_5 = 9.10^{-9}$ cm². This capture cross-section is not consistent with the values from the literature, associated to impurities and defects in

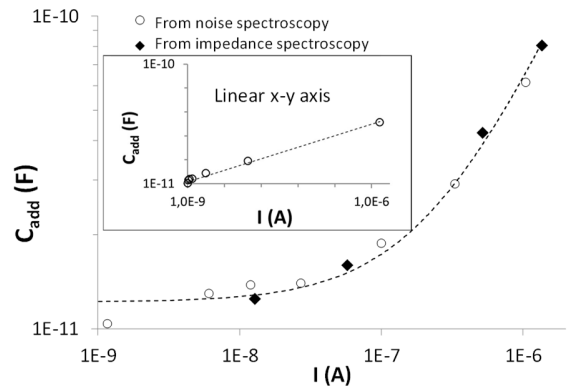


Fig. 7. Comparison of C_{add} variation versus I either derived from noise (data from Fig. 2) or from impedance spectroscopy data. Inset validates the linear dependence of C_{add} versus the direct current I .

silicon technologies (considering both electron and hole type of carrier) [13]. These points are contradictory with the present findings if considering a time constant, instead of a physical RC cell, associated to the defect.

In the second approach, the equations developed by Overstraeten et al. in [14] can be used to compute the electrons carrier lifetime τ (the 2N2222 emitter-base junction is a n+p junction and, hence, the minority carriers in the base region are electrons). Hence $G_j(f)$ can be calculated and, in turn $S_i(f)$ and γ can be derived from Eq. 1. However, we have to speculate about many unknown technological data and the agreement between experimental and theoretical data does not look sound enough.

The third hypothesis involves an unexpected electrical behavior occurring under these specific low biasing and low frequency conditions. First, it must be noticed the linear dependence of C_{add} with the DC current I (inset in Fig. 7), as can be found for diffusion capacitance: then C_{add} could be written in a first approximation as $q\tau J/(2kT)$, where J is the current density and τ the minority carrier lifetime. Furthermore, the resistance R_{add} can be associated to a resistive layer acting in parallel with the junction diode, and can be noisy as stated by our model in Fig. 5. The variation of R_{add} with the current I also features a linear representation with I^{-1} , as for the junction resistance. Nevertheless, an ideality factor of $n=1.1$ is extracted for the junction diode resistance R_d , whereas an ideality factor of $n=0.36$ is extracted for the resistance R_{add} under consideration. Ideality factors usually range between 1 (volume recombination limited by minority carrier) and 2 (recombination in the space charge region), as in the case of R_d . The unexpected value of 0.36 lower than unity is out of the usual bounds and further work is needed in order to determine the physical origin of this phenomenon. At least, the abnormally high value of the cross-section $\sigma_s = 9.10^{-9} \text{ cm}^2$ (associated to the activation energy of $E_a = 0.9 \text{ eV}$) can be interpreted as the action of a new electrical path translated into $R_{add}-C_{add}$, and located within the base zone (towards emitter or collector according to the diode under test). Fig. 9 represents the schematic cross-sections of a BJT silicon device a), and of an HBT GaAs device b). Different silicon schematics can be found from the literature, but all of them feature more or less the same n, n+ and p zones

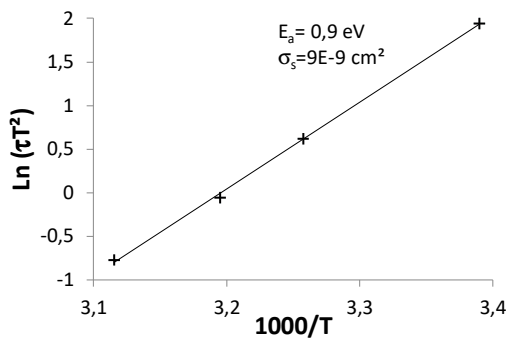


Fig. 8. τT^2 evolution versus $1/T$ for the 2N2222 bipolar transistor emitter-base junction operating at a constant $V_{be}=321\text{mV}$ ($I_{be}=1.2 \text{ nA}$ at 300K) for temperature ranging from 295 K to 320 K. τ is the calculated equivalent “time constant” associated to $R_{add}-C_{add}$ cell extracted at each temperature at constant V_{be} biasing.

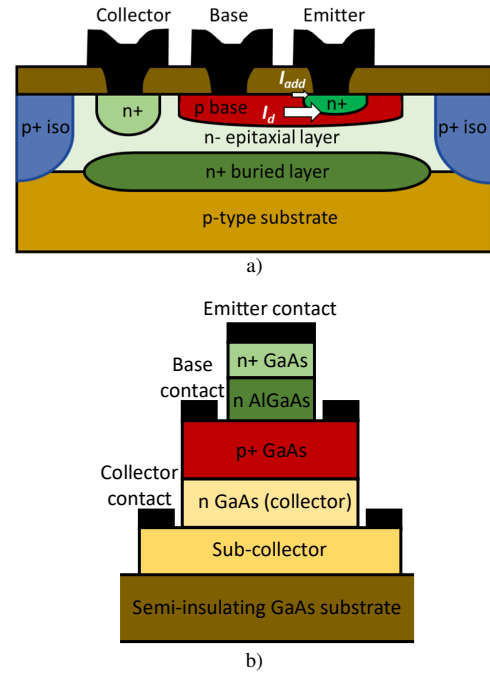


Fig. 9. Schematic cross section of an n-p-n silicon junction bipolar transistor (BJT picture a), and GaAs heterojunction bipolar transistor (HBT – picture b) structures. White arrows in a) stand for the current distribution between the main diode current I_d and the additive contribution I_{add} sensed at low bias and low frequency (base-emitter diode mode configuration).

as depicted in Fig. 9 a). The partition of the electrical field between the base and the emitter in Fig. 9 a) is not uniform and depends on the base current for a transistor mode. If the BJT depicted in Fig. 9 a) is biased in diode configuration (emitter-base for example), then the vertical p-n junction is not located in the same region at low current I than at high current (due to the non-uniformity in the electrical field distribution). The interface lateral area (upper zone of the p base) under consideration at low current can be the location of the phenomenon occurring when $R_{add}-C_{add}$ balances the effect of the main junction diode R_d-C_d as usually considered. Thus, the cross-section found from Fig. 8 data can be interpreted as the total perimeter zone where the interface plays a contribution trough at a given depth (and represented as $R_{add}-C_{add}$). According to the result from Fig. 8, and assuming a perimeter of 1 mm between base and emitter (values of 880 μm or 975 μm emitter perimeters can be found from various 2N2222 layouts). Then the averaged depth that could be related to the electrical model $R_{add}-C_{add}$ would be in the range of 0.1 \AA (knowing that the atomic ray of a silicon atom is 1.1 \AA). Lastly, considering that we have not observed such noise deviation from $2qI$ equation for diodes in any HBT devices under test, the difference of the vertical structure between BJT and HBT, and the associated process steps may probably explain why the reported noise increase occurs only in silicon diodes. Although the different collector, base and emitter zones are achieved by planar technologies for silicon BJT, stacked layers are used in HBT devices. Fig.9 b) depicts the vertical structure of such HBT technologies (same principle used for SiGe process). The vertical stacking avoids any lateral path between the base and emitter (or collector), and then no additive $R_{add}-C_{add}$ cell is

involved in the electrical and low frequency noise schematic of HBT.

To end with the previous hypothesis, some papers have pointed out the effect of mesoscopic fluctuations in the hopping conductivity for thin film silicon layers (with localized states impacting the conductivity by forming conductive chains, even at 300K [15]). A thermal and field dependence of the hopping conductivity is exhibited. The conductivity dependence of these thin films with temperature obeys an activation law, not related to the simple Mott formula. Activation energy at 300 K ambient temperature is extracted at 0.32 eV for those heavily doped p-type Si layers in [15]. On a comparable basis, we assume that a (lateral) thin film between the electrodes can operate in parallel with the intrinsic main diode for our study case; this phenomenon may occur at the vicinity of the upper p interfacial zone of the base, as the same low frequency noise increase is noticed both for base-emitter or base-collector diodes. Moreover, the statistical probability of scattering in the resistance (conductance) due to individual hops is higher for large area/section devices (due to the higher probability of formation of such hopping chains). Then these related mesoscopic phenomena could match with our hypothesis concerning the partition of an interface electrical path featuring an equivalent average depth of 0.1 Å if we consider a distribution over the total 1 mm emitter perimeter. Further investigations are needed in order to harmonize the hypothesis made in this paper (collective approach of the shot noise) and other related works (using equations at a corpuscular scale).

V. CONCLUSIONS

In this paper, a low-frequency noise model is proposed for the p-n junction noise floor at low injection level. This noise floor (i.e the observed junction noise as long as the junction is rid of any excess noise) is a diffusion noise classically given by the Gupta's theorem and, for direct current bias, it very frequently reduces to the well-known shot noise formula $S_i = 2qI$. Essentially only one exception is already well established and largely published, because of the charge carrier generation in the space charge region, and can result in up to 50 % noise suppression.

In this paper, we report, for the first time, low frequency diode noise spectra featuring a monotonous increase with frequency above the expected $2qI$ shot noise and getting to a plateau that can be an order of magnitude larger. Both the magnitude of this plateau and its associated corner frequency depend on the current flowing through the junction. Due to hardware limitations, that preclude accurate measurements above 1 MHz, this degradation of the noise floor, present in most p-n junctions, can only be observed in a very limited range of frequencies below 1 MHz and of low direct currents below 1 μ A.

We have selected two possible models for this noise increase phenomenon.

The first one uses the van der Ziel's general expression (Eq. 1) where the impact on noise of the junction admittance variations $G_j(f)$ versus frequency are theoretically anticipated but not experimentally verified. We have therefore substituted

the $G_j(f)$ measured from junction admittance spectroscopy in Eq. 1 and found that it correctly fits the measured data. It therefore provides an unexpected and new validation of Eq. 1.

The second noise model involves the thermal noise of an additional R_{add} - C_{add} series network to the conventional junction electrical network (Eq. 2). We have found that such a network is consistent with admittance spectroscopy measurements as well as with noise measurements, for a large range of low current and for various temperatures. Such a model can be easily implemented in any CAD software. Further investigations are needed in order to clarify the origin of this resistive noise contributor. In particular, it must be investigated what will happen with this noise increase beyond 100 kHz or 1 MHz for currents respectively above 10 nA or 1 μ A.

We believe that this additional noise source in the conventional diode model can seriously affect the noise performance of circuits involving very low bias operating device junctions, such as in some telecommunication applications (low phase noise oscillators), or optical detection. It could possibly heavily impact the dark leakage noise current of CCD detectors and hence the minimum detectable signal.

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