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Version of Record: https://www.sciencedirect.com/science/article/pii/S0026271419304846
Manuscript_99c084b836158ed36b89d350e54d627e

S-Band Pulsed-RF Operating Life test on AlGaN/GaN HEMT devices for Radar application

N. Moultif[a,*], O. Latry[a,*], M. Ndiaye[b], T. Neveu[a], E. Joubert[a], C. Moreau[c], J-F. Goupy[d]

[a] *University of Rouen Normandy, GPM Laboratory- UMR-CNRS 6634, 76800 Saint tienne de Rouvray, France*
[b] *CEVAA, Technopole du Madrillet, 76800 Saint tienne de Rouvray, France*
[c] *DGA-MI, BP7 35998 Rennes CEDEX 9, France*
[d] *Thales LAS France, ZI du Mont Jarret, 76520 Ymare, France*

Abstract

Reliability studies are fundamental to optimize the use of new emerging technologies such as AlGaN/GaN HEMTs. This paper reports a reliability study on two power amplifiers using AlGaN/GaN HEMT in real operating conditions for radar applications. Three pulsed-RF long ageing tests (8000h/11000h total) are performed under different conditions of (V_{ds}), Temperature, gain compression and Duty cycle. A following of various degradation indicators during the ageing tests is presented (P_{out}, I_{ds}, I_{gs}, $R_{ds(on)}$, G_m and V_{th}). This study will contribute to establish a new reliability prediction model of GaN devices and update the FIDES guide.

Key words: Ageing, AlGaN/GaN HEMT, Pulsed-RF Operating Life test, Reliability, Traps.

1. Introduction

Thanks to the interesting GaN properties (Wide band gap, high saturation electron velocity and high mobility) [1], the AlGaN/GaN high electron mobility transistors (HEMTs) technology has shown excellent performances in high frequency and high power switching applications. These devices have high breakdown voltage and high electron mobility that makes them suitable for power converters and RF amplifiers designs [2, 3]. However, the long-term reliability of these devices remains a challenge that must be addressed to provide a rapid industrialization of this technology [4, 5]. In order to evaluate the reliability and the robustness of AlGaN/GaN HEMT devices, a variety of studies perform DC and step stress test [6, 7, 8]. These types of test provide a fast feed-back on the development and the processing quality. Other normalized test such as MIL STD or JEDEC are usually applied for the qualification of the technology for foundries [9, 10]. Considering the standard conditions used (duration, temperature, etc) in the public qualification reports, the purpose of the tests is not for ageing assessment.

Yet, the best way to increase the lifetime of AlGaN/GaN HEMTs, is to understand the failure mechanisms which could occur in these devices when used in their operating system. It is fundamental to perform long-term reliability tests with a stress level close to real mission profiles. These tests are able not only to improve the intrinsic reliability and the operating lifetime of AlGaN/GaN HEMTs devices, but also to construct new reliability prediction models. The qualification reports and the reliability data collected from different suppliers indicate that the majority of the RF tests conducted on this technology are in CW (Continuous Wave) mode and are carried on only for a few thousand hours.

In this paper, long duration ageing tests (11000 h) are performed on AlGaN/GaN HEMTs for radar applications on RF pulsed mode with different conditions on: gain compression and Duty cycle (DC) in order to construct a new reliability prediction model and update the FIDES guide [11]. The stress parameters (Duty Cycle and the gain compression) were chosen to reflect the different mission profiles of radar applications. This paper first presents the results of these tests (8000 h on 11000 h total), and different ageing indicators are shown (drain current, gate current, output power, ect.). This work presents at first the devices under test and the power amplifier design. Then the test bench and the tests protocol are described. The main results of the three ageing tests are presented and discussed. Finally, the conclusion summuries impacts of these tests on the reliablility of AlGaN/GaN components tested.

2. Experimental setup

2.1. Power amplifier design

The purpose of this paper deals with the ageing of two commercial AlGaN/GaN HEMTs on SiC substrate from two different foundries: Supplier "A"(with the voltage and current rating of 30 V and 5 A respectively) and Supplier "B" (with the voltage and current rating of 50 V and 1.5 A respectively). Both transistors are in a ceramic package and designed for S-Band in this case. The device "A" has a gate length of $0,25\mu m$ with T shape with a total development of 5,5mm. A field plate with a source termination is used in this transistor. The device "B" has a $0,25\mu m$ gate length, $7,6\mu m$ source/drain spacing and $1,13\mu m$

*Corresponding authors
Email addresses: niemat.moultif@gmail.com (N. Moultif), olivier.latry@univ-rouen.fr (O. Latry)

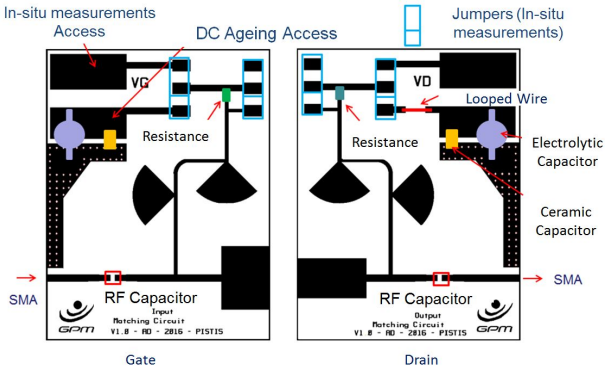


Figure 1: Circuit diagram for the designed RF amplifier

source/gate spacing. This transistor possesses 20 gate fingers with an interdigitated structure (total gate development of 5 mm).

A power amplifier has been designed for each transistor. The same amplifier architecture was used for the two transistors to limit uncertainties in case of extrinsic failures. Only the dimensions of the RF path necessary for the impedance adaptation differentiate the two types of circuits, as well as the central part because of the different package dimensions of the two transistors. Input and output matching circuits were designed with microstrip impedance transformers. The adaptation circuits were simulated via the ADS software and the MOMENTUM electromagnetic simulation module. A global schematic of the designed amplifier is shown in Figure 1. Circuits are etched on Rogers Duroid RT6010.2 Cu-clad substrate and mounted on brass baseplates. The design of the amplifiers allows in-situ measurements: Jumpers are used for bypassing the decoupling capacitors (Figure 1). The ageing can be stopped at any time and I-V pulsed characterizations and diode measurements can be performed without unplugging the amplifiers and losing the bench RF calibration. In our knowledge, this is an original and efficient way to ensure measurements accuracy regarding consistent with the expected parameters drifts.

2.2. Test bench and protocol description

Three test benches are dedicated to this work. The first bench has independent channels. Each channel is related to a chassis integrating DC and RF boards. The system manages all test independently. The chronogram test, measurements of voltages, currents, RF powers and temperature of the heating elements are carried out and stored for the duration of the test. This bench is able to perform ageing in the 2-6GHz frequency band. The two other benches are based on a central unit that can test several devices simultaneously [12]. It consists of a computer driving control and data-recording peripherals (power supplies and memories). Power modules are driven by this central unit. A signal generator is used to provide RF pulses triggered by the central unit. A power amplifier is needed to ensure sufficient input power level on each device. A power divider, couplers and circulators are employed to measure input and reflected powers. The output of the devices under test is connected to a 40 dB attenuator, itself connected to a power sensor. During the test, different parameters (RF power, current, voltage and temperature) are monitored and recorded in memory. These benches can address ageing both in L-Band ([1; 2] GHz) [13] and S-Band ([2; 4] GHz) [14, 15, 16, 17].

Three ageing campaigns are conducted on the devices under test. The stresses are defined to meet the operational RADAR conditions as it is summarized in the Table 1 with a pulse period in the range of $100\mu s$. The first and the third tests address the Supplier "A" devices, while the second test is carried out on the Supplier "B" devices. All devices are stressed at 3 GHz operating frequency. A burn-in of all devices was carried out before the ageing in order to stabilize the DC and RF devices performance. The input power is adjusted at 32 dBm for the first test, to have a compression around 6 dB and a duty cycle at 80%. To obtain the same duty cycle and a compression around 4 dB, the input power in the second test is adjusted at 30.3 dBm. For the third test, the input power corresponding to a 4.5 dB compression and a duty cycle at 60% is applied separately on each channel. During the test, only RF signal is pulsed, while drain and gate voltages are kept constant. Both devices have been run under their maximum rating drain-source voltage specified by the manufacturer, and at a quiescent current (I_{dq}) corresponding to a class-AB amplification close to $V_{ds(max)}$ for each technology:

- For Supplier "A" devices: V_{DS0}=30V and I_{dq}=6mA.
- For Supplier "B" devices: V_{DS0}=43.5V and I_{dq}=100mA.

The base plate temperature is adjusted at 120°C and 130°C for "A" amplifiers and "B" amplifiers respectively. The reference temperature of the base plate is measured with PT100 placed inside a hole in the board just beneath the transistor. Using pulsed IV measurements at different temperatures and dissipated powers [18], the mean junction temperature is estimated at: 208°C for "A" devices and 210°C for "B" devices and check with to IR thermography. The junction temperature calculated is the maximum temperature in the RF pulse for the whole device. For the three tests, one of the devices is used as a reference and underwent a temperature storage test in order to verify that at the base plate temperature, the board, the electronics of the board, the circuit and the whole measurement branch are stable during time, and to ensure that the observed variations are intrinsic and are not related to an extrinsic failure.

In order to follow the degradation in the devices, many parameters are monitored and analyzed during the aging tests: the input, output and reflected power, in addition to the average voltages and currents on the drain and the gate, and the case temperature. The aging is stopped at logarithmic intervals for interim measurements. These measurements include:

- RF characterization: $P_{OUT} = f(P_{IN})$, $PAE = f(P_{IN})$, $Gain = f(P_{IN})$, $I_G = f(P_{IN})$.
- DC characterization: Pulsed $I_{DS} = f(V_{DS}, V_{GS})$, Schottky characterization (leakage current, ideality factor, barrier height), transconductance (G_m), On-state resistance ($R_{ds(on)}$), Threshold voltage (V_{th}).

Table 1: Ageing conditions of AlGaN/GaN HEMTs

	Foundry	Reference	Test Conditions
Test1	**Supplier "A"**	A01-A02-A03	DC=80%; 6dBc; f=3Ghz V_{DS0}=30V; I_{dq}=6mA T_b = 120°C; T_j = 208°C
		A04_Ref	$T_b = T_j$ = 120°C
Test2	**Supplier "B"**	B01-B02-B03	DC=80%; 4dBc; f=3Ghz V_{DS0}=43.5V; I_{dq}=100mA T_b = 130°C; T_j = 210°C
		B04_Ref	$T_b = T_j$ = 130°C
Test3	**Supplier "A"**	A05-A06-A07-A08	DC=60%; 4.5dBc; f=3Ghz V_{DS0}=30V; I_{dq}=6mA T_b = 120°C; T_j = 208°C
		A09_Ref	$T_b = T_j$ = 120°C

So far, these measurements have been carried out at t0, 48, 96, 144, 500, 1000, 3000, 5000 and 8000 h for Test1 and Test2. For Test3 the interim measurements have been conducted at t0, 700, 3000h and 5000h. The three tests are planned for a total duration of 11000h unless a failure occurs for all the devices tested. In our study, a device is considered in failure if a drop of 1 dB is noticed at the output power or if the drain-source current I_{ds} is lowered by 20% (values usually found in manufacturer's failure criteria).

3. Aging tests results

The first noticeable element from the monitoring of the electrical parameters during the aging in the three tests, is the stability of the drain current (Figure 2) and the output power (Figure 3) of the Test3 devices. Test3 is the least restrictive test (DC=60% and 4.5dB of gain compression), and the least advanced in time. Consequently we are going to focus mainly on the results of the two other tests.

During the 8000h of aging in Test1 that offers the most severe conditions (DC=80% and 6dB of gain compression), the "A" amplifiers show moderate decrease in drain current (drift less than 14 %) (Figure 2) and output power (0.5 dB) (Figure 3). Device "A02" seems to be the most impacted by stress. The monitoring of the gate current during the aging (Figure 4) shows a slight increase of I_g in time. In figure 4-b, we notice a correlation of Ig variations between "B" amplifiers. We ignore the root cause of this correlation. It could be the impact of noise due to the whole bench (even if the room temperature is stable close to 1°C and the bench is calibrated). In fact, the most important is the I_g variation in the scale of several mA. I_g is a precursor sign of failure when it increases quickly and significantly. In the case of the "B" amplifiers, it turns out that there is no significant variations. On the other hand, the variation of I_g of the device "A02" suggests that there will be in a short time a modification of the performances.

For Test2, the "B" amplifiers show the same general trend evolution as the Test1 devices after 8000h of aging at DC=80% and 4dB gain compression. As shown in Figure 2 and Figure 3, a slight decrease of drain current (shift lower than 8 %) and

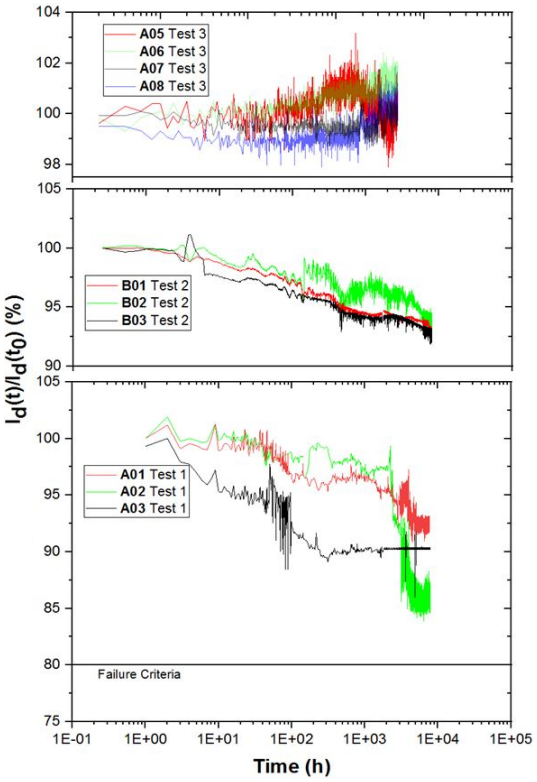


Figure 2: Relative average drain current evolution during stress tests in percentage

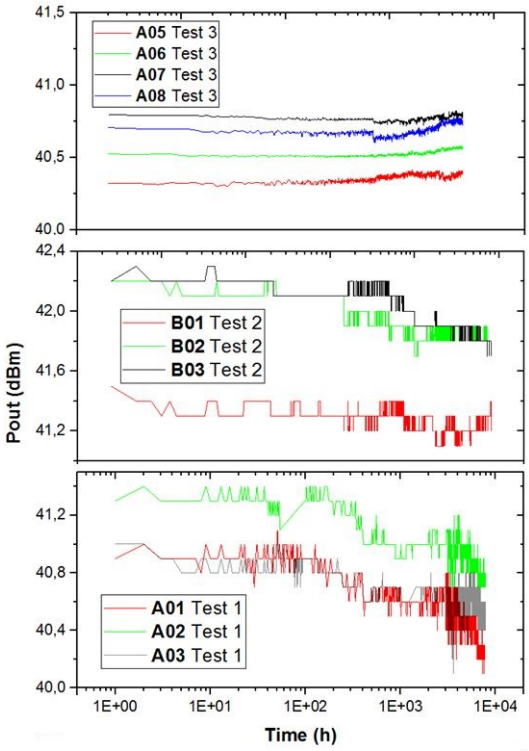


Figure 3: Evolution of the RF output power for the three tests

output power (-0.4 dB) can be observed. The Power Added Efficiency (PAE) evolution during the aging tests (Figure 5) fol-

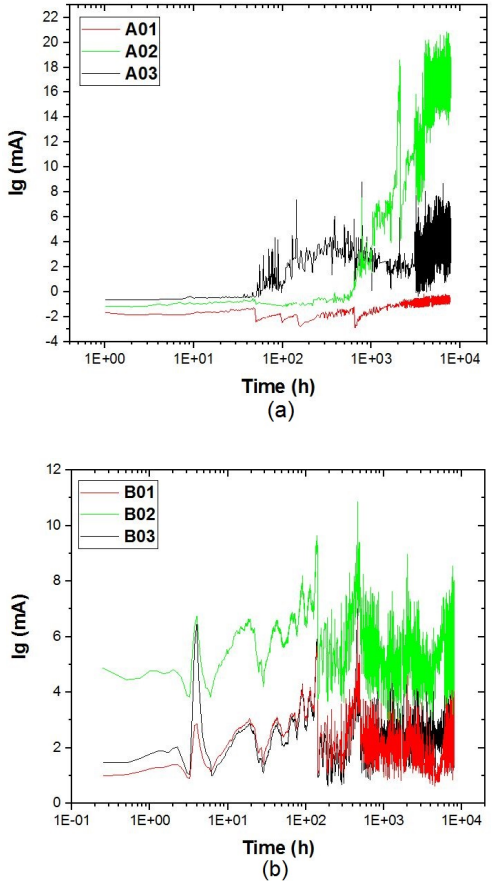


Figure 4: Gate current evolution during stress tests (a) Test 1 (b) Test 2

lows the evolution of the drain current and the output power. The PAE drops by 4% for the Test1 devices and 2% for Test2 devices. The "B" devices operate at higher current density than the "A" devices. However, this fact, the "A" devices aged with 6dB of gain compression manifest much higher variations than the "B" devices. This suggests that compression has an important role in aging. Other longer test will try to validate this result. Given the duration of the tests, this will be done in a further work.

From the interim measurements, complementary information about the aged devices could be extracted. The schottky characterizations validate the gate stability of all devices as schottky parameters (Schottky barrier, Ideality factor) do not vary. Many efforts were made to stabilize the schottky gate of AlGaN/GaN HEMTs by modifying the HEMTs structure (such as adding GaN cap [19, 20, 21] or SiN passivation layer [22]), or by using a gate metal with higher work function (i.e., Pt, Mo [23], Cu [24] etc.) or diversion to metal-insulator-semiconductor heterostructure field-effect transistors (MISHFETs) [25, 26]. The gate stabilization in our test may be due to these improvements in the manufacturing process. However, we notice from the reverse schottky characteristics, that the reverse gate leakage current shows a slight variation in the early hours of the stress (Figures 6-a and 7-a): For the aged devices in Test2, I_{gss} decreases in the first 1000 h of aging then stabilizes gradually. For the

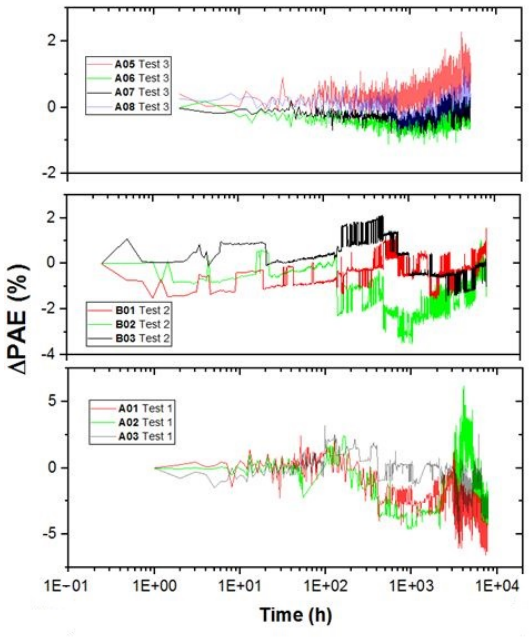


Figure 5: Power added efficiency evolution during stress tests in percentage

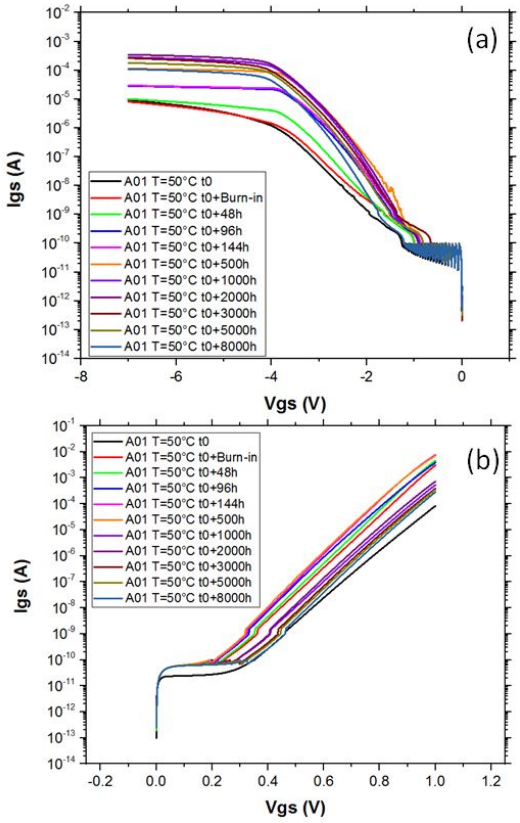


Figure 6: Schottky Characteristic of the device "A01" (a) Forward (b) Reverse

Test1 devices, I_{gss} increases for the first 3000h then recovers and decreases. Generally, the gate leakage current reduction is attributed to trapping phenomenon.

An easy way to get an idea about the evolution of traps is

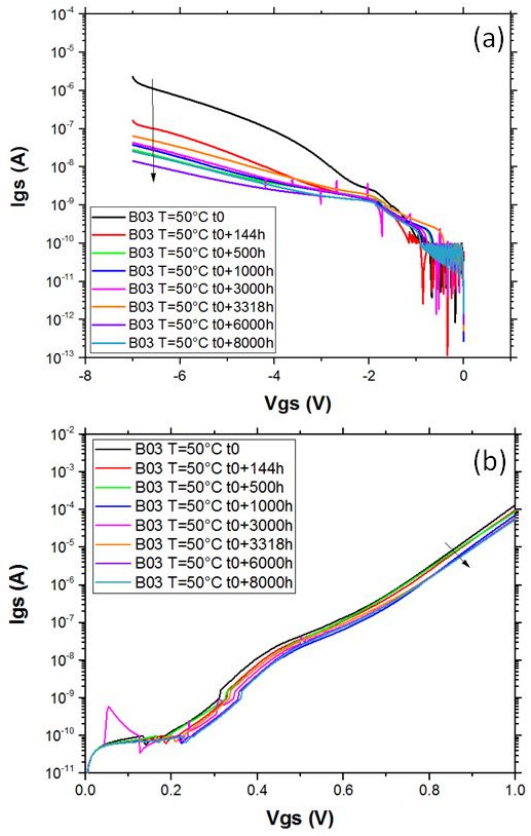


Figure 7: Schottky Characteristic of the device "B03" (a) Forward (b) Reverse

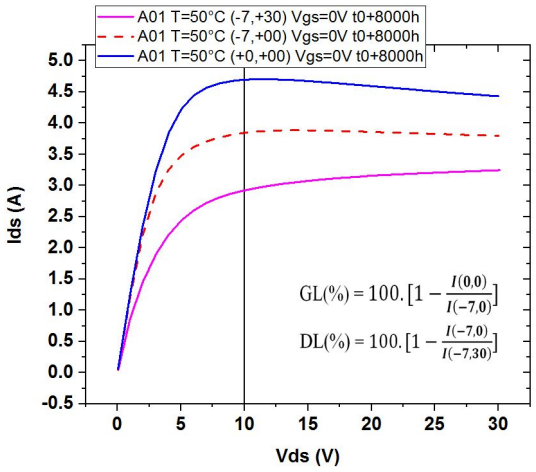


Figure 8: Output characteristic of the A01 device at t0+8000h for different quiescent points

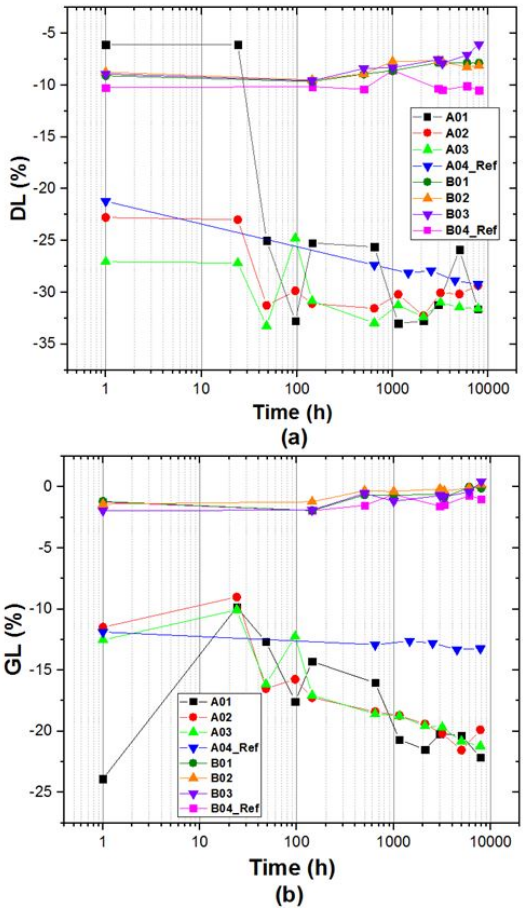


Figure 9: Drain-lag and Gate-lag evolution during stress tests 1 and 2

by drain-lag and gate-lag measurements using I-V pulsed characterizations at different quiescent points. In fact, the point (V_{GS0}, V_{DS0}) = (0V, 0V) is the standard quiescent point. The point (V_{GS0}, V_{DS0}) = (-7V, 0V) is used to quantify the possible trapping effects at the gate, whereas the point (V_{GS0}, V_{DS0}) = (-7V, 30V) allows the presence of traps at the gate and drain in the same time. From the output characteristics of the device in these three points (Figure 8), we can quantify the phenomenon of gate-lag and dain-lag, during the stress at each interim measurement.

An increase of the drain-lag (around 10%) and the gate-lag (close to 2%) have been observed for the Test1 devices (Figure 9). However the Test2 devices have shown a slight decrease of these parameters (around 2%) (Figure 9).

This suggests an evolution of the quantity of traps in the buffer and in the gate edges. To have more information about these traps (energy level, time constant, capture cross section), more characterizations in Athermal DC Transient Spectroscopy (A-DCTS) [27] or current or capacitance deep level transient spectroscopy (CDLTS or DLTS) must be conducted [28, 29, 30]. Trap measurements are carried out at many different temperatures, which take a lot of time that cannot be allowed during recovery measurements. We therefore did not consider performing these measurements until the end of the tests. The technique that will be used is A-DCTS [27].

The On-state resistance and the threshold voltage are one of the parameters that have varied during the aging tests "1" and "2" (Figure 11 and Figure 10). The On-state resistance of all devices has increased during the stress leading to a decrease of the drain current. A decrease of V_{th} has been noticed for the Test1 devices except the device "A02" that represents a positive shift of V_{th}. The evolution of the threshold voltage of the Test2 devices is similar to the device "A02". The negative shift of the

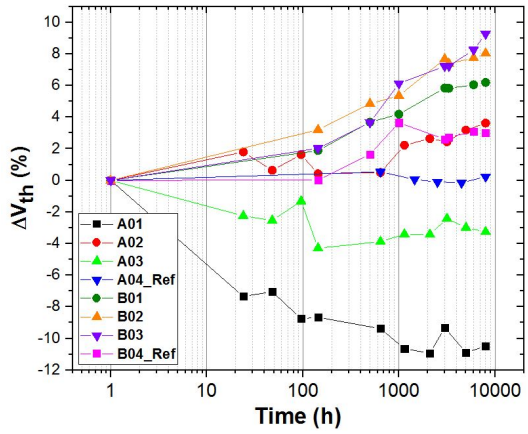


Figure 10: Evolution of the relative Threshold voltage variation during stress

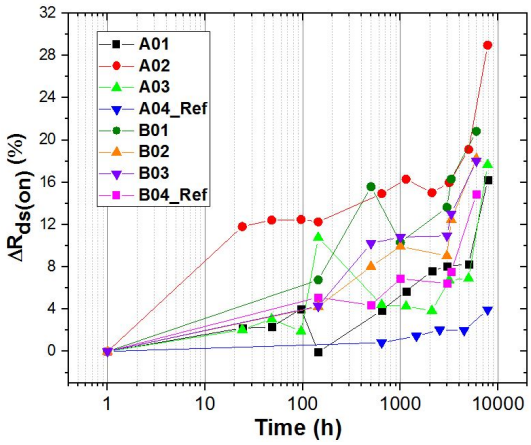
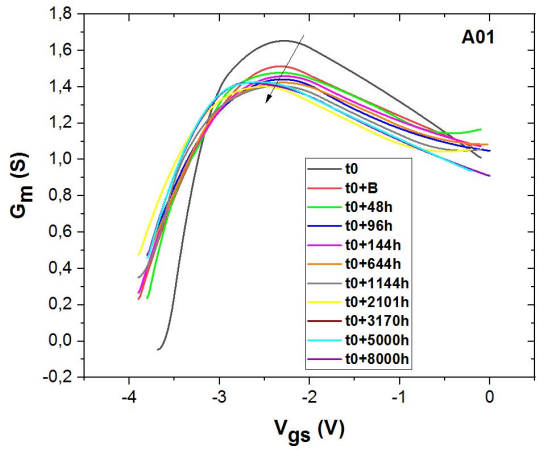


Figure 11: Evolution of the relative On-state resistance variation during stress



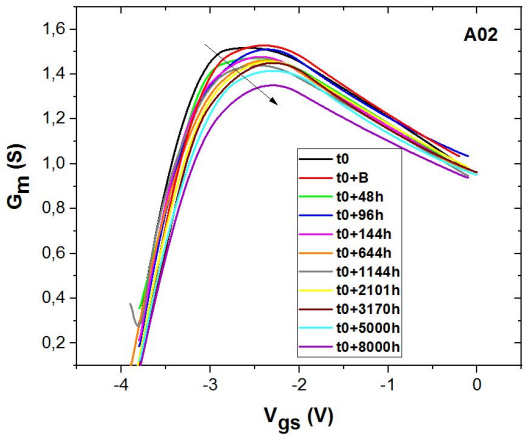


Figure 12: Test 1 devices transconductance evolution during stress

threshold voltage can be caused by an increase in charge carrier concentration in the channel below the gate after the stress [31]. However, the V_{th} positive shift indicates an accumulation of negative charges trapped under gate region [32, 33]. The shift of V_{th} is also noticed on the extracted transconductance curves ($G_m - V_{gs}$) presented in Figure 12. For Test1, the devices have the same G_m behavior under stress except the "A02" which has a behavior similar to the Test2 devices. This suggests that two different degradation mechanisms can be observed. It appears from the transconductance characteristics that the maximum of G_m decreases during the aging for all the devices of both tests. Test2 devices have exhibited a decrease in drain current with a positive shift of threshold which indicates the trap presence under the gate region. Moreover, an increase of the On-resistance as well as a transconductance reduction were observed, revealing the presence of traps on the gate-drain access region [34].

The little drop of output power and drain current seems to be due to drain-lag and gate-lag effects. The evaluation of the trapping state is then essential for a better interpretation of the results. The interim measurements performed on the reference devices "A04_Ref" and "B04_Ref", indicate that the board, the electronics of the board, the circuit and the whole measurement branch are stable at the used base plate temperature.

4. Conclusion

This paper investigates the reliability of AlGaN/GaN HEMTs using long duration aging tests under radar operating conditions in order to update the FIDES guide by constructing a reliability prediction model taking into account the effect of drain voltage, junction temperature, duty cycle and gain compression. The first results of the aging tests show little drift of RF and DC performances of the aged transistors. This suggests that these technologies are reliable for radar applications. We have reported a small decrease in output power, drain current and transconductance, in addition to an increase in the On-state resistance and a shift of the threshold voltage. The variation in electrical parameters seems to be related to drain lag and gate lag effects. A-DCTS measurement will be performed at the end of the aging tests in order to characterize the traps. In this work, two technologies were studied and aged at two different current densities. The aging of the "B" devices shows that despite a higher current density, the evolution of the electrical parameters is lower. This suggests that gain compression is probably the parameter that has the most important impact in aging. The aging tests presented in this paper are being pursued and the failure analysis will be performed at the end of the tests and be presented in another work. In a short term, the results will also be compared with manufacter's qualification data in terms of

end of life mechanisms.

Acknowledgements

The authors would like to thank the French Ministry of Defence for their support. This work is funded by the French Defence Procurement Agency (DGA), contract n°2015 91 0907.

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