

Beyond 100 GHz: High frequency device characterization for THz applications

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Where I am from?



Bordeaux



IMS-Lab



Strategy of IMS

Fields of expertise

➤ Established

- Compact modelling and RF-characterization
- RFIC design
- IC reliability

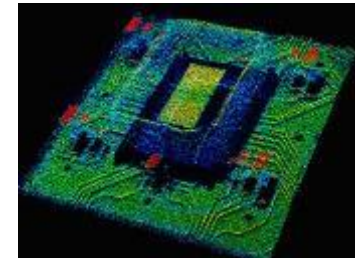


➤ Emerging

- Bioelectronics
- Organic electronics



2 → Expertise



Biographical Summary

Prof. Thomas Zimmer

- **Education**

- 1983 – 1989 University Study, Physics, University Würzburg, Germany
- 1990 – 1992 Ph.D. Student at University Bordeaux 1

- **Professional Life**

- 1989-1990 Research employee, Fraunhofer Institute of Erlangen, Germany
- 1992-1993 Research employee – Adera, France
- 1993 Assistant Professor (MdC), University of Bordeaux 1
- 2003 Professor, University of Bordeaux

- **Degrees**

- 1989 Master Degree in physics, University of Würzburg, Germany
- 1992 PhD: University of Bordeaux
- 2001 Habilitation: University of Bordeaux

- **Further Professional Activities**

- 2002 Cofounder of the company XMOD Technologies
- 2008 Senior Member of the IEEE
- 2008 – 2015 Head of the research group Nanoelectronics at the IMS Lab
- 2012 TPC chair of the ESSDERC conference
- 2013 Organizer of Open Bipolar Workshop at the BCTM
- 2014 Organizer of THz-Workshop at the ESSDERC/ESSCIRC
- 2015 Organizer of the Workshop “SiGe for mmWave and THz” at the European Microwave Week
- 2015 Organizer of the Seminar “ SiGe-THz devices: Physics and reliability ” in Bordeaux

Acknowledgement

- Bertrand Ardouin (XMOD Technologies)
- Christian Raya (PhD, PostDoc, now with XMOD Technologies)
- Peter Baureis (Professor, FH Würzburg, Germany)
- Arnaud Curutchet (Associate Professor, IMS - Bordeaux)

Outline

I. Context: THz: applications

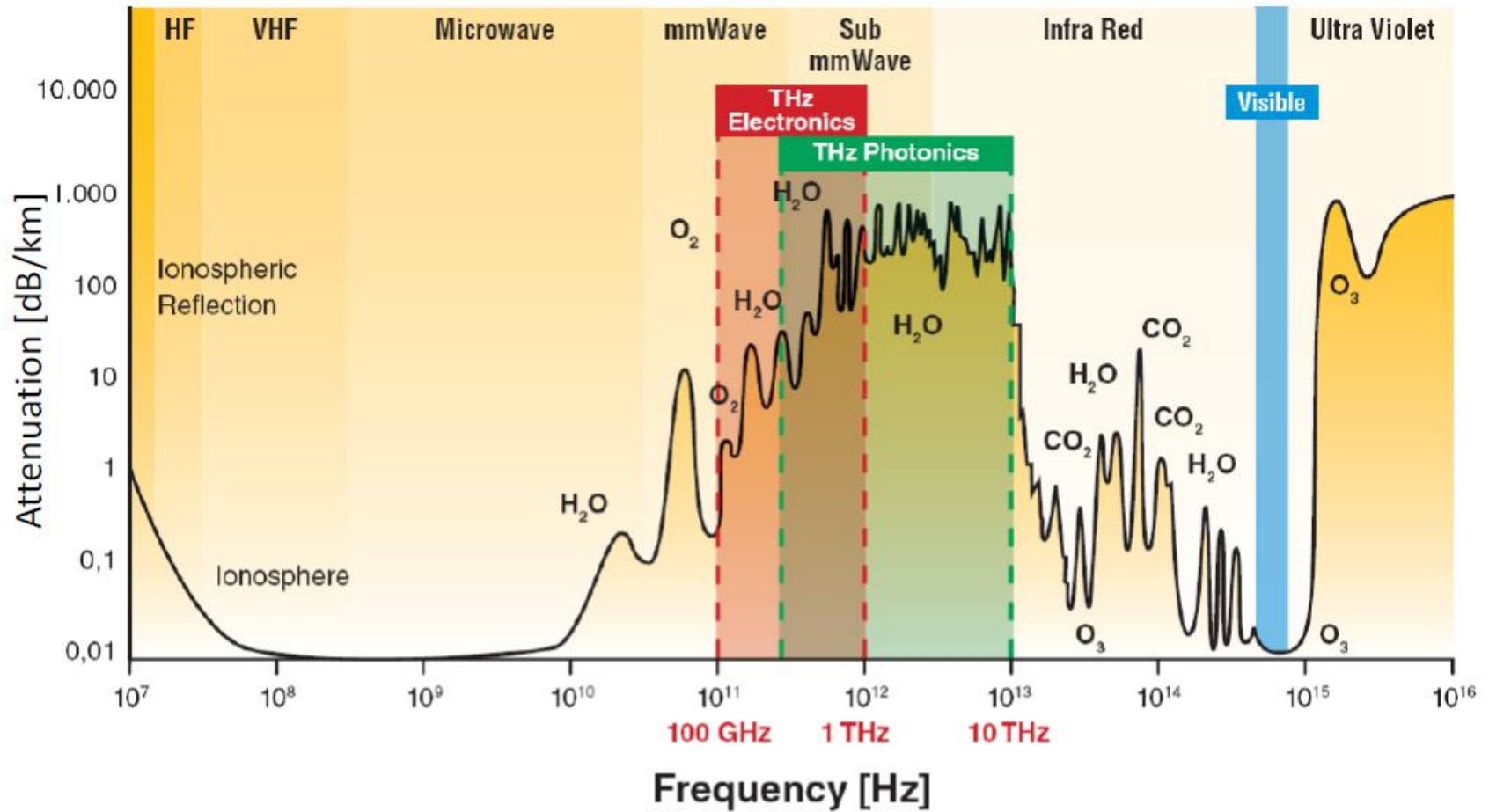
II. State of the Art of calibration and deembedding

III. On-wafer calibration improvements

IV. Beyond 100GHz

V. Conclusion

Where could we use silicon?



Source: U. Pfeiffer, DOT7 WS 2015

Why Silicon for terahertz?

- III/V dominated
 - High performance
 - Low volume production
 - Low integration level
- Silicon technologies
 - Low performance in comparison with III/V
 - Enable system-on-chip
 - Low power consumption
 - Reduced cost at high volumes



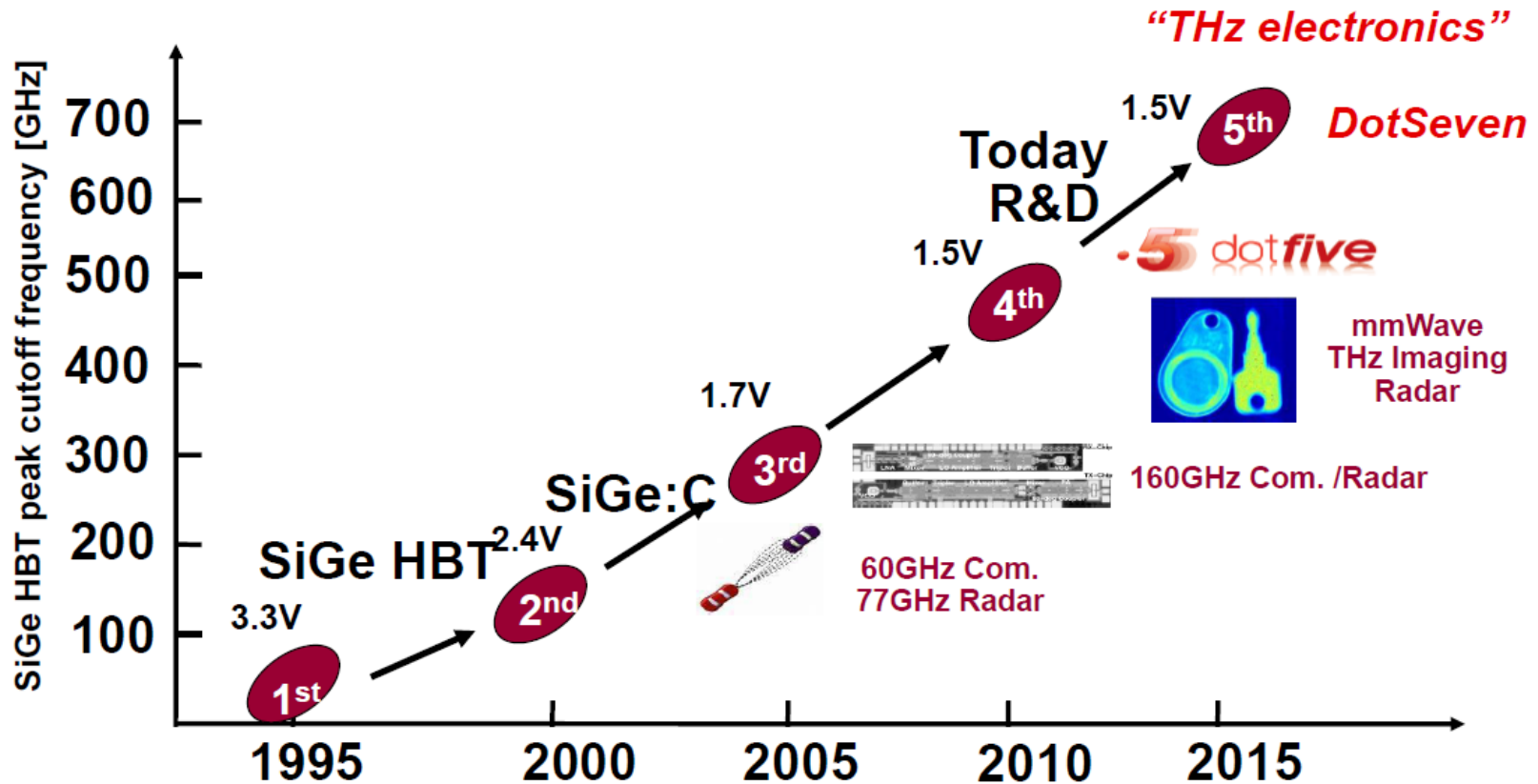
<http://www.teraview.com>



H. Sherry *et. al*, ISSCC 2012

Source: U. Pfeiffer, DOT7 WS 2015

BiCMOS Technology Evolution

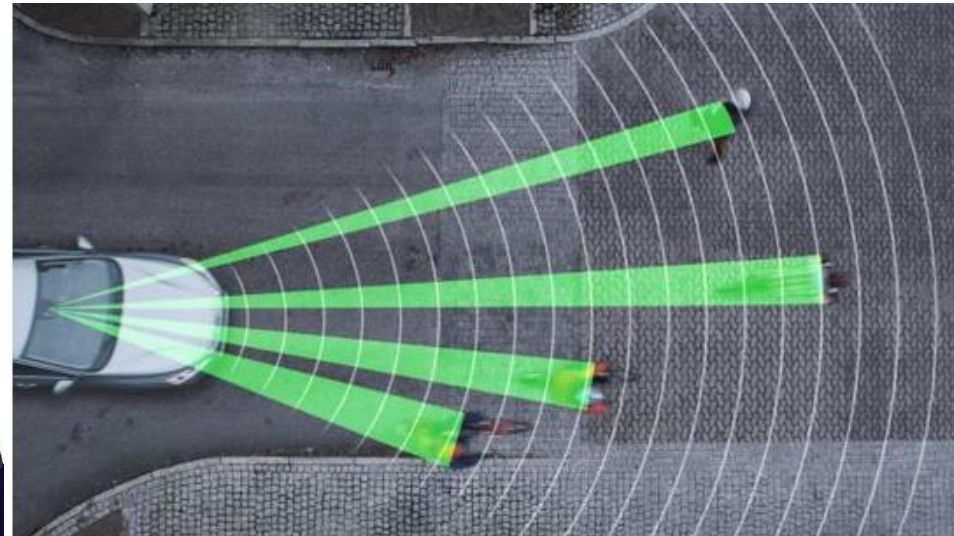


Source: U. Pfeiffer, DOT7 WS 2015

Application: Automotive radar



Source: NYSTEIN

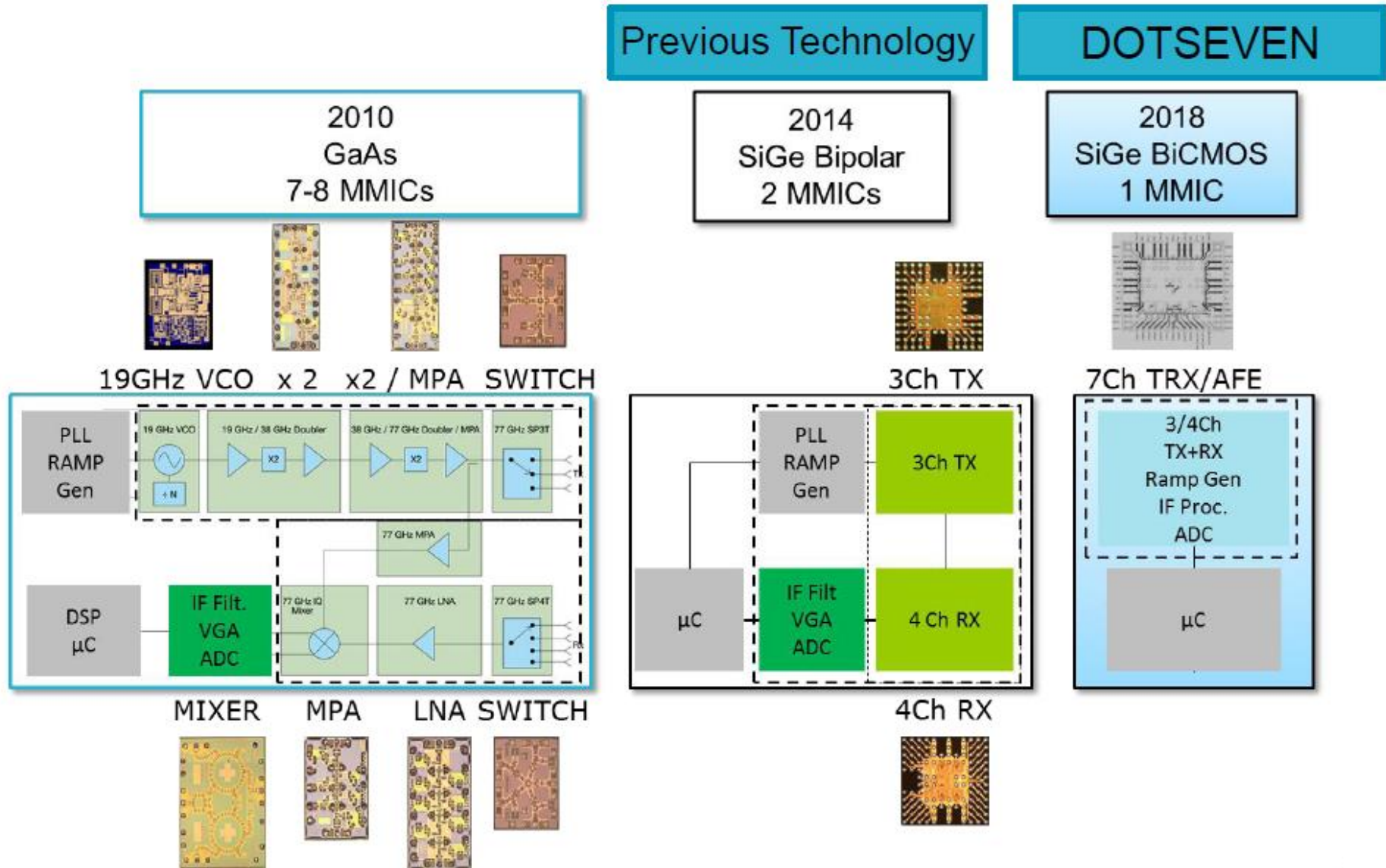


Source: eetimes

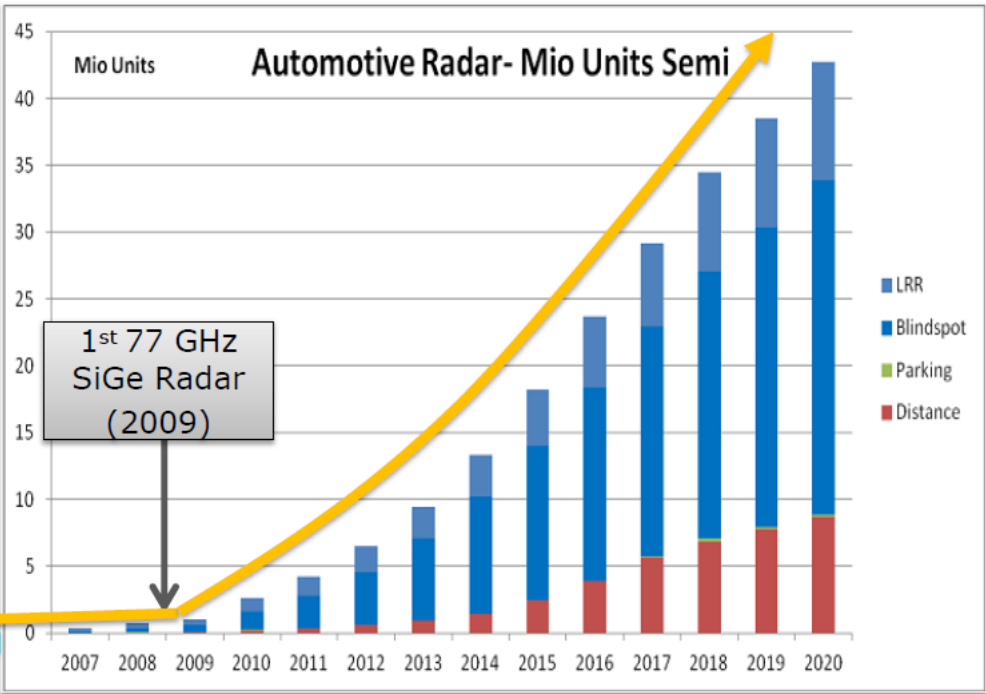
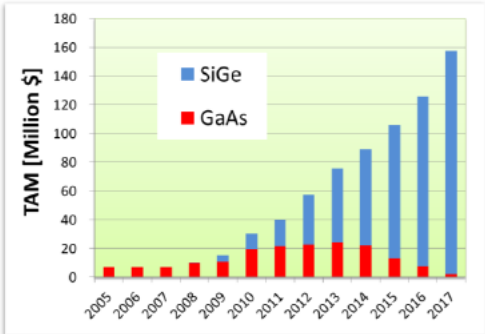


Source: remcom

Impact of SiGe on Radar Sensors



Impact of BiCMOS on Automotive Radar Market

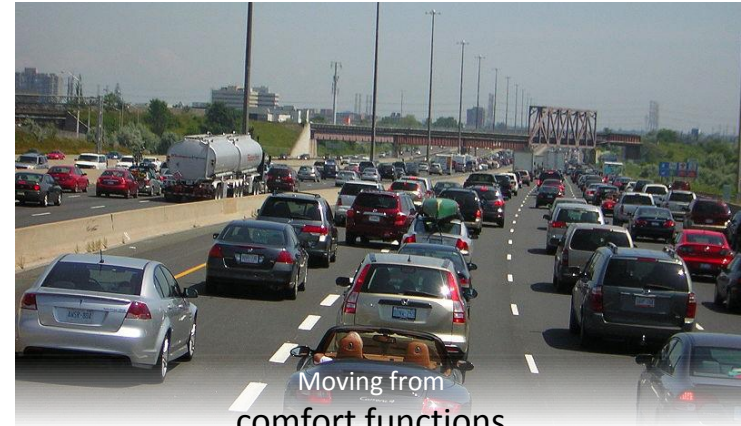


1st Car Radar
(Mercedes Distronic)

1999

What comes next?

- In Europe each year about 1.3 million traffic accidents cause:
 - More than 40.000 fatalities
 - Economic damage of more than 200 billion € per year
- Human error is involved in over 90% of accidents
- Automotive radar help drivers to
 - Maintain a safe speed
 - Keep a safe distance
 - Avoid overtaking in critical situations
 - Safely pass intersections
 - Avoid crashes with vulnerable road user
 - Reduce severity of an accident
 - Drive more efficiently



Moving from
comfort functions
(e.g. adaptive cruise control)
in luxury cars

to

safety functions
(e.g., emergency braking, pre-crash preparation)
in every car.

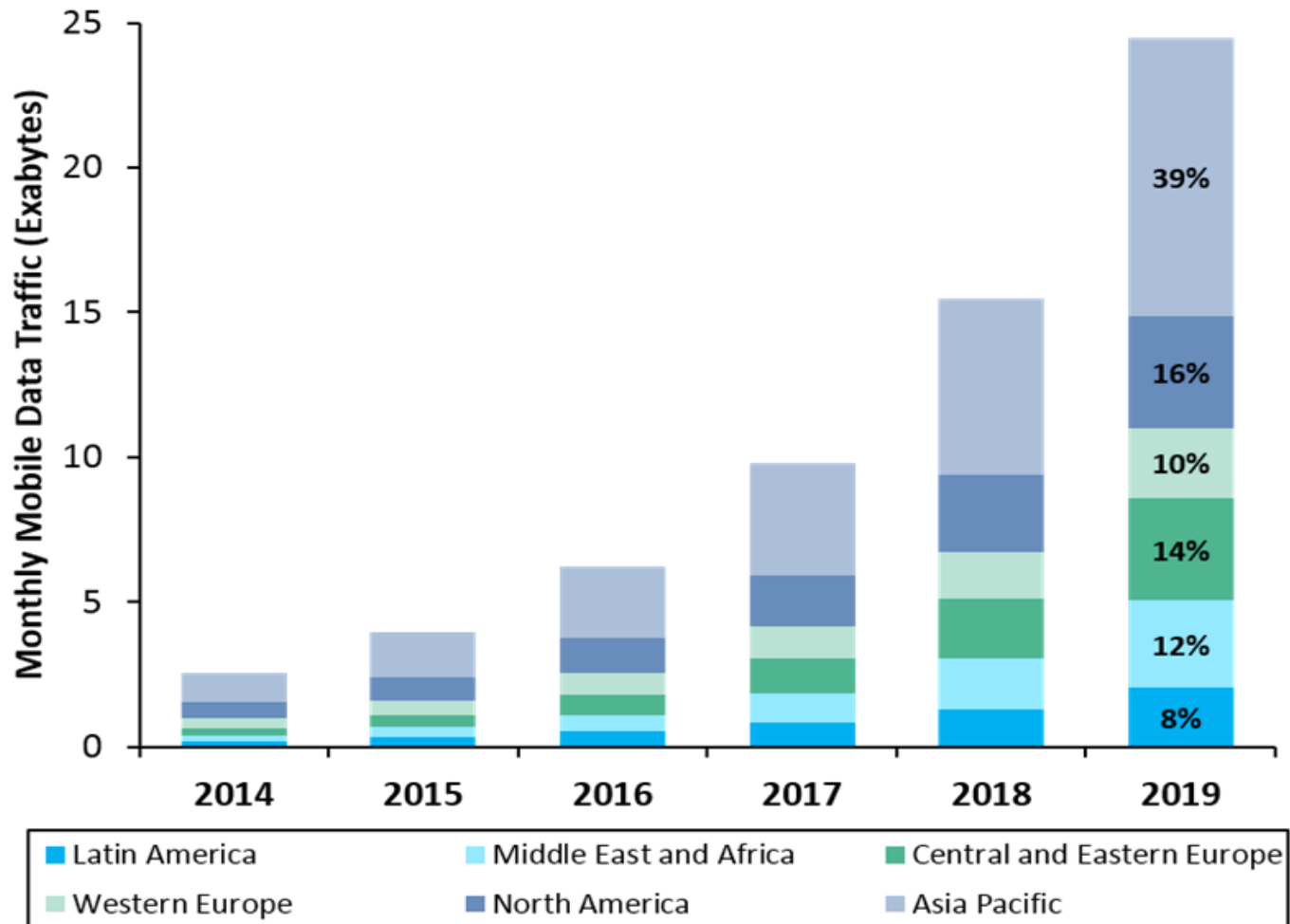


http://en.wikipedia.org/wiki/File:401_Gridlock.jpg

http://en.wikipedia.org/wiki/Rear-end_collision#mediaviewer/File:Car_accident_-_NSE_Malaysia.jpg

Source: H. Jäger, DOT7 WS 2015

Mobile data traffic growth until 2019

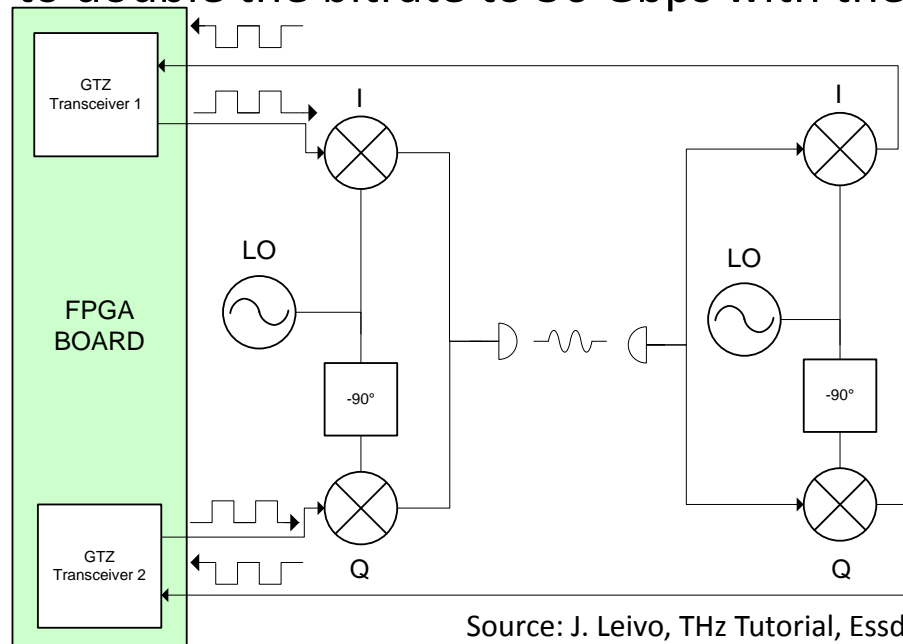


source: Cisco VNI study

=> Need of high data transfer rate

Application: Toward 100Gbit/s

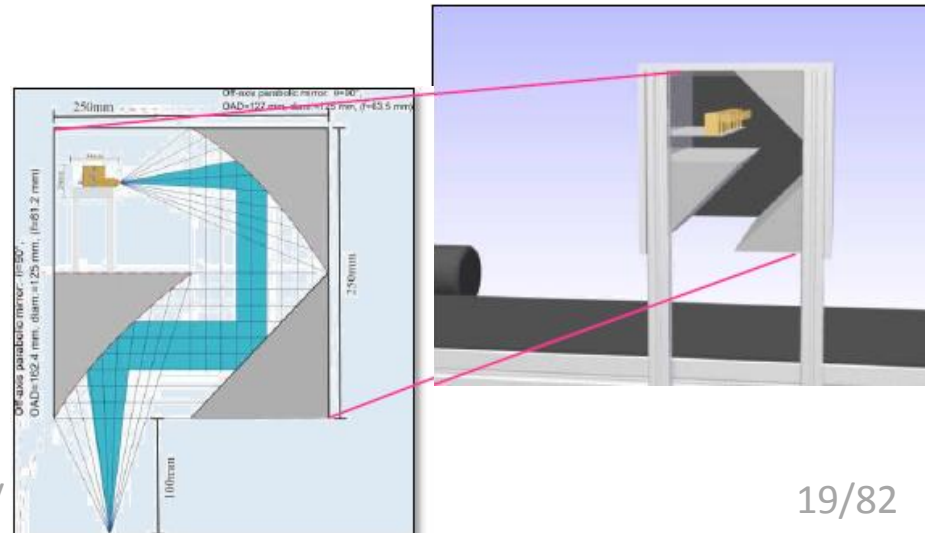
- 56 Gbps Short Range Communication with FPGA and SiGe-transceivers
 - Xilinx Virtex 7 FPGA has high speed transceivers that are capable of generating baseband signals with bitrates up to 28 Gbps
 - Use QPSK with IQ-mixer to double the bitrate to 56 Gbps with the same bandwidth



Source: J. Leivo, THz Tutorial, Essderc 2016

Application: THz Image scanner for material and product testing

- Wideband 240GHz imaging system with excellent spatial resolution
 - 3D-imaging system using coherent THz-TX and –RX for synthetic aperture radar imaging (reflection imaging)
 - Specific Imaging system setup and Image generation
 - Integration of 32 Rx + 32 Tx Modules at 240 GHz
 - Aiming for horizontal and vertical imaging in reflection
- => Non Destructive Control



Application: THz image scanner for security

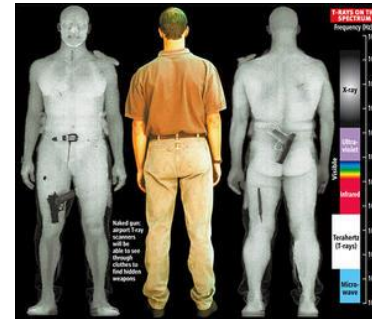
Millimeter-wave technology
for **security scanner**
(airport, railway station etc.)

The security scanner automatically detects
potentially **dangerous objects**:

- under clothing
- or on the body,

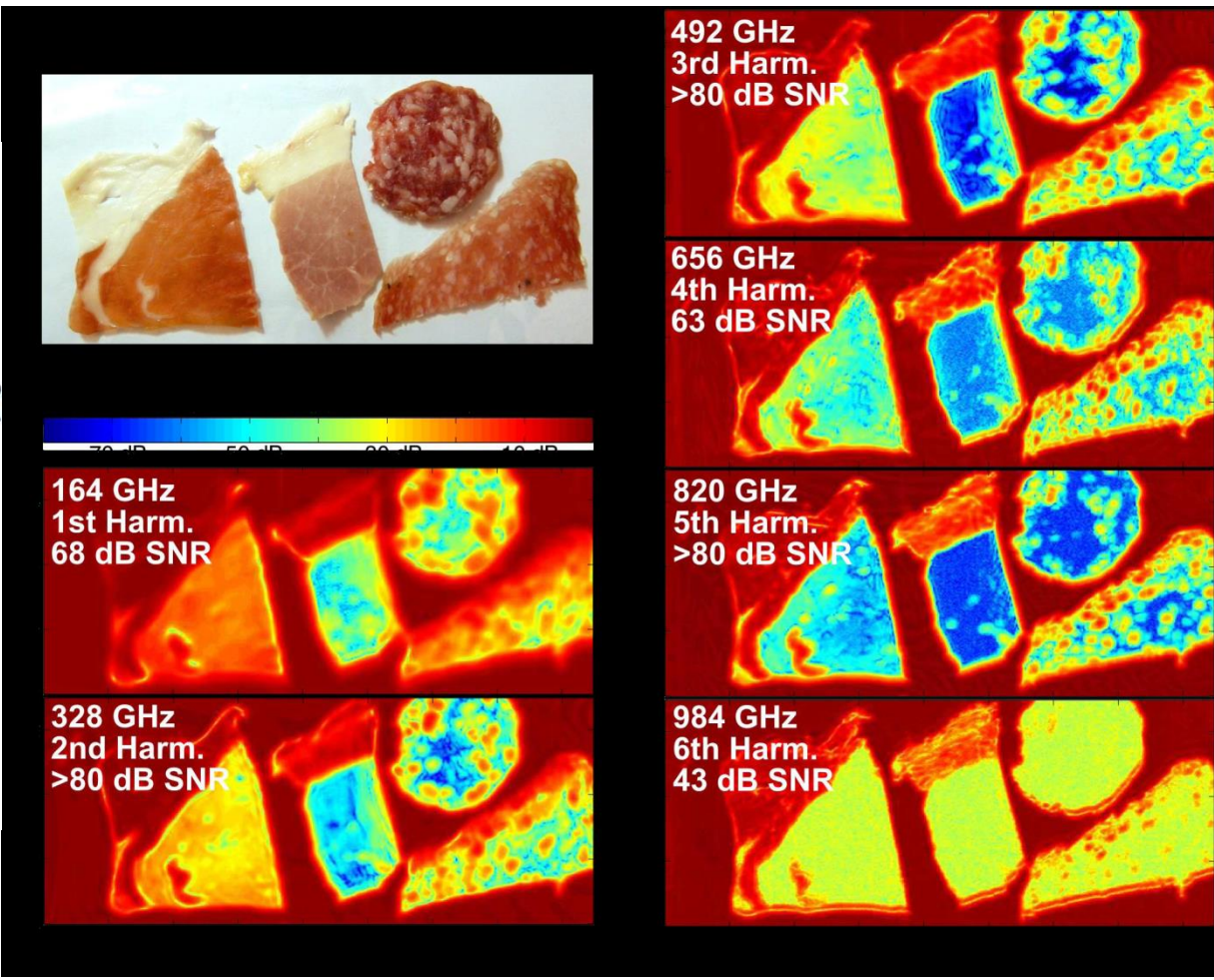
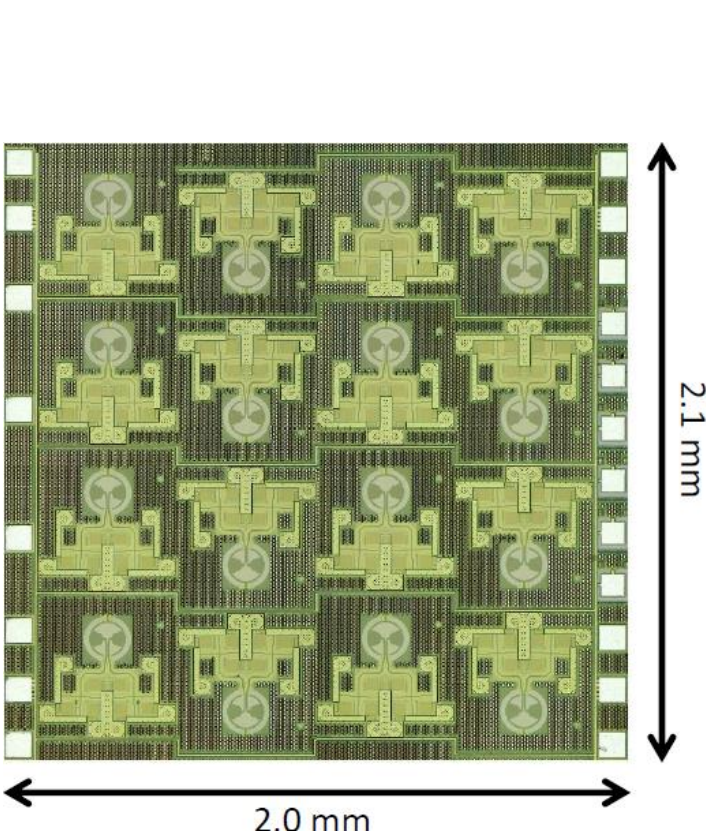
whether they are rigid, flexible, fluid, metallic or non-metallic.

If the scanner reports an alarm,
the **location of the object is marked**
on an avatar, a symbolic graphic of the human body.



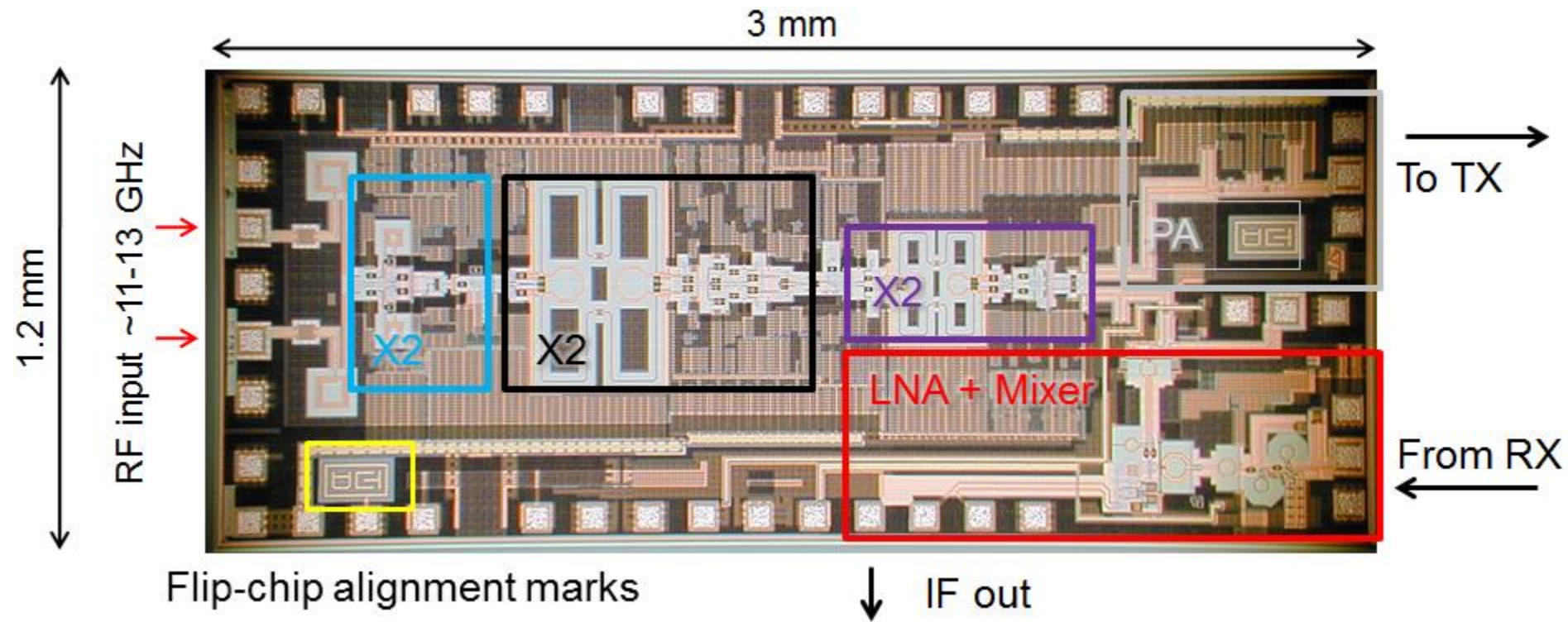
Source: Rohde & Schwarz

Application: THz image scanner for health



System demonstrator IC

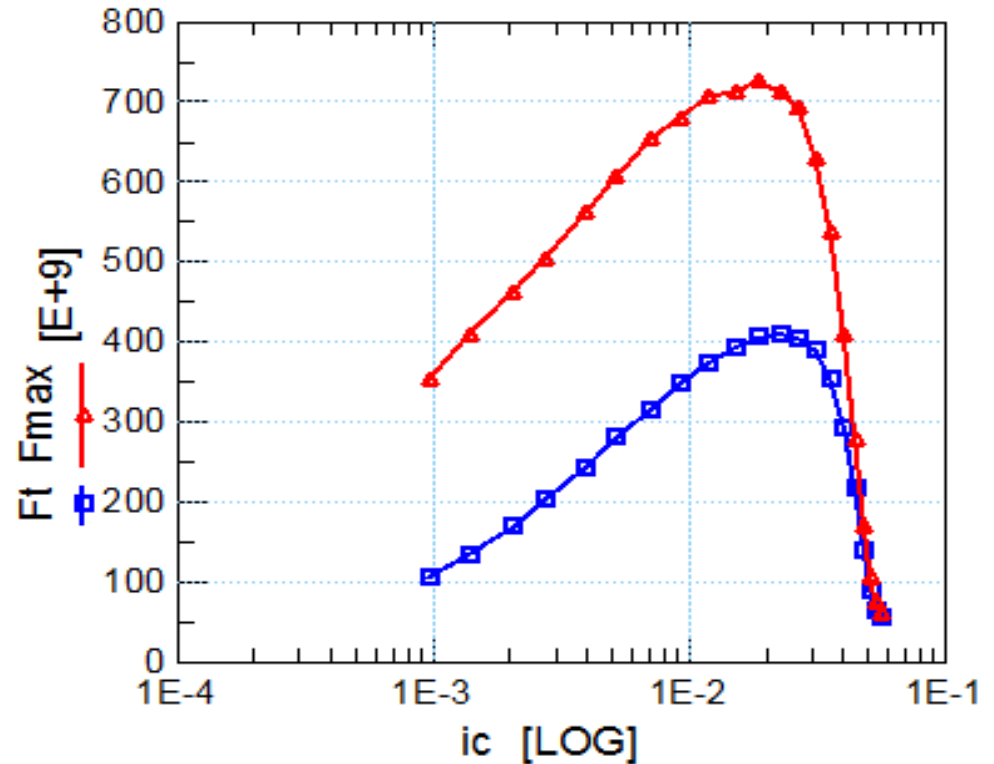
- Single-chip 94 GHz up-conversion and receiver in 0.13 μm Bi-CMOS, integrated in ST 9MW technology (230/280, f_t/f_{max}).



- 8x frequency up-conversion + down-converting mixer

World record of SiGe HBT (IHP)

- SiGe heterojunction Bipolar Transistors operating at a maximum oscillation frequency of 700 GHz
- THz-Applications
 - Automotive radar
 - 100Gbit/s data rate
 - Non-destructive control
 - Security scanner
 - THz imaging for health



Max oscillation freq f_{max} and transition freq of a SiGe HBT transistor fabricated at IHP.
Measurements done at IMS Lab, Bordeaux.

Outline

I. Context

II. State of the Art of calibration and deembedding

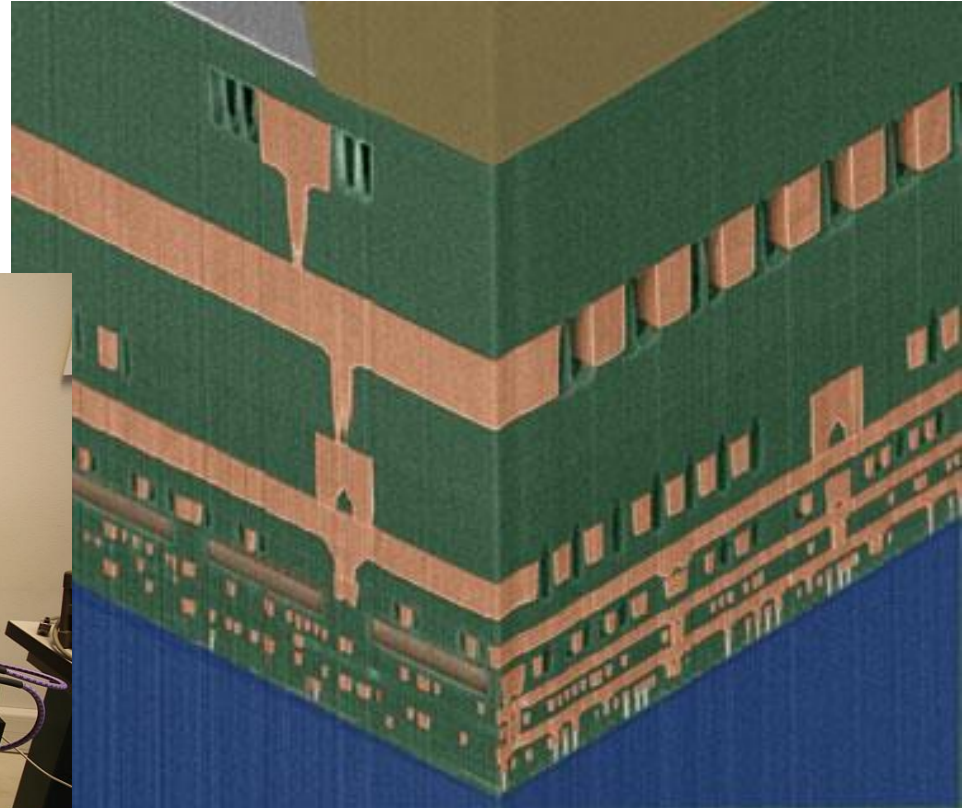
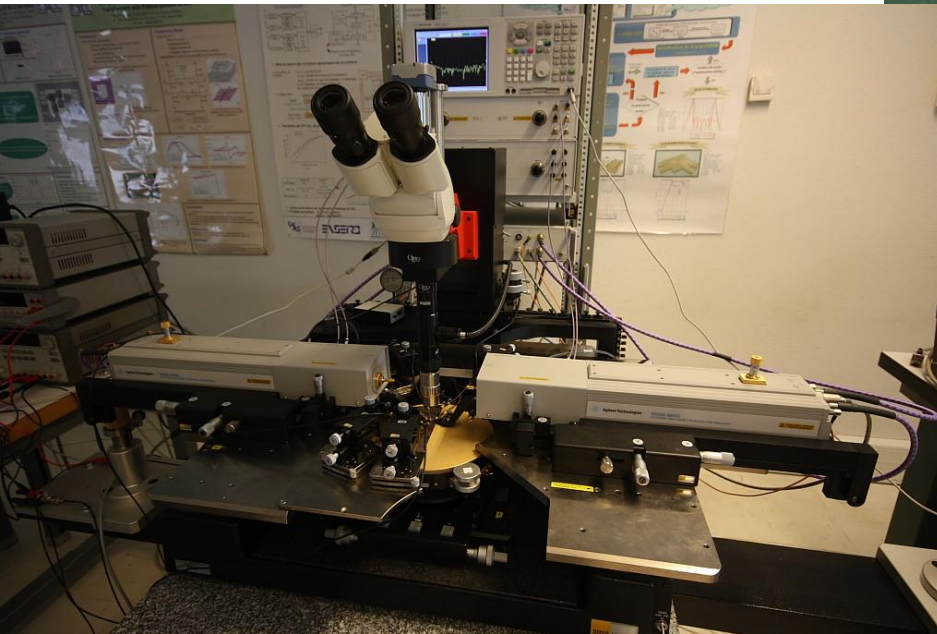
III. On-wafer calibration improvements

IV. Beyond 100GHz

V. Conclusion

Motivation

- Where is the device?



Source: IEEE Spectrum

Outline

I. Context

II. State of the Art of calibration and deembedding

Off-wafer calibration and 4 steps deembedding

On-wafer calibration and deembedding

III. On-wafer calibration improvements

IV. Beyond 100GHz

V. Conclusion

Off-wafer calibration and 4 standards deembedding

Review of calibration techniques

SoA methods 1/1

Acronym	Number of Standards	Error model	Analytical solution	Electrical Hypothesis	Standards width	Wide band
SOLT	4	12 terms	Yes	6 (magnitude and phase of all standards)	Constant	Yes
LRRM	4	8 terms	No	0	Constant	Yes
SSST	4 or 7	8 terms	Yes	6 (magnitude and phase of all standards)	Constant	No
TRL	3	8-12 terms	Yes	1 (REFLECT symmetry+2 length)	Not constant	No
TRM	3	8 terms	Yes	2 (magnitude and phase of match)	Constant	No
LS1S2	3	8 terms	No	0 (+1 length)	Not constant	No

➤ For off-wafer calibration

Direct analytical solution

➔ faster, easily implementable, no optimization step

Constant width

➔ no probe manipulation (higher accuracy)

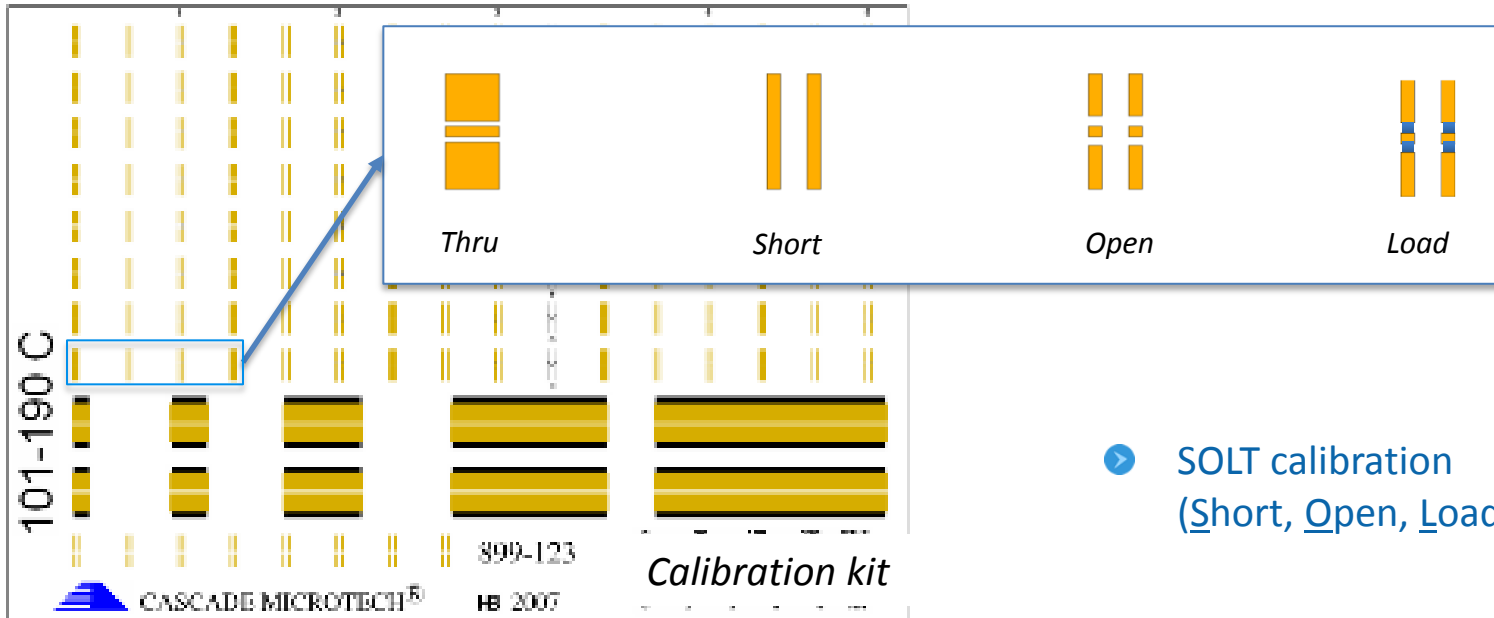
Wide band

➔ measurement between 0,1GHZ and 110GHZ

Off-wafer calibration and 4 standards deembedding

SOLT calibration

Off-wafer calibration 1/8



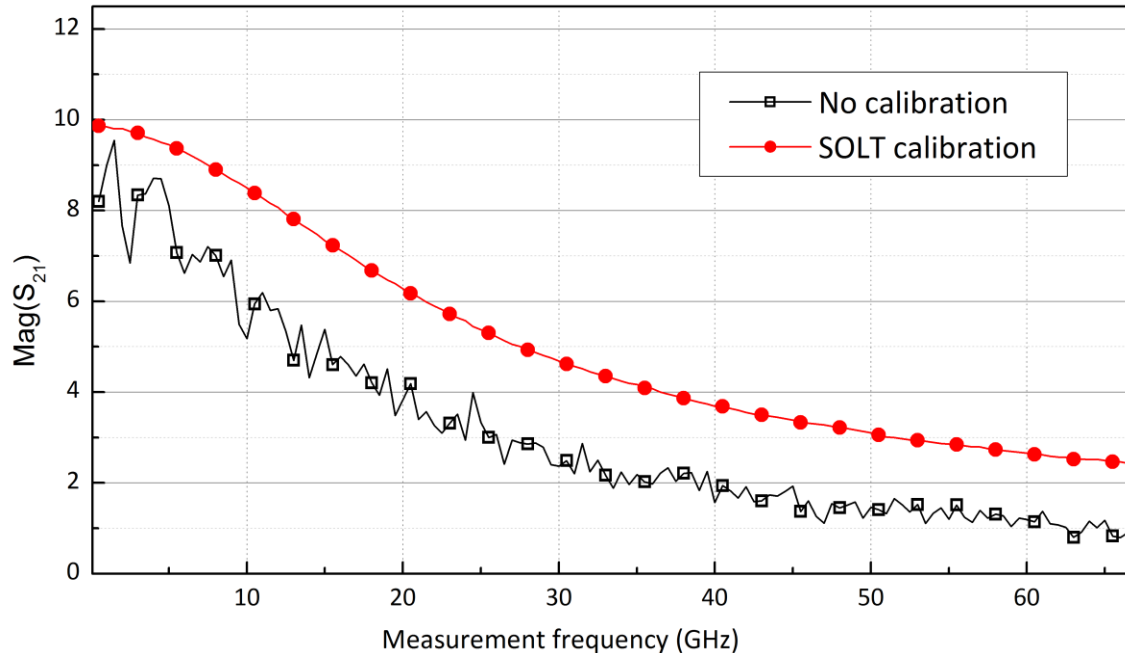
- SOLT calibration (Short, Open, Load, Thru)

Off-wafer calibration and 4 standards deembedding

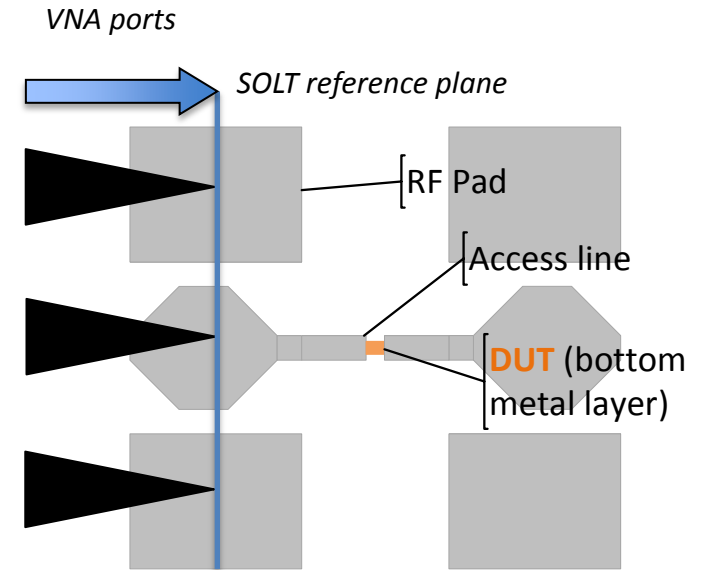
SOLT calibration: Results

Off-wafer calibration 2/8

HBT B11HFC ($5 \times 0.16 \mu\text{m}^2$)



- Better performances
- Smoother curve

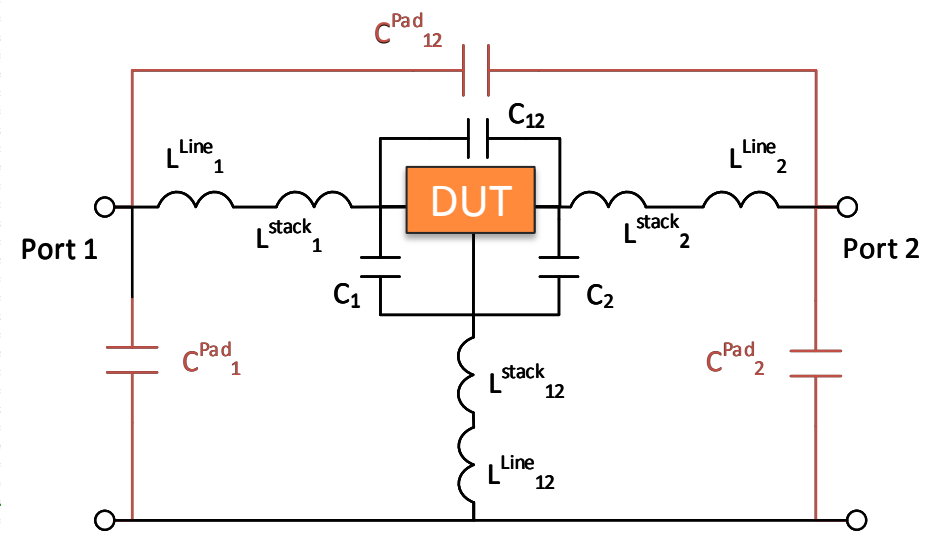
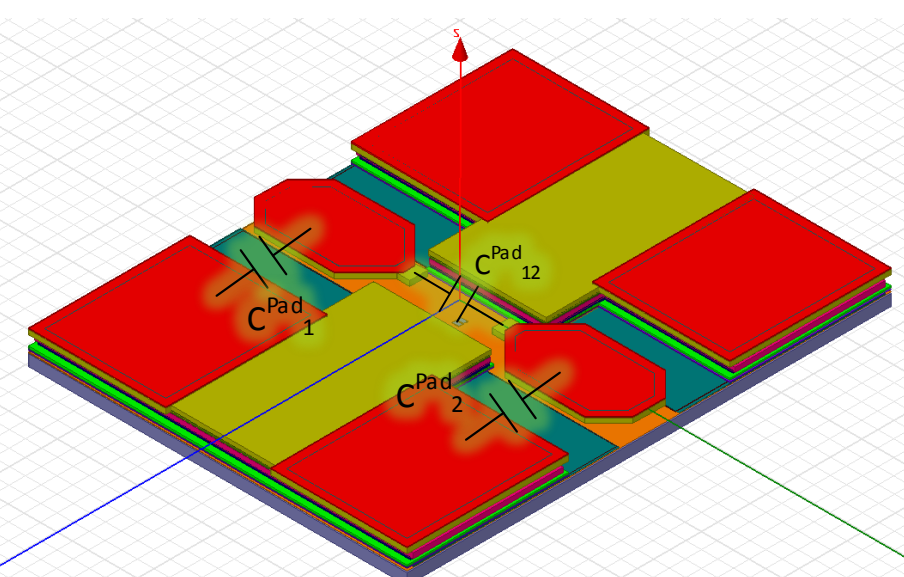


- Reference plane : VNA ports
- RF probes

Off-wafer calibration and 4 standards deembedding

Method PO/PS/CS/CO

Off-wafer calibration 3/8



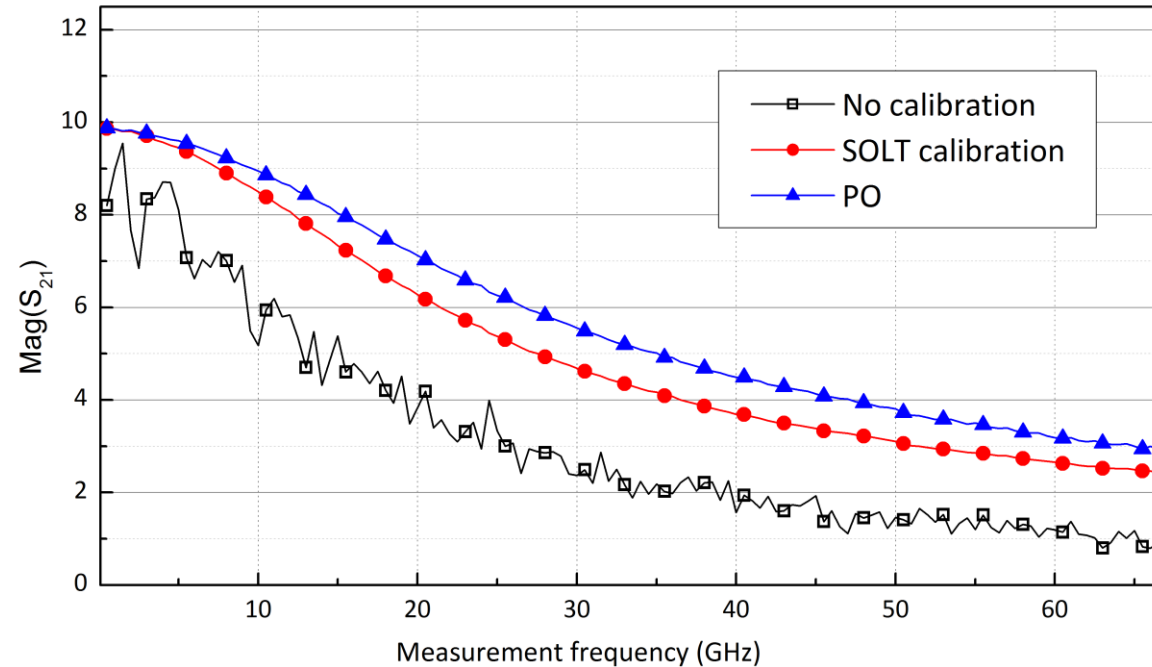
➤ Remove capacitance of RF pad

Off-wafer calibration and 4 standards deembedding

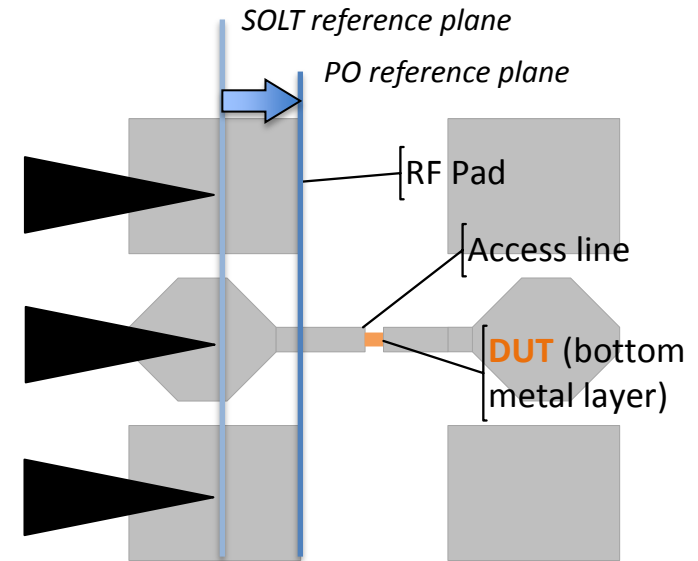
Method PO/PS/CS/CO

Off-wafer calibration 4/8

HBT B11HFC ($5 \times 0.16 \mu\text{m}^2$)



- Better performances at high frequencies
- Reference plane → beginning of access line



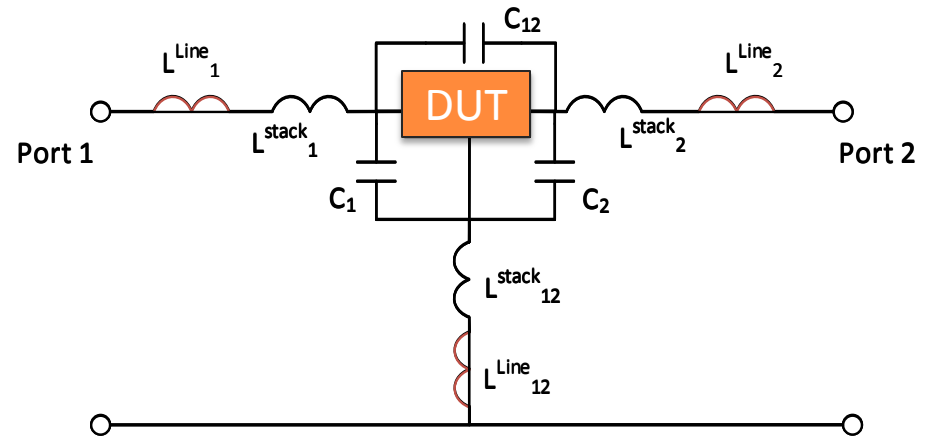
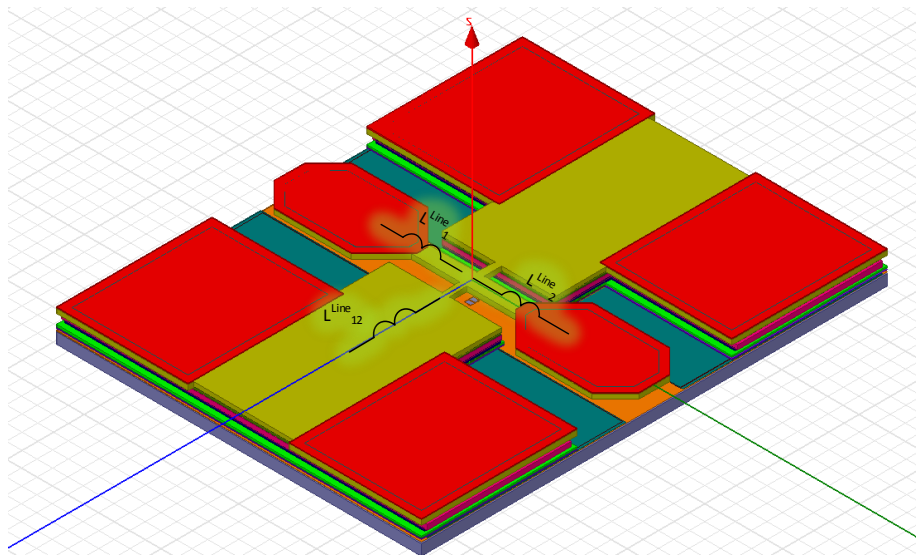
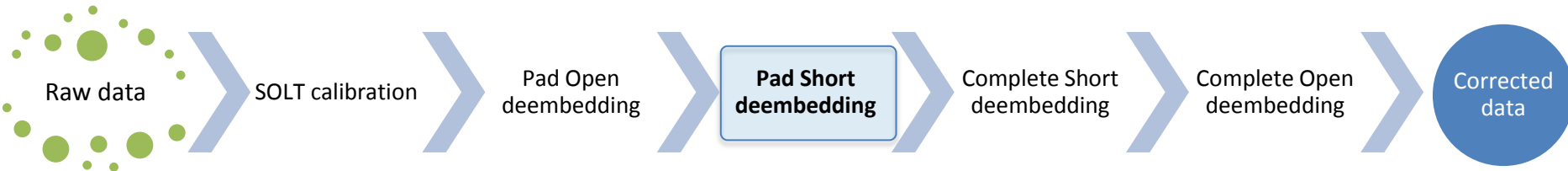
Test structures dimensions

- Pitch = $100 \mu\text{m}$
- $L_{PAD} = 80 \mu\text{m}$
- $L_{LINE} = 30 \mu\text{m}$

Off-wafer calibration and 4 standards deembedding

Method PO/PS/CS/CO

Off-wafer calibration 5/8

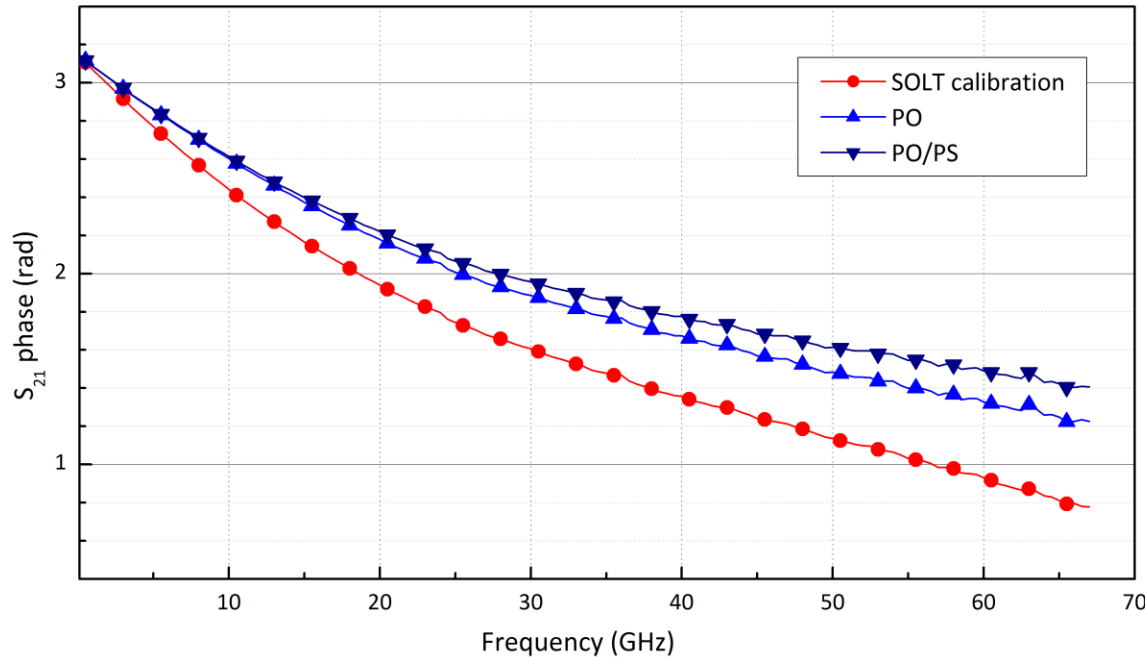


➤ Remove inductance of access line

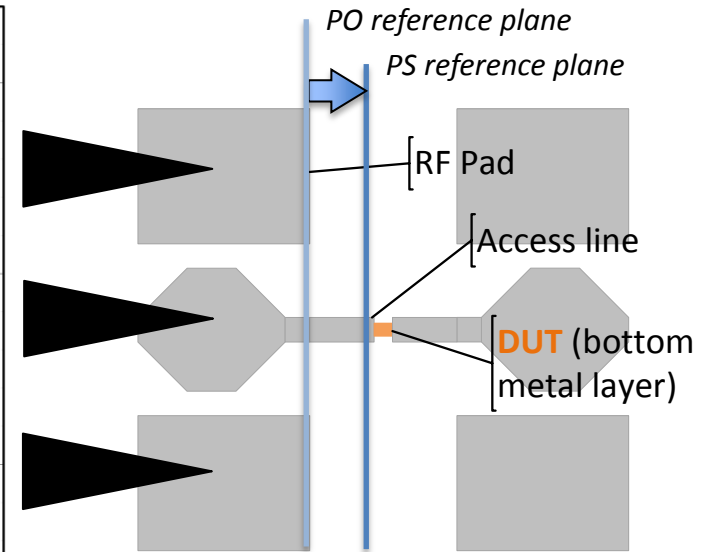
Off-wafer calibration and 4 standards deembedding

Method PO/PS/CS/CO

Off-wafer calibration 6/8



- No significant modification in gain
- Reference plane → end of access line



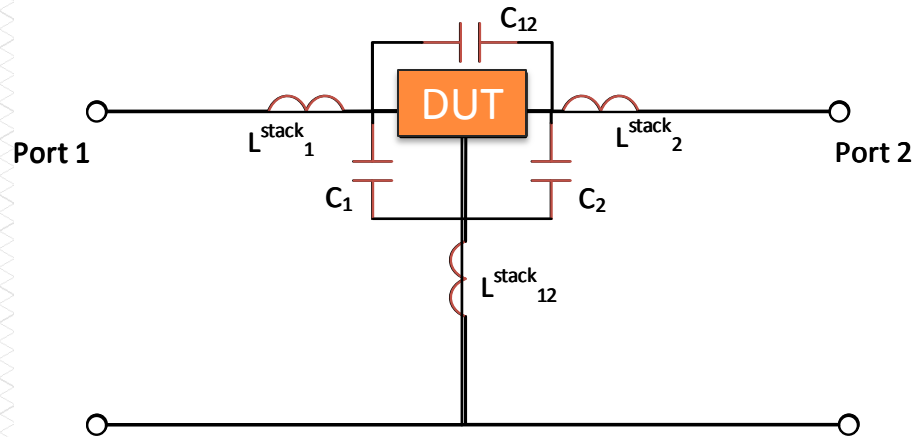
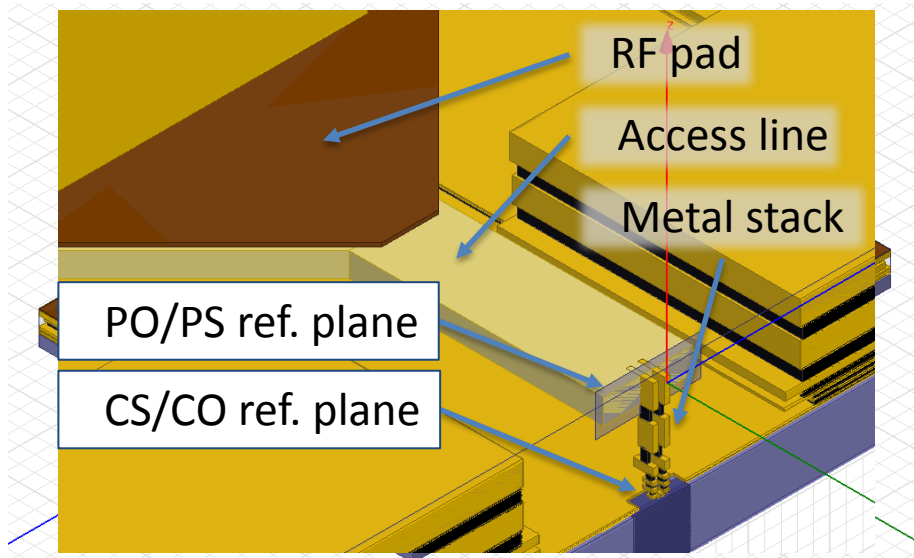
Test structures dimensions

- Pitch = $100\mu\text{m}$
- $L_{PAD} = 80\mu\text{m}$
- $L_{LINE} = 30\mu\text{m}$

Off-wafer calibration and 4 standards deembedding

Method PO/PS/CS/CO

Off-wafer calibration 7/8

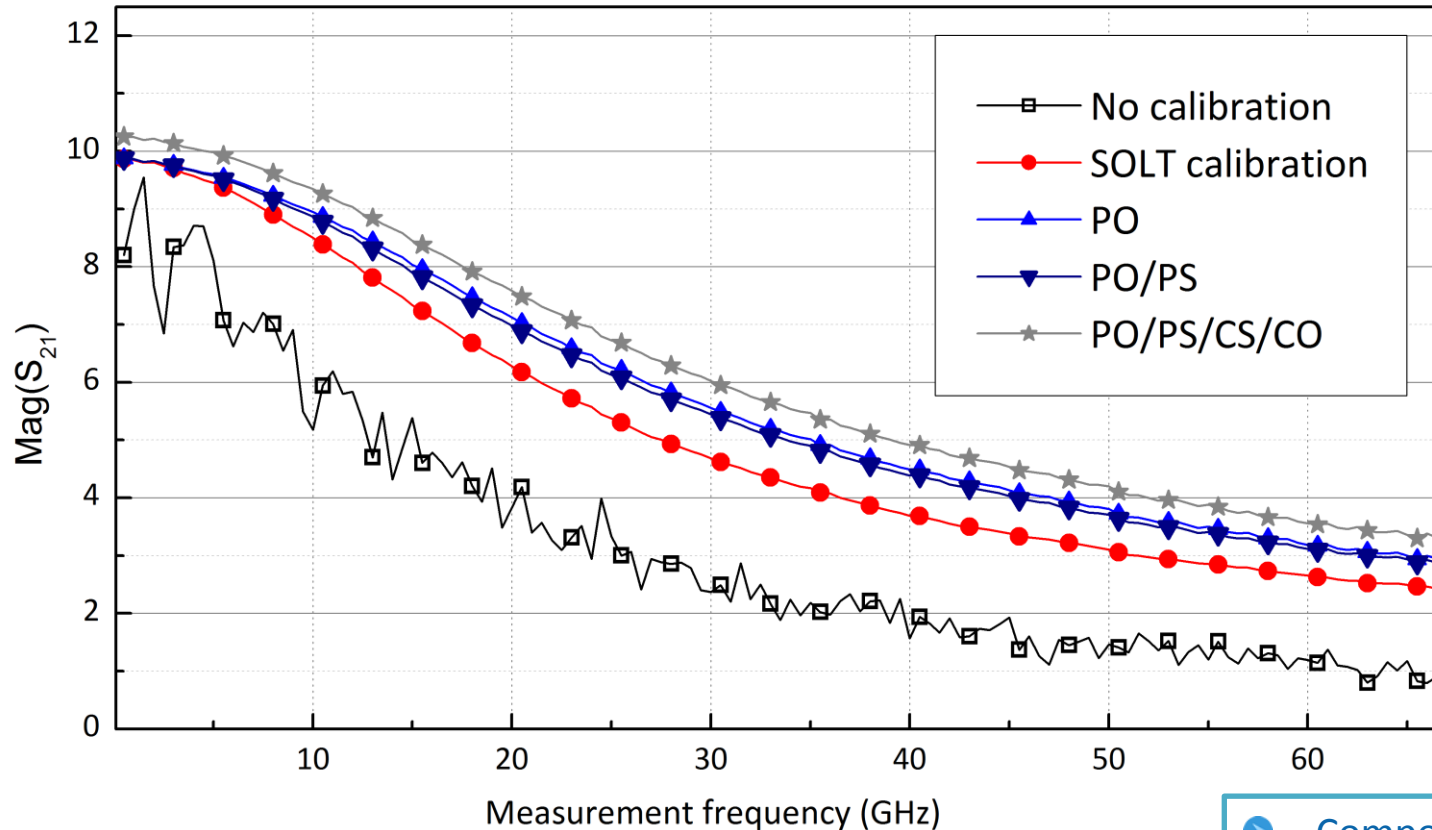


➤ Remove parasitic of metal stack

Off-wafer calibration and 4 standards deembedding

Method PO/PS/CS/CO

Off-wafer calibration 8/8



➤ Component only
Reference plane → DUT contacts

Outline

I. Context

II. State of the Art of calibration and deembedding

Off-wafer calibration and 4 steps deembedding

On-wafer calibration and deembedding

III. Issues and proposed improvements

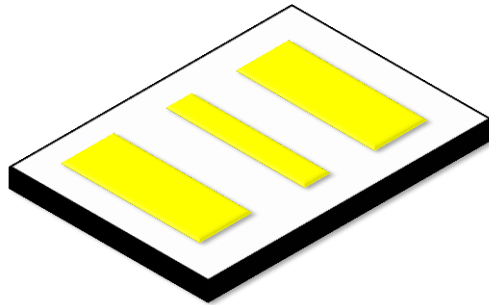
IV. Beyond 100GHz

V. Conclusion

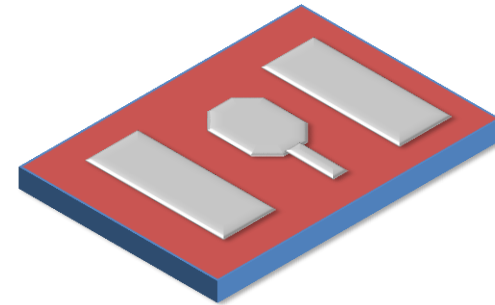
On wafer calibration

Why ?

SoA methods 1/2



≠



- ▶ The calibration kit environment is very different from the silicon one (DUT).

Calibration kit	Silicon wafer
Alumina substrate	Silicon substrate
Rectangular pad	Hexagonal pad
Gold metallization	Aluminum metallization

- ▶ The environment is different, error is introduced in measurement
 - ▶ The solution is on-wafer calibration !

State Of the Art methods

Review of calibration technics

SoA methods 2/2

Acronym	Number of Standards	Error model	Analytical solution	Electrical Hypothesis	Standards width	Wide band
SOLT	4	12 terms	Yes	6 (magnitude and phase of all standards)	Constant	Yes
LRRM	4	8 terms	No	0	Constant	Yes
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TRM	3	8 terms	Yes	2 (magnitude and phase of match)	Constant	No
LS1S2	3	8 terms	No	0 (+1 length)	Not constant	No

➤ For on-wafer calibration

Analytical solution

→ Faster, easily implementable

Few Electrical Hypothesis

→ Less sensitive to variation process

→ Few constraints on the standards accuracy

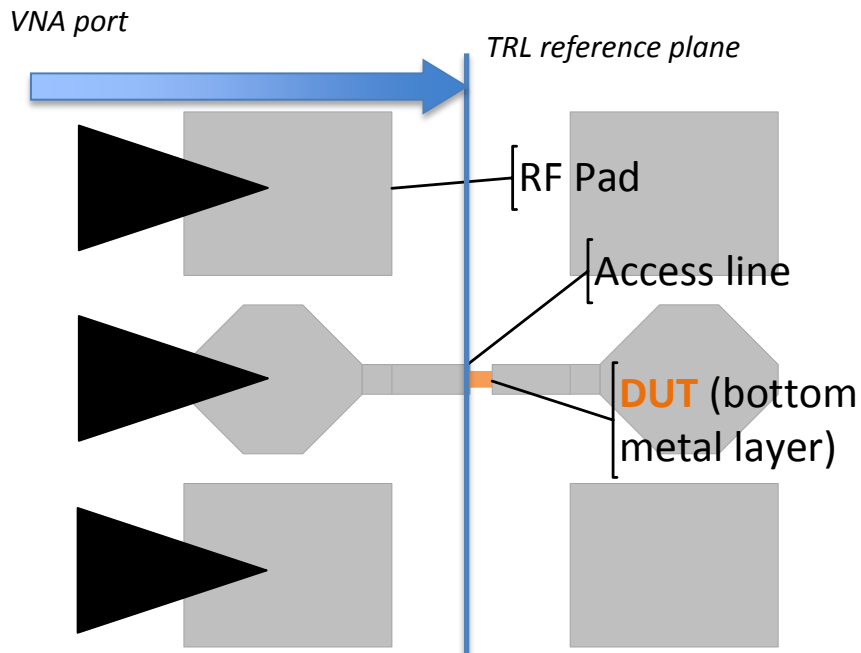
Standard 50Ω Match

→ Very hard to make in mmwave and THz range

On-wafer TRL calibration and deembedding

On-wafer TRL calibration

On-wafer calibration 1/4

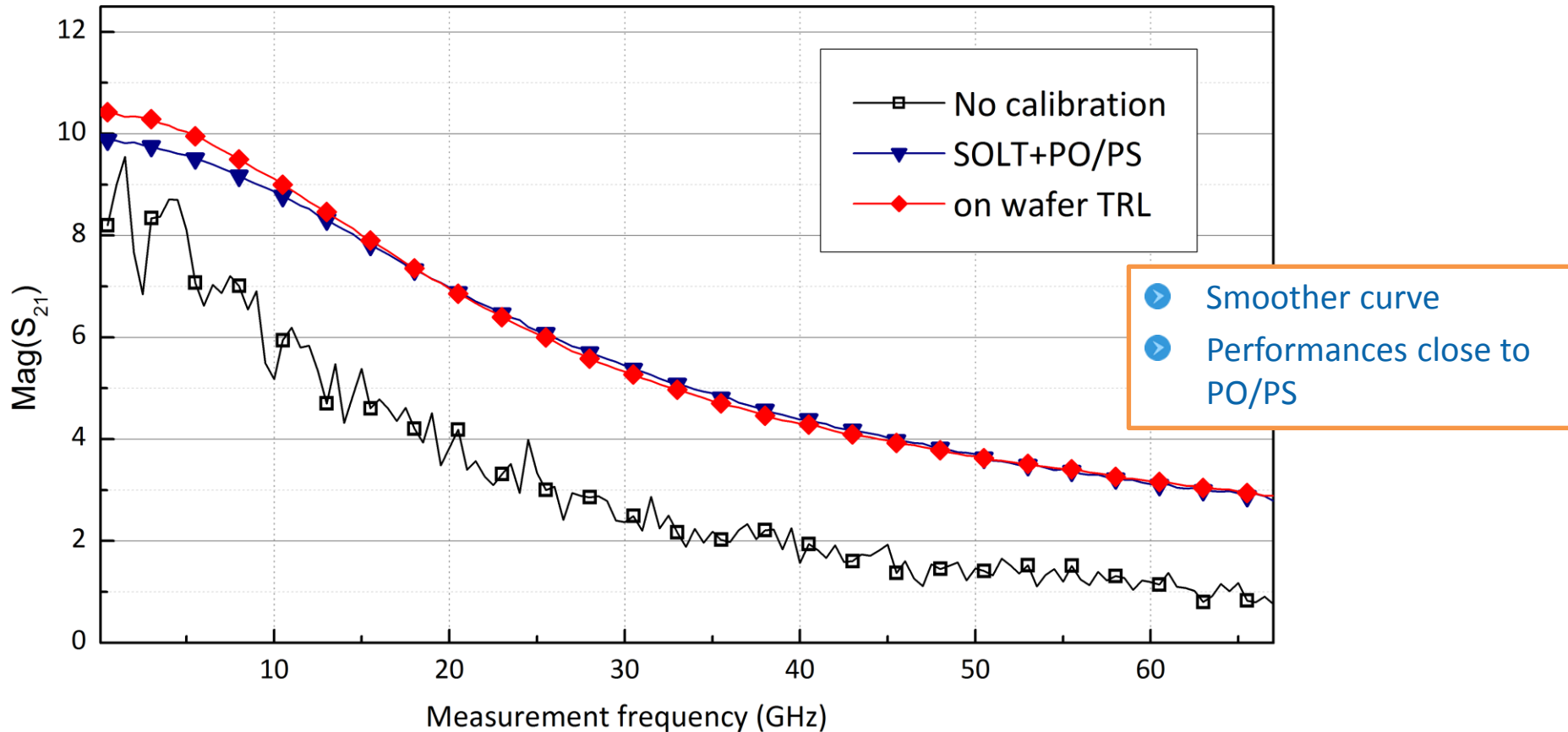


- ▶ TRL On wafer calibration (Thru, Reflect, Line)
 - ▶ Remove contribution of cable, millimeter head, RF probes, RF pads and access lines
 - ▶ Define the reference plane at the access line ends

On-wafer TRL calibration and deembedding

on-wafer TRL calibration : results

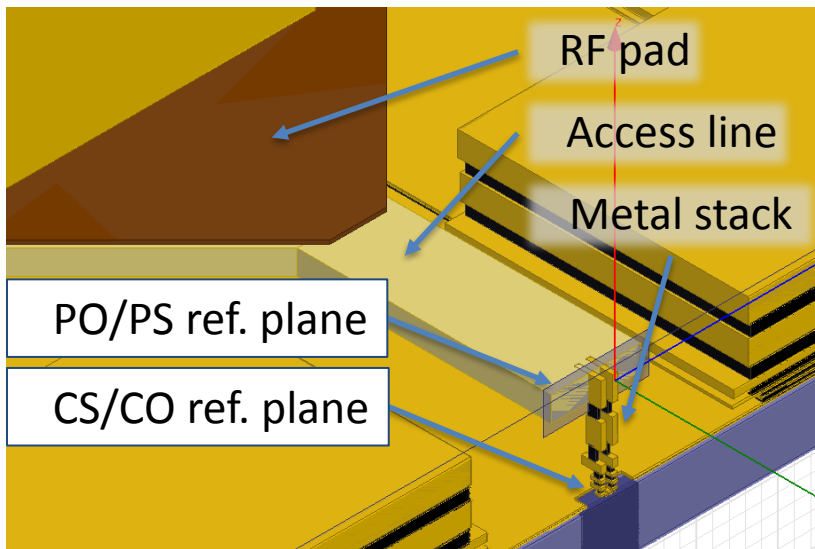
On-wafer calibration 2/4



On-wafer TRL calibration and deembedding

CS/CO deembedding

On-wafer calibration 3/4

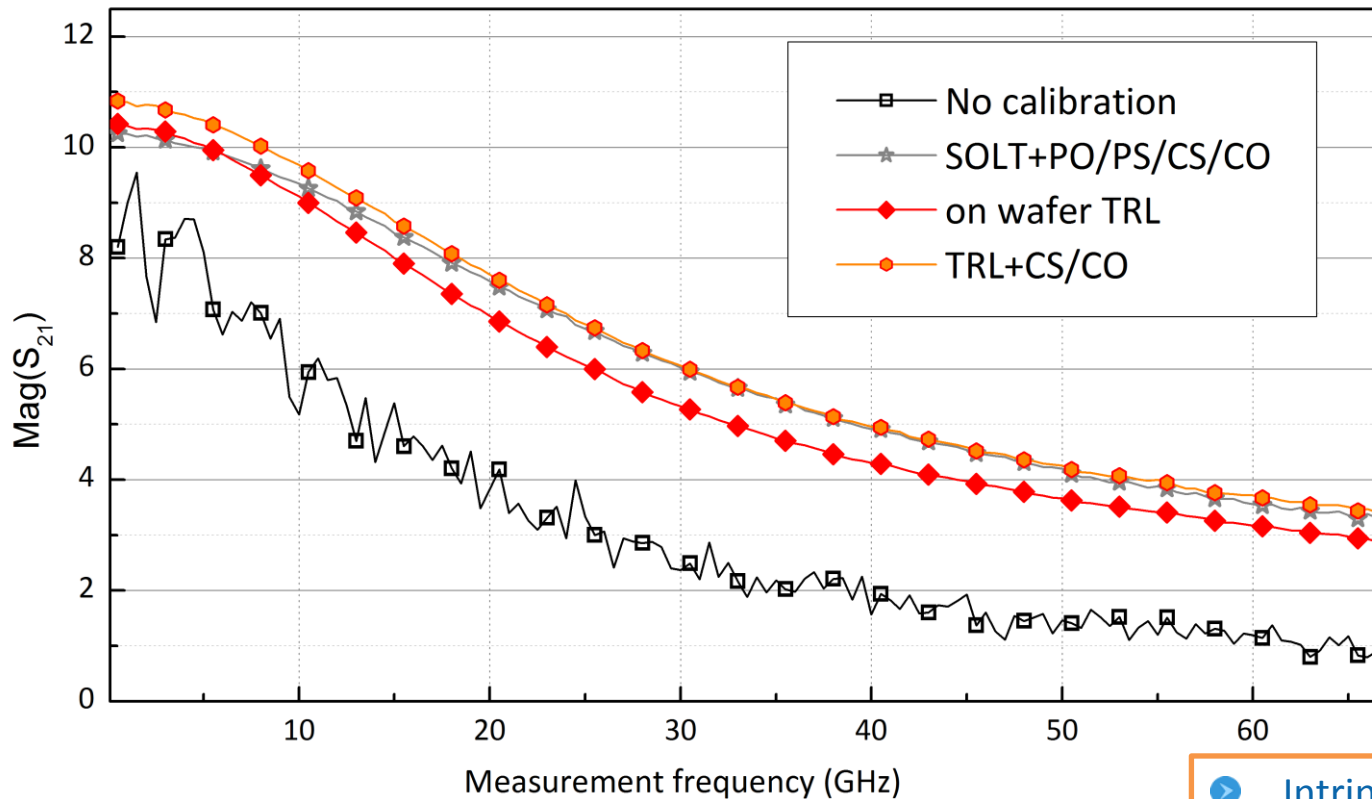


- Deembedding Complete-open and Complete-short correction (CS/CO)
 - Remove parasitic of metal stack
 - Reference plane → DUT contact

On-wafer TRL calibration and deembedding

CS/CO deembedding : results

On-wafer calibration 4/4



➤ Intrinsic component
➤ Less steps, less standards

State Of the Art methods

To sum up

➤ Off wafer SOLT calibration and 4 steps deembedding

Pro	Cons
Wide Band	Many standards → Complex procedure
Same width standards → No probes manipulation required	Off wafer → Deembedding necessary

➤ On wafer TRL calibration and 2 steps standards

Pro	Cons
Less standards → less contact error	Use more silicon area
On wafer → Same environment as measurement	Line length is longer → Environment alteration

Outline

I. Context

II. State of the Art of calibration and deembedding

III. On-wafer calibration improvements

Meander Line

3D-TRL

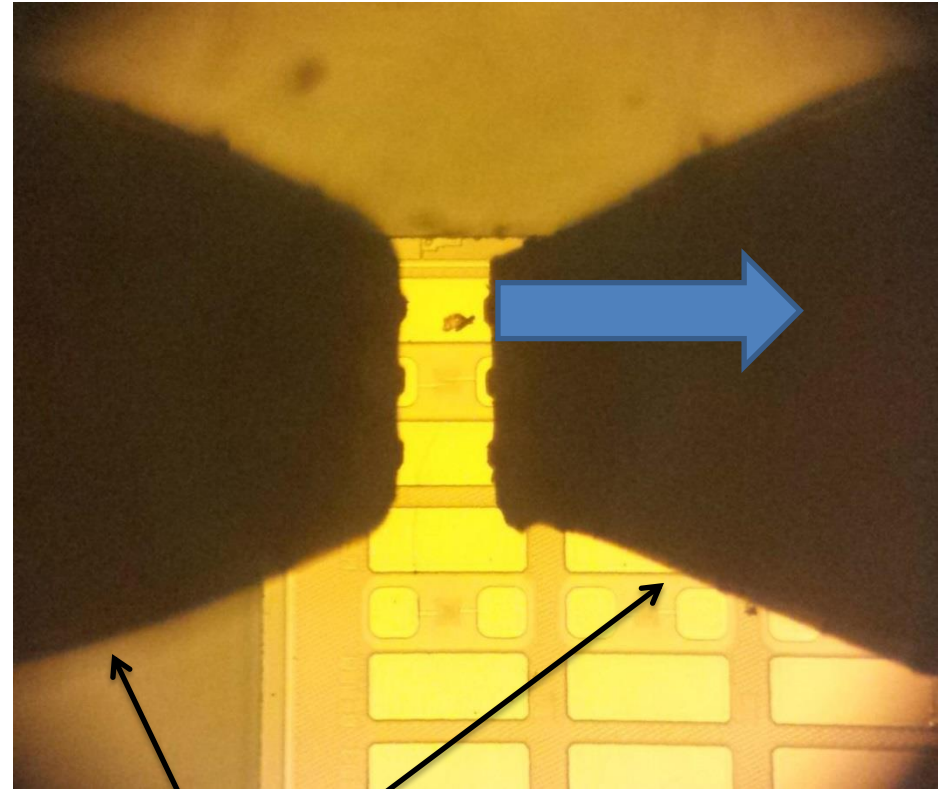
IV. Beyond 100GHz

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Probe movement during calibration

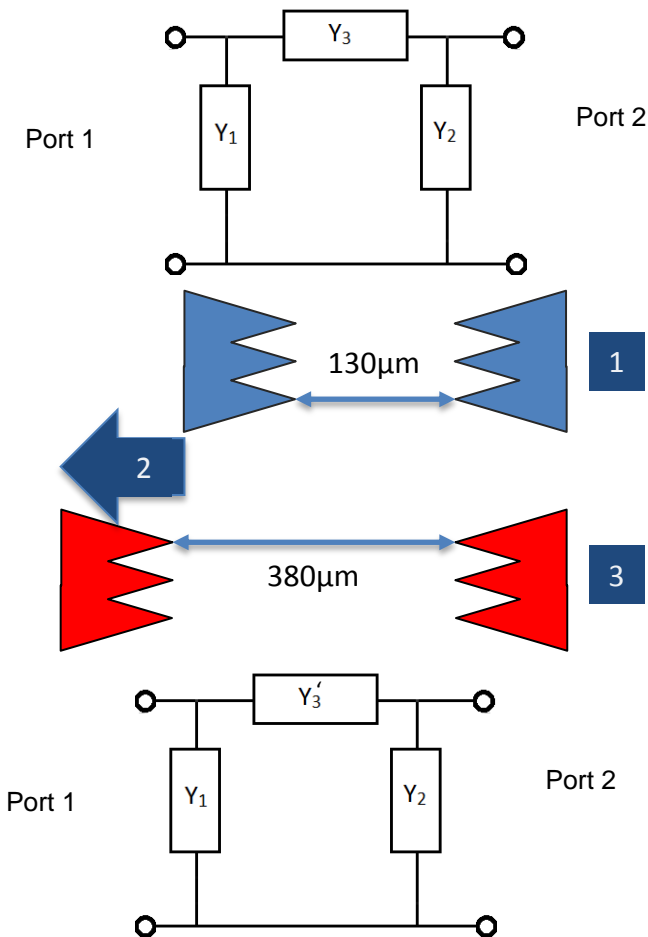
Probe movement 1/3

- ▶ The Line is longer than the other standard
 - ▶ At least one probe needs to be moved
 - ▶ The RF signal path may be altered



RF probes

Probe movement during calibration



1 Measurement of the “probe in air”
(distance between probes : 130 μ m)

2 Movement of the left probes

3 Measurement of the “probe in air”
(distance between probes : 380 μ m)

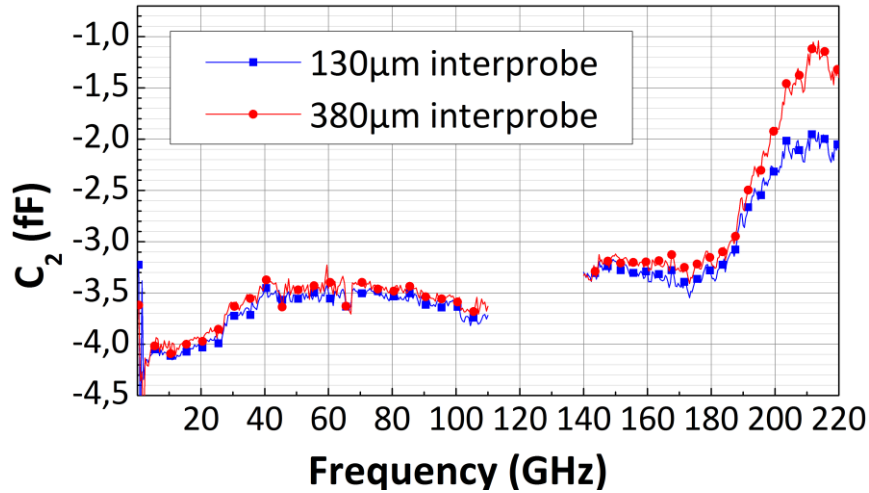
4 Comparison of the probe impedance
before and after the probe movement

M Potéreau, C Raya, “Limitations of on-wafer calibration and deembedding methods in the sub-THz range”, JCC, vol1, n°6, p25-29, nov13

Probe movement during calibration

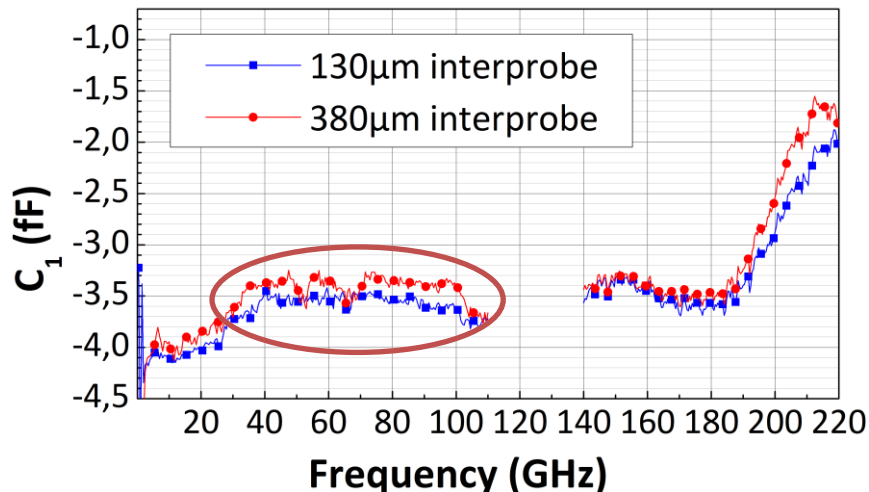
Experimentation results : Probes capacitance

Probe movement 3/3



Probe not moved between the two measurements.

No significant modification under 110GHz
Above 190GHz, not clear so far



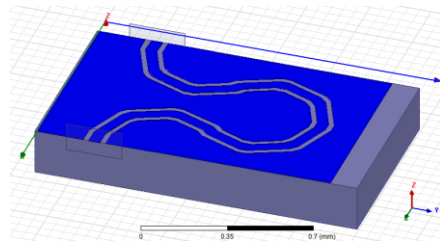
Probe moved between the two measurements.

Higher modification under 110GHz (10%)
Above 190GHz, not clear so far

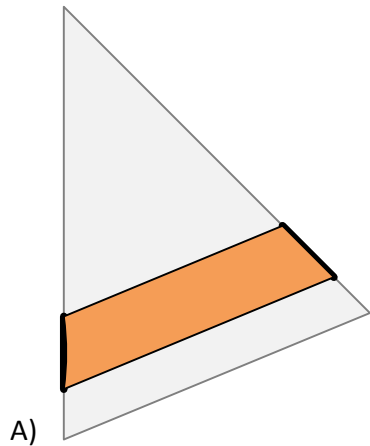
Description of the new standards

TRL with meander lines method

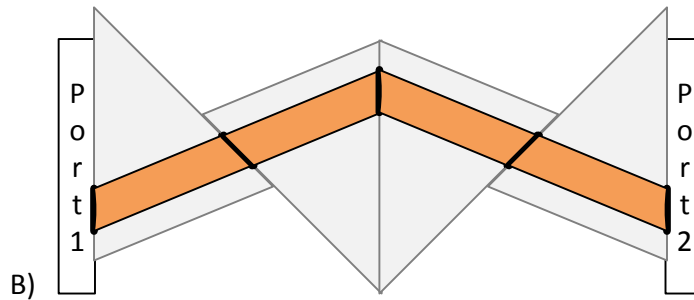
- ▶ Based on “on-wafer” TRL calibration.
 - ▶ LINE and THRU standards are made from patterns lined-up.
 - ▶ REFLECT standard is remained unchanged.



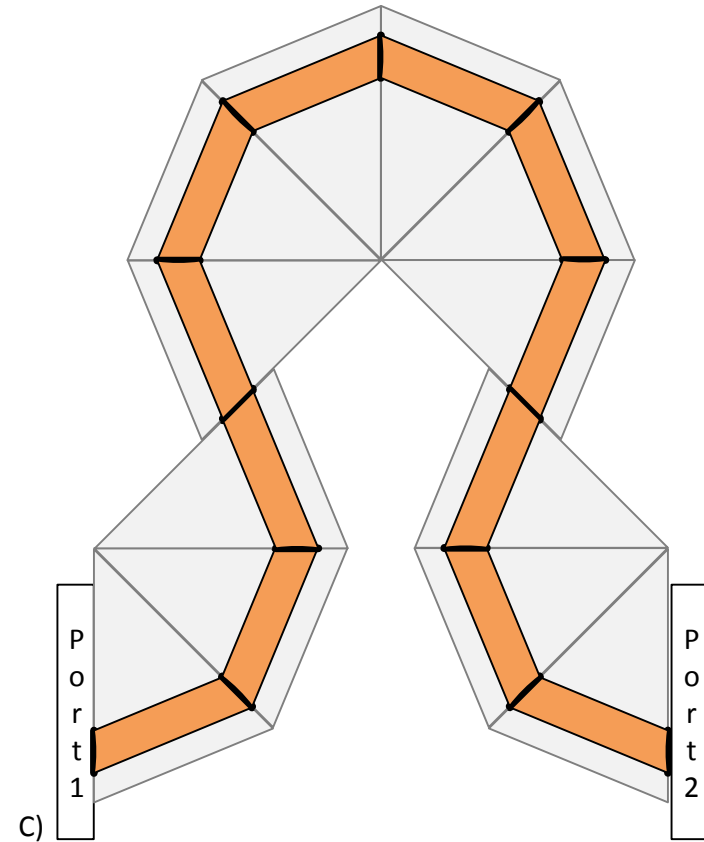
HFSS modelling



A)



B)

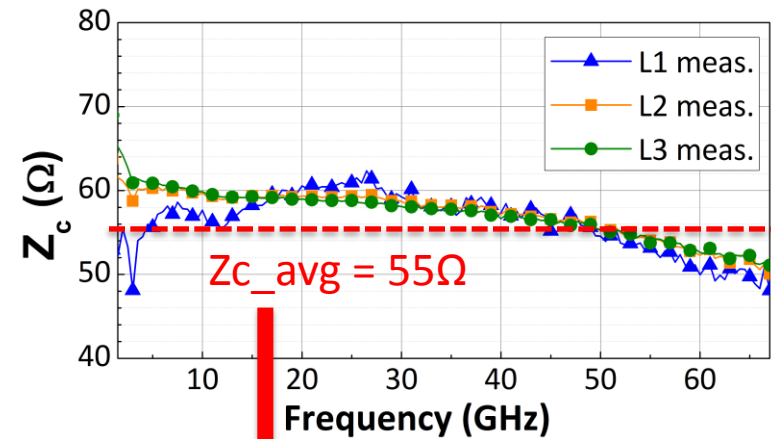
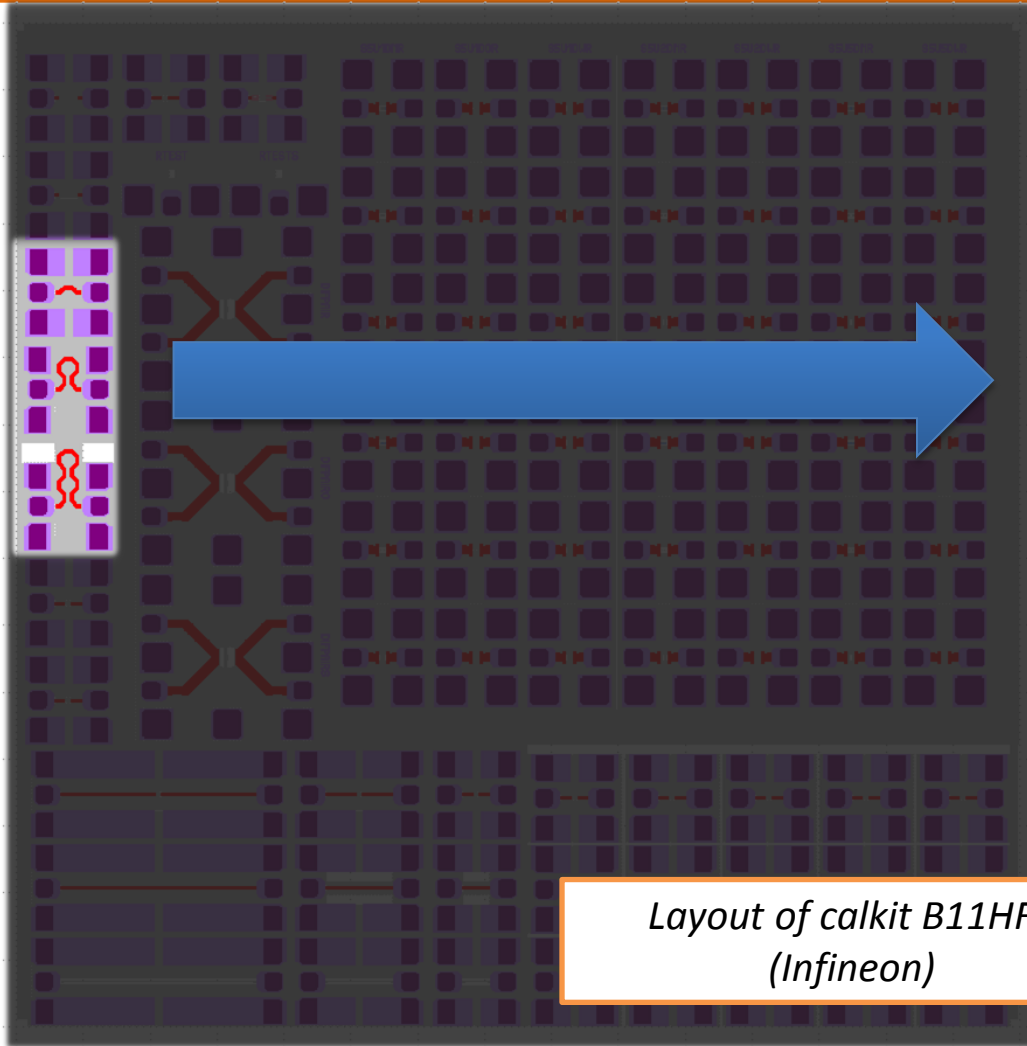


C)

Patented method

Implementation

Layout for B11HFC (Infineon)



Correction with 50Ω match

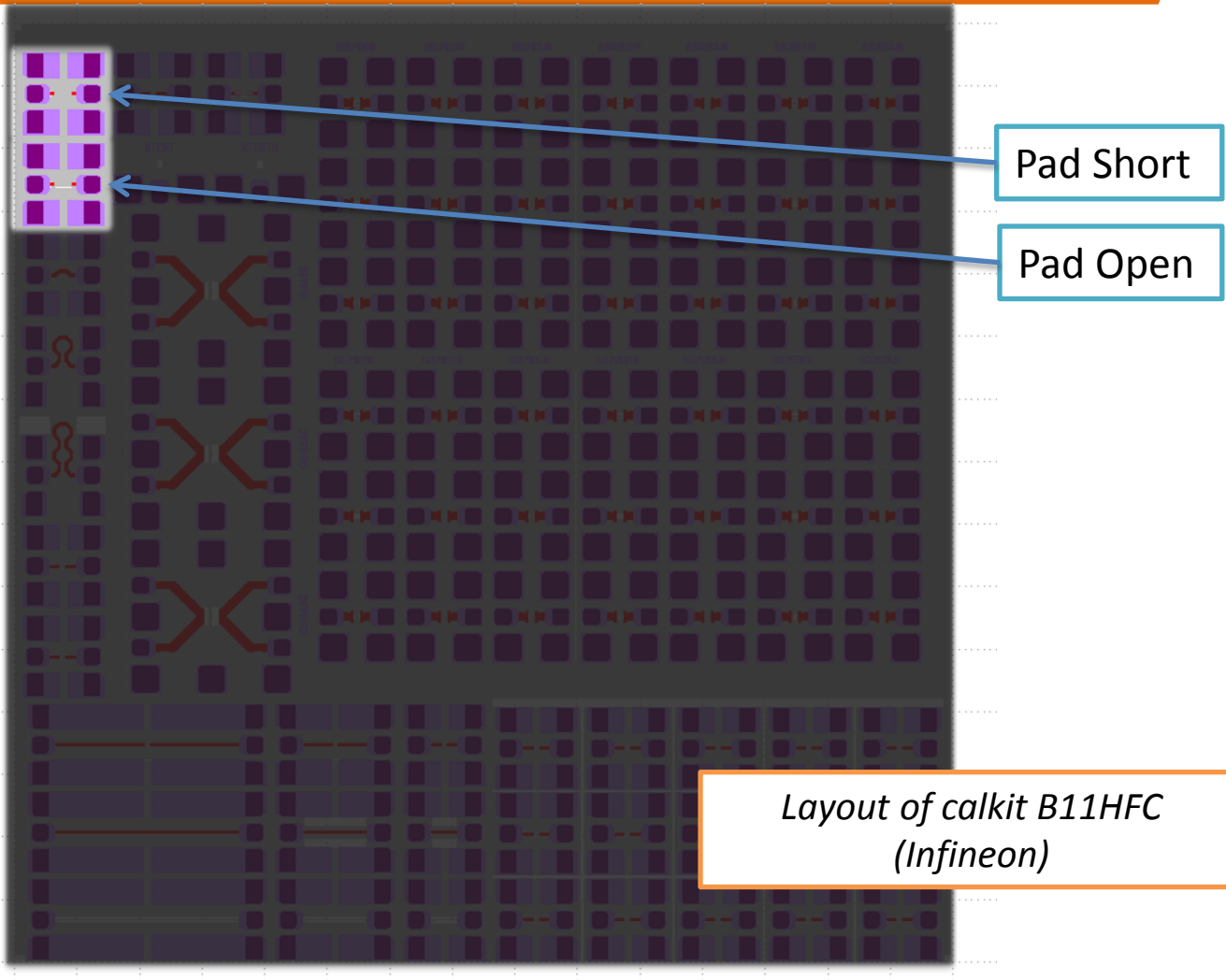
Experimentation : setup and results

- Comparison between three methods :
 - SOLT+PO/PS
 - TRL with straight lines
 - TRL with meander lines
- The reference plane is defined at top metal for all methods
- Measurement of a HBT from Infineon B11HFC (emitter window : $5 \times 0.16 \mu\text{m}^2$)
 - Transit frequency f_T
 - Base emitter capacitance C_{BE}
 - Base Collector capacitance C_{BC}

Experimentation : setup and results

Structures used in the deembedding PO/PS

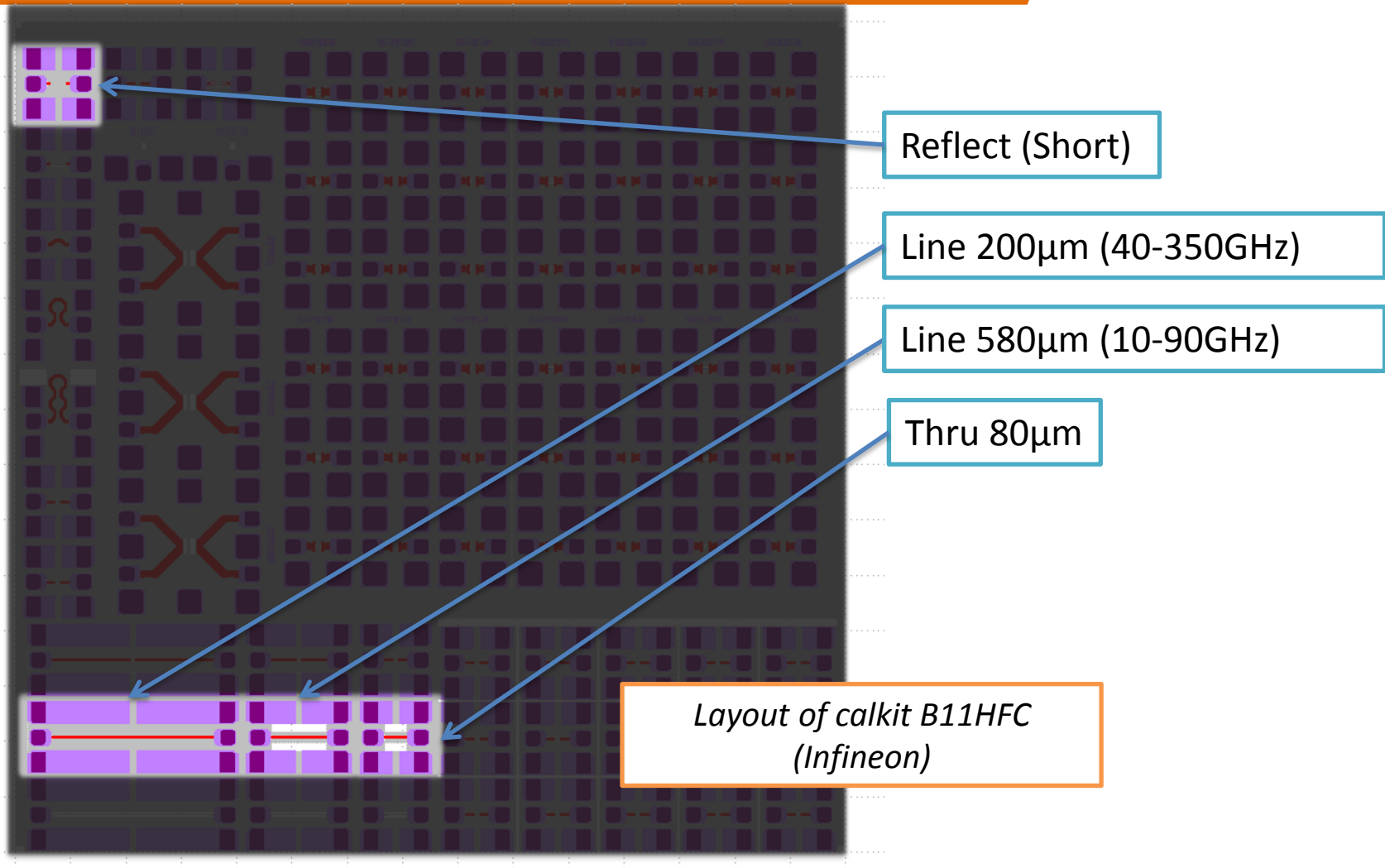
Experimentation 2/3



Experimentation : setup and results

Structures used in the TRL using straight lines

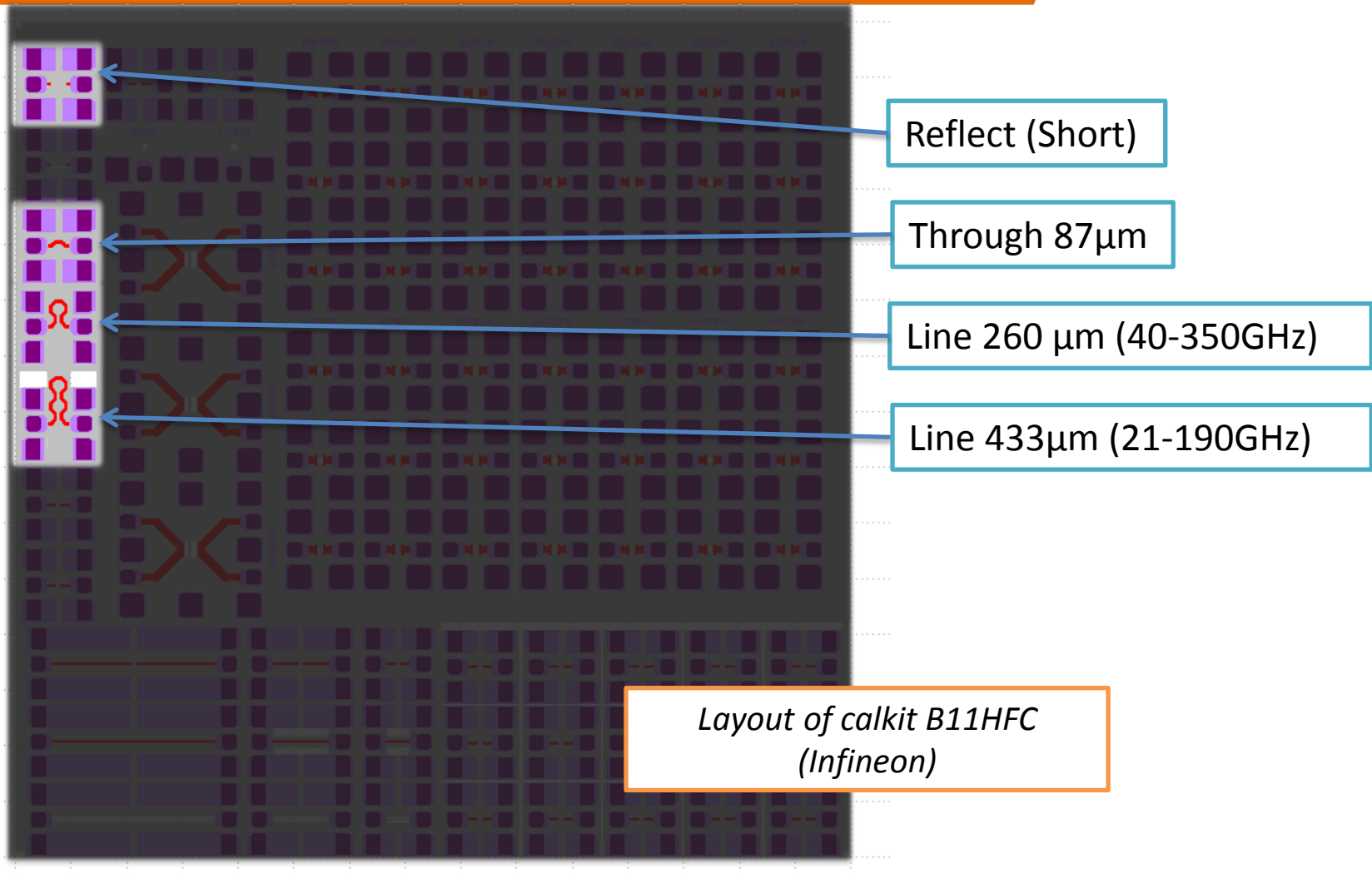
Experimentation 2/3



Experimentation : setup and results

Structures used in the TRL using meander lines

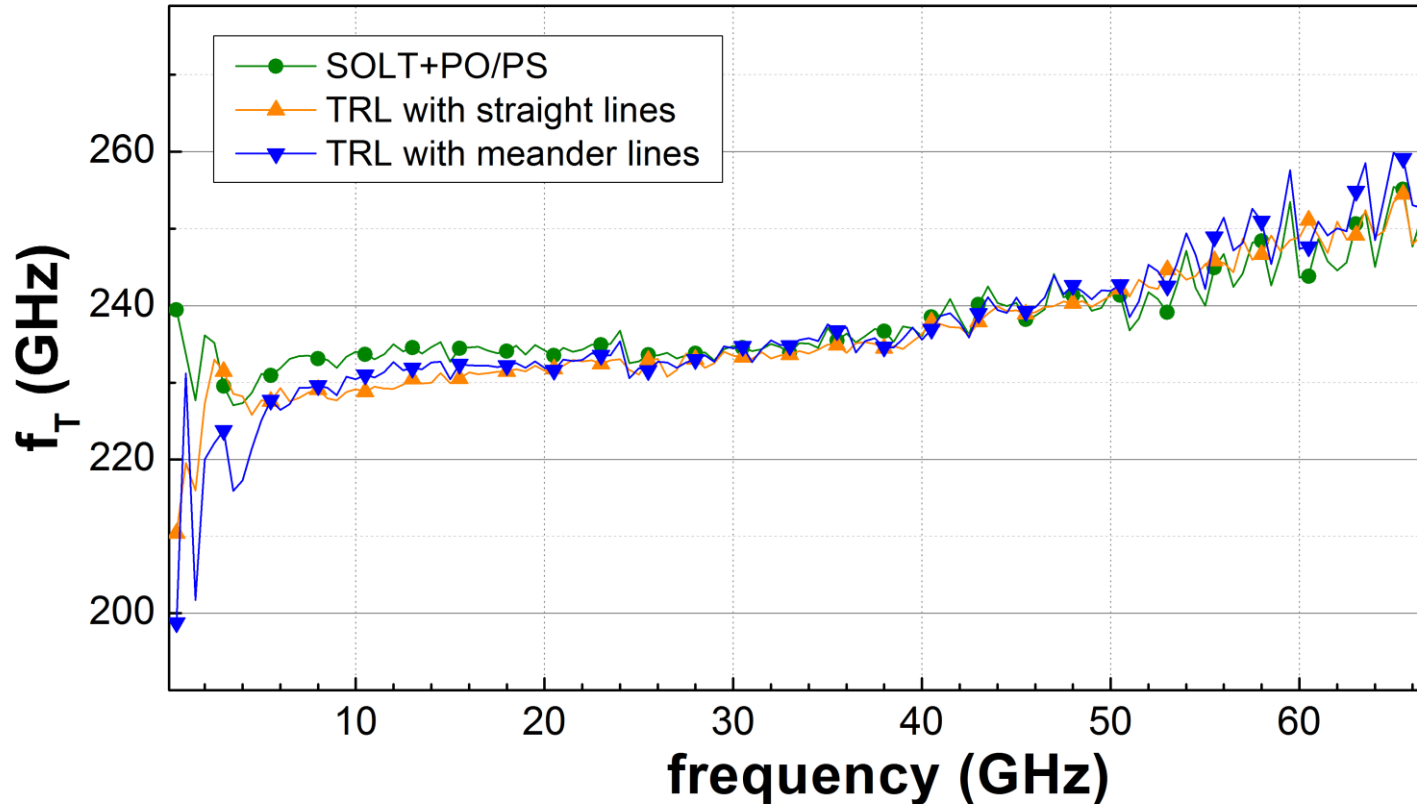
Experimentation 2/3



Experimentation : setup and results

Results : f_T

Experimentation 3/3



- ▶ The three methods give very close results.

Contribution à la caractérisation de composants sub-terahertz

Outline

I. Context

II. State of the Art of calibration and deembedding

III. Issues and proposed improvements

Meander Lines

3D-TRL

IV. Beyond 100GHz

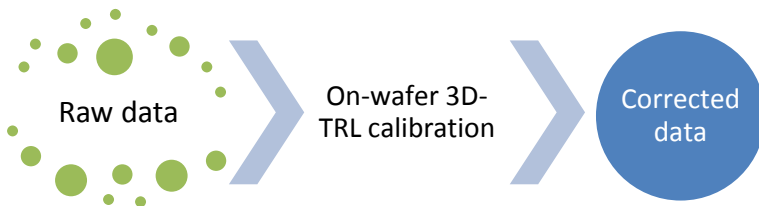
V. Conclusion

Description of the new standards

3D-TRL method

3D-TRL method 1/3

- Based on “on-wafer” TRL calibration
- LINE and THRU standards are altered to take into account the metal stack

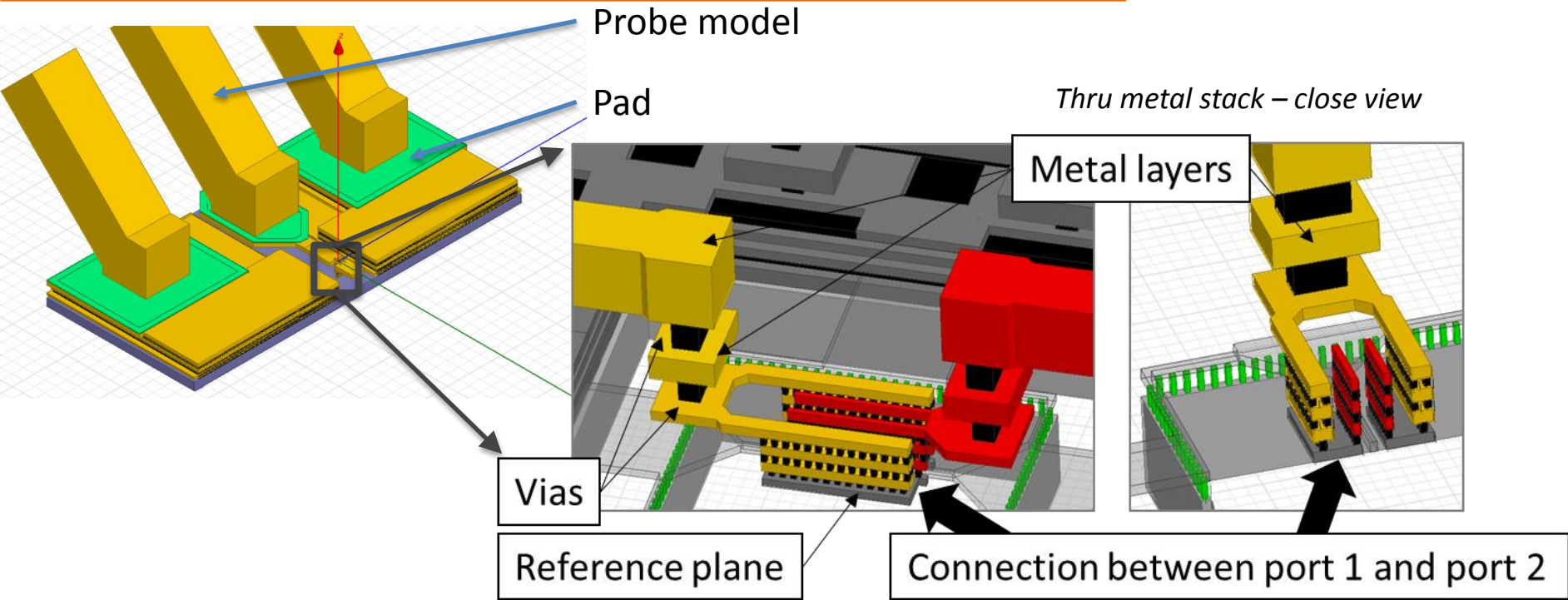


Reference plane defined at DUT
access in **1 step**

Description of the new standards

THRU modification

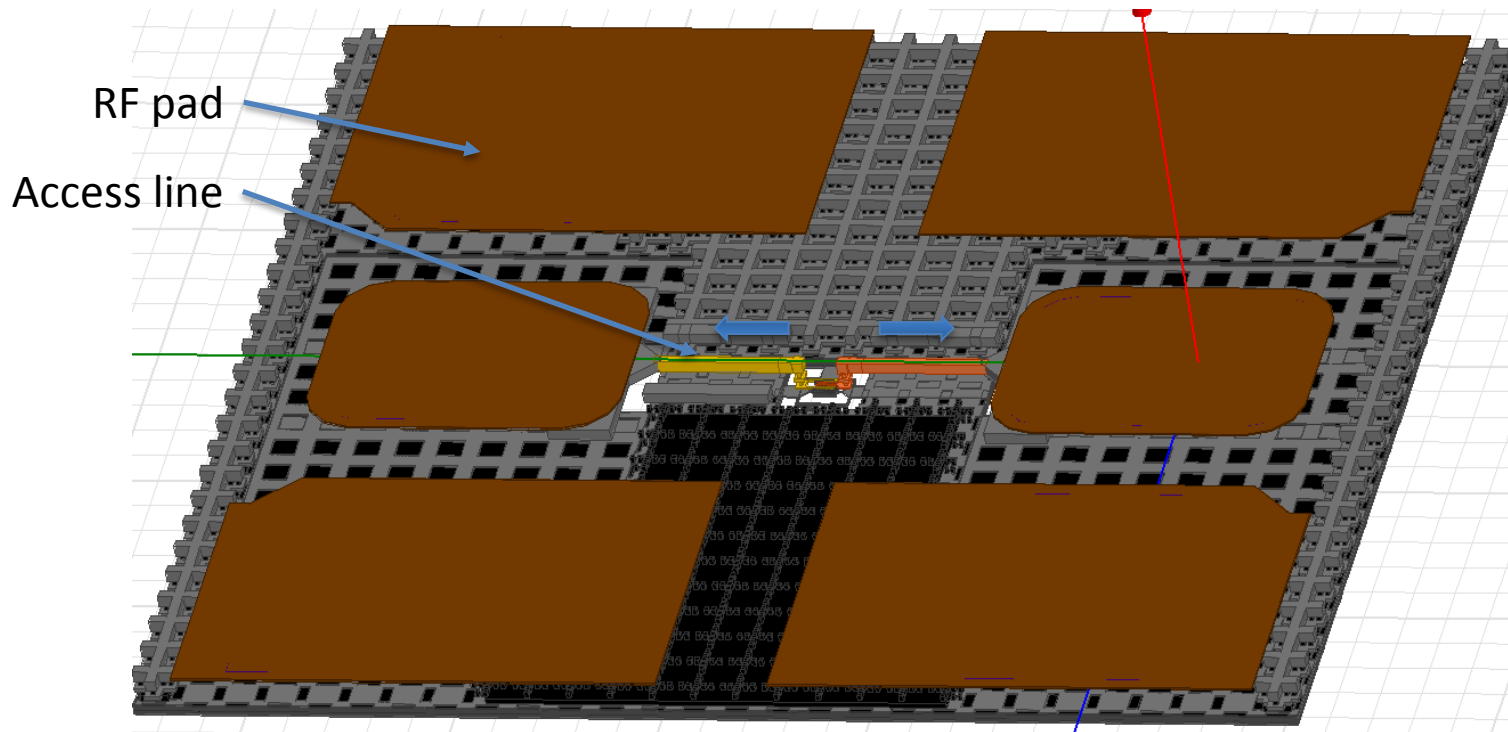
3D-TRL method 2/3



- Based on the component structure
 - Component is removed
 - Port 1 and port 2 are connected on bottom metal layer

Description of the new standards

- ▶ LINE standard is based on THRU standard
 - ▶ Access lines (red and yellow) are stretched along blue arrows



Experimentation : setup and results

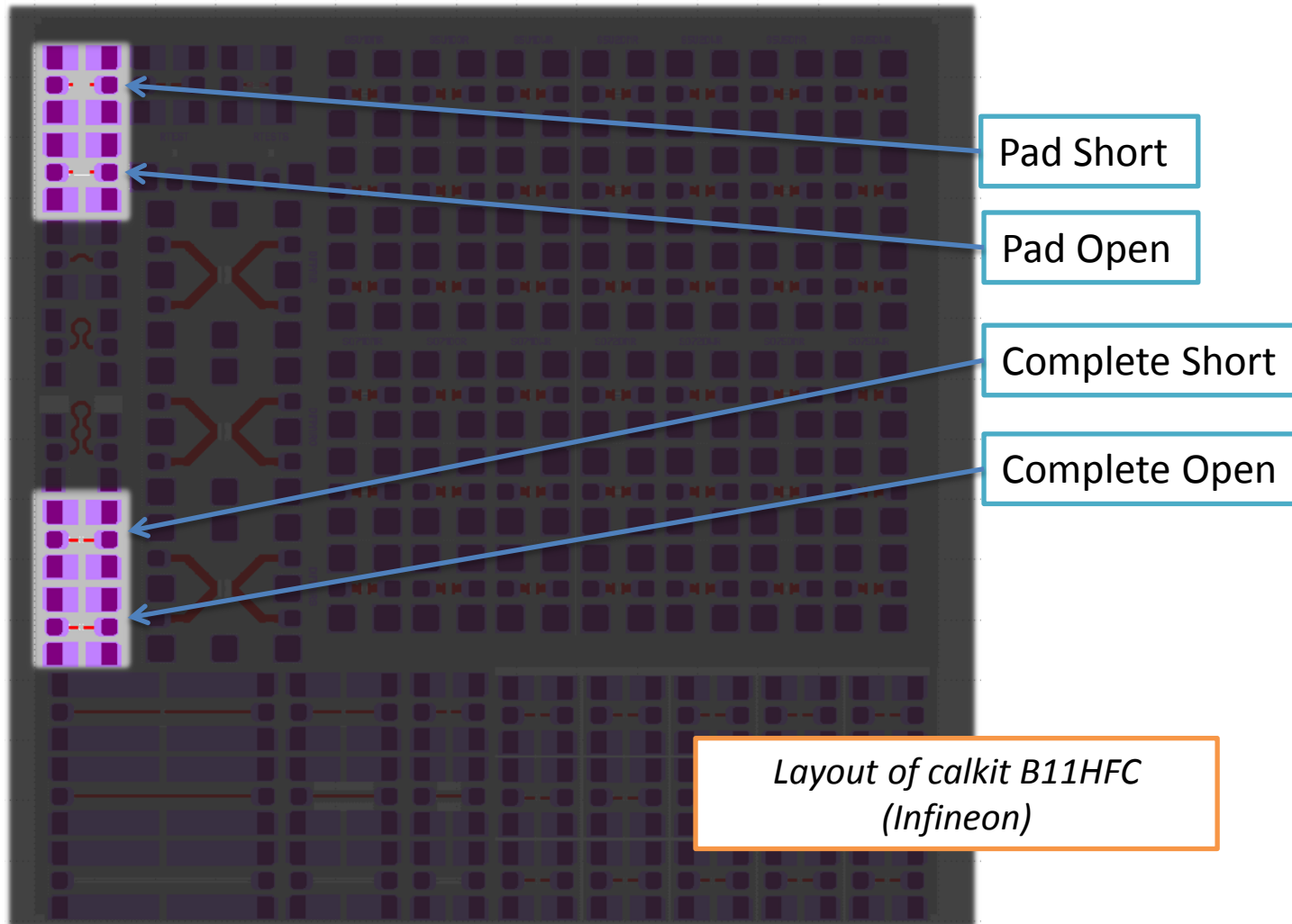
- Comparison between the three methods exposed
 - SOLT+PO/PS/CS/CO
 - TRL+CS/CO
 - 3D-TRL

- Measurement of a HBT from Infineon B11HFC (emitter window : $5 \times 0.16 \mu\text{m}$)
 - Transit frequency f_T

Experimentation : setup and results

Structures used in the deembedding PO/PS/CS/CO

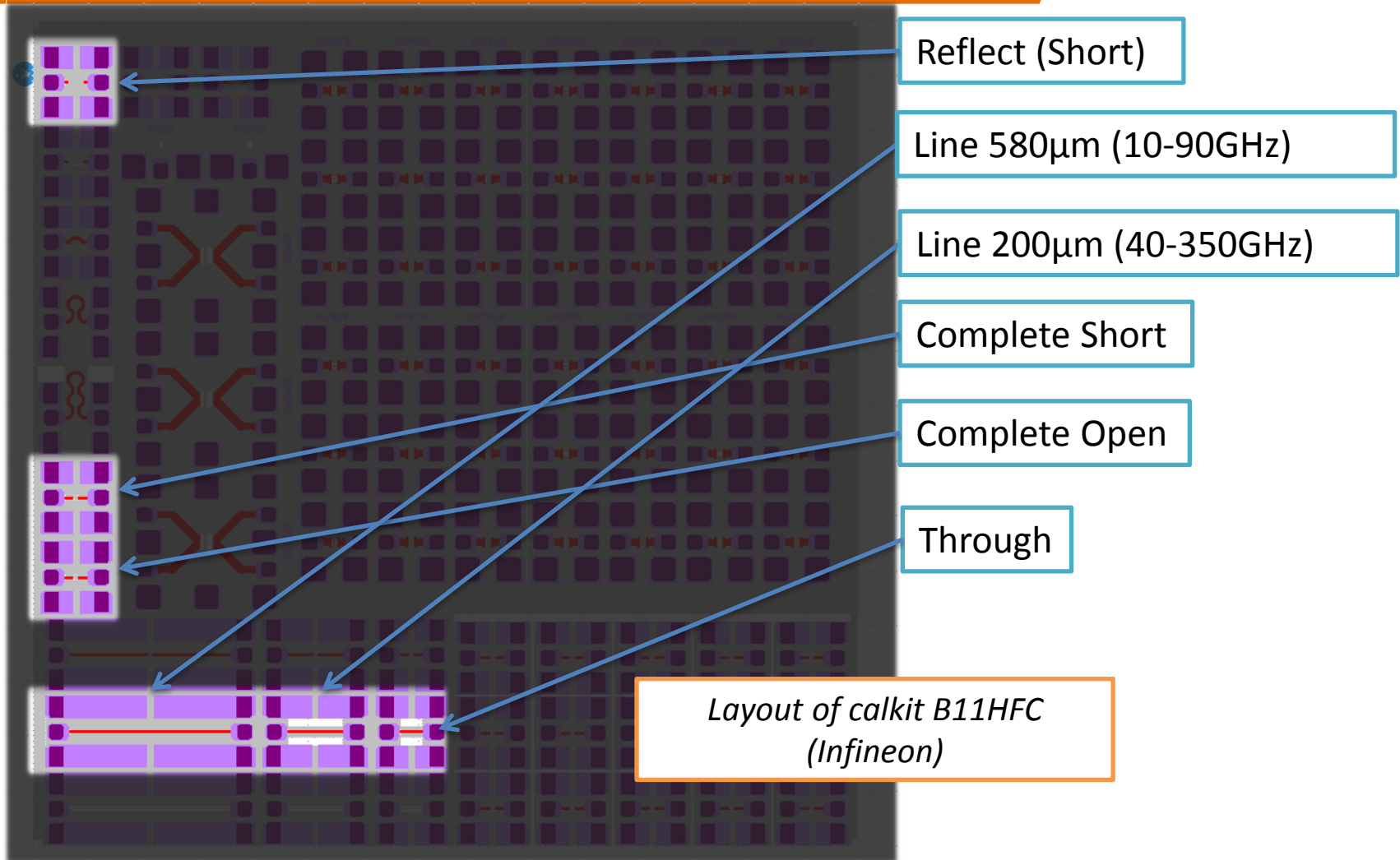
Experimentation 2/3



Experimentation : setup and results

Structures used in on-wafer TRL and 2 steps deembedding

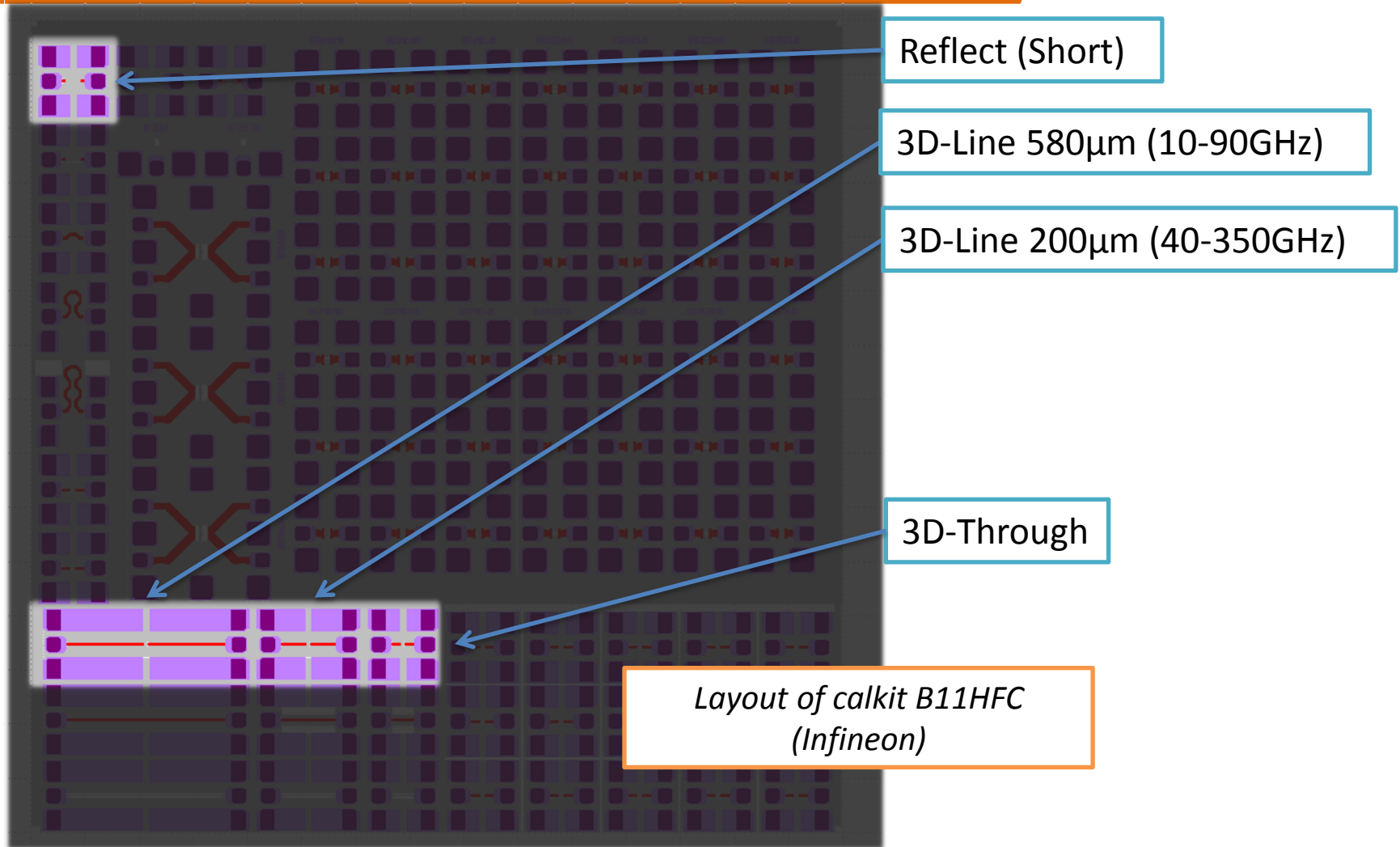
Experimentation 2/3



Experimentation : setup and results

Structures used in on-wafer 3D-TRL

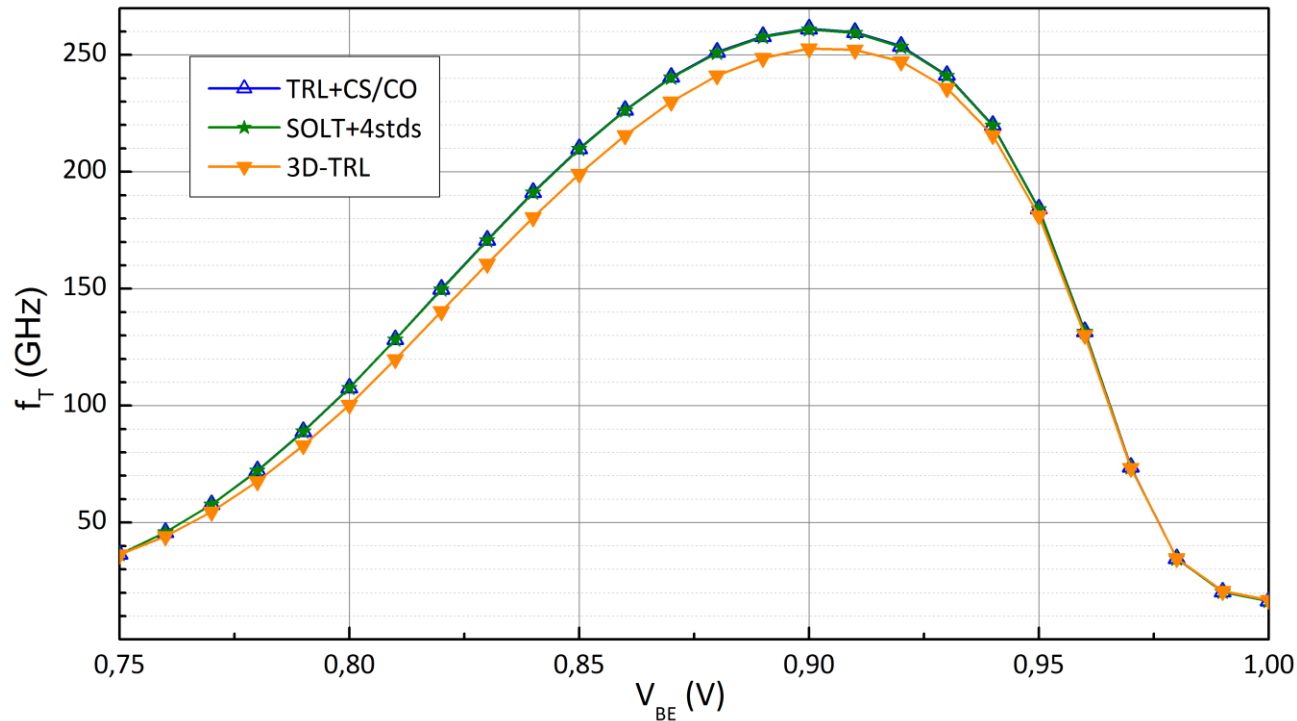
Experimentation 2/3



Experimentation : setup and results

Results : f_T

Experimentation 3/3



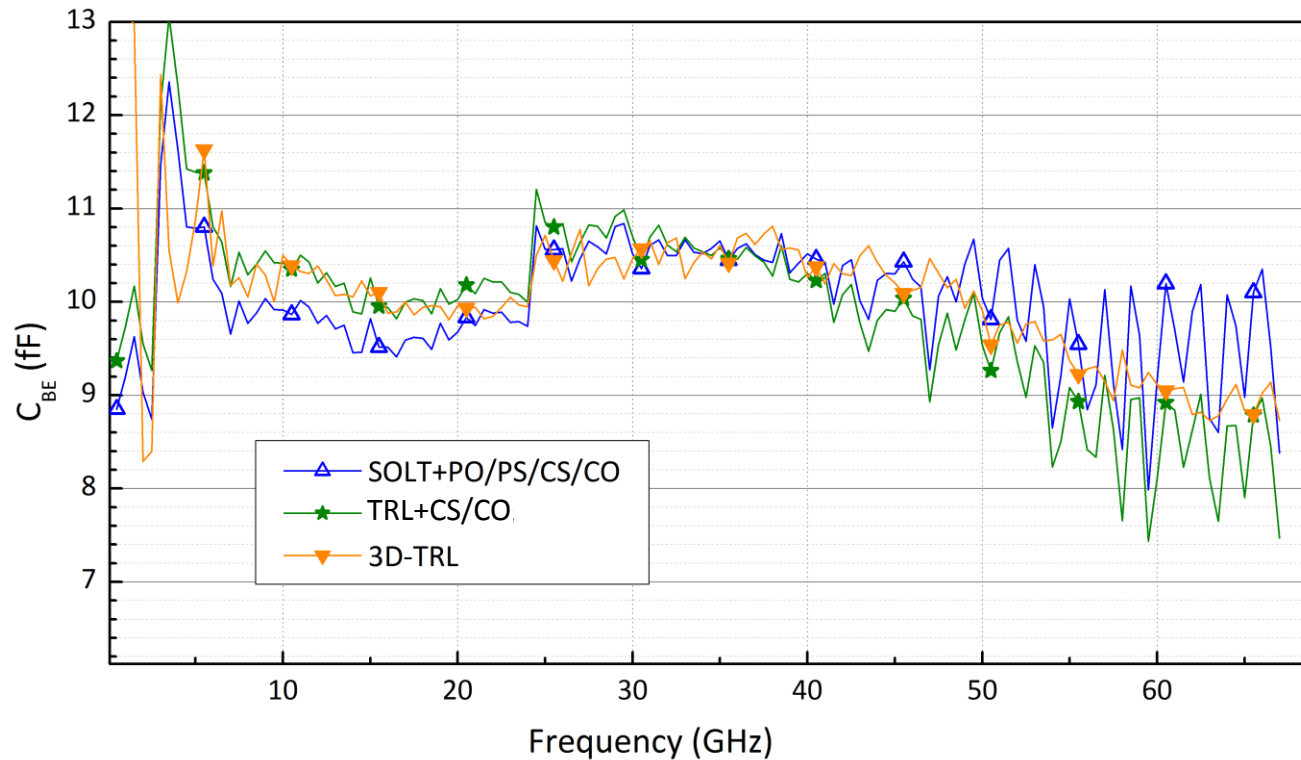
f_T versus V_{BE}
($f = 30\text{GHz}$; $V_{BC} = 0\text{V}$)

- ▶ PO/PS/CS/CO and TRL+CS/CO give same results
- ▶ 3D-TRL slightly lower
 - ▶ Remaining parasitic ?

Experimentation : setup and results

Results : C_{BE}

Experimentation 3/3



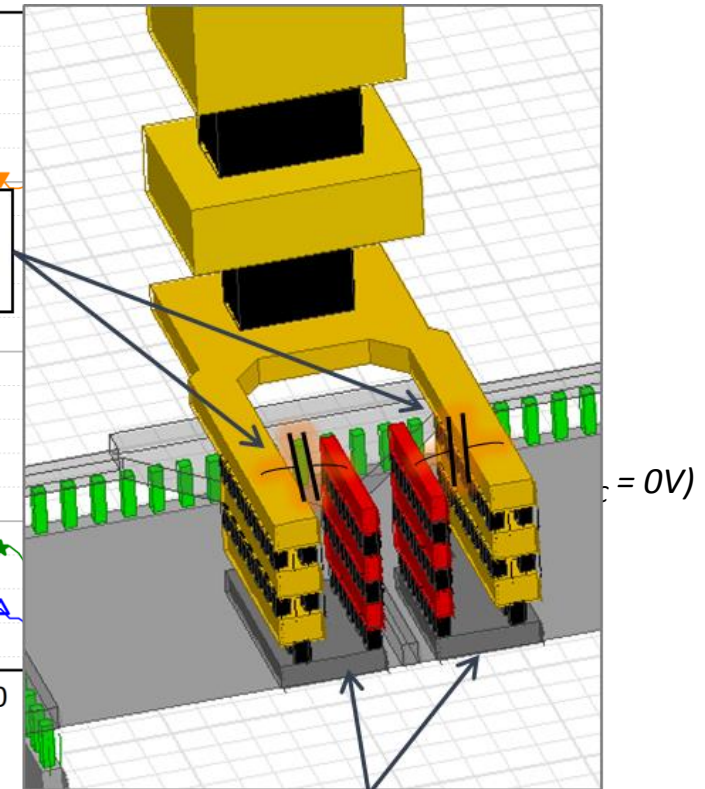
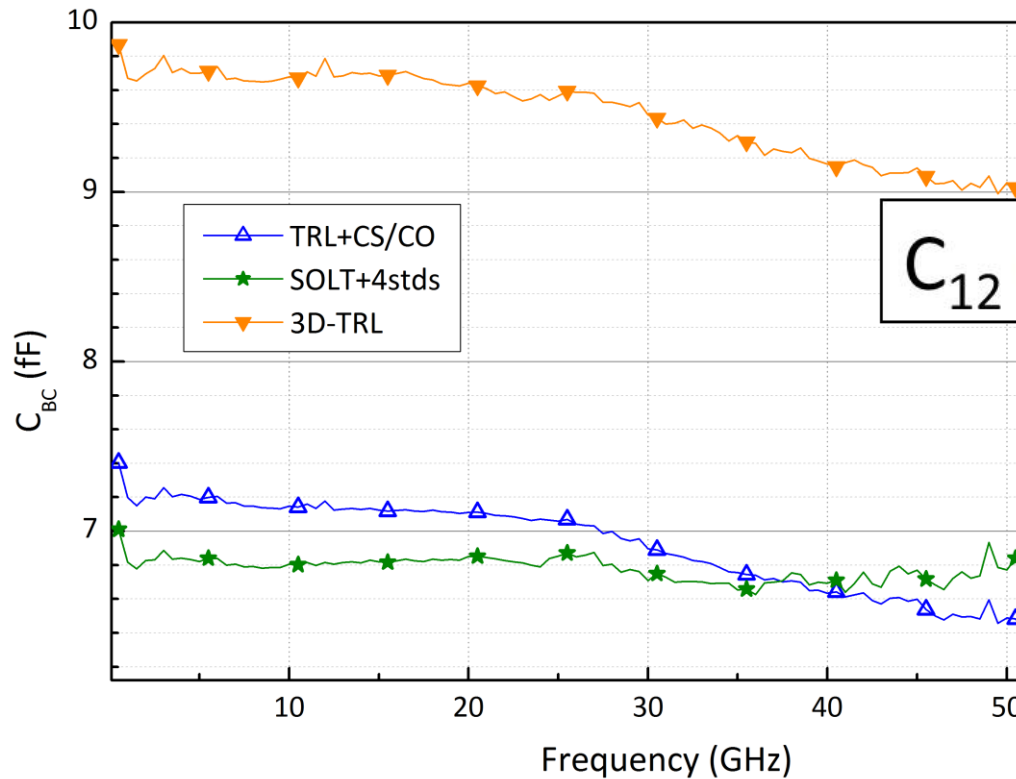
C_{BE} versus F
($V_{BE} = 0.5V$; $V_{BC} = 0V$)

- 3 methods gives same results
- C_{BE} value close to 10fF → above the 1fF limit
- 3D-TRL less noisy above 40GHz
 - less standards → less contact errors

Experimentation : setup and results

Results : C_{BC}

Experimentation 3/3



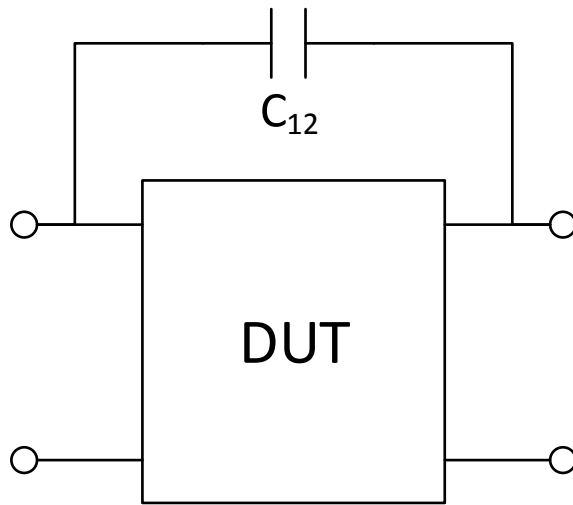
- ▶ PO/PS/CS/CO and TRL+CS/CO give similar results
- ▶ 3D-TRL higher by 2.6fF
 - ▶ Remaining error (C_{12}) → deembedding needed

Short-circuit in M1

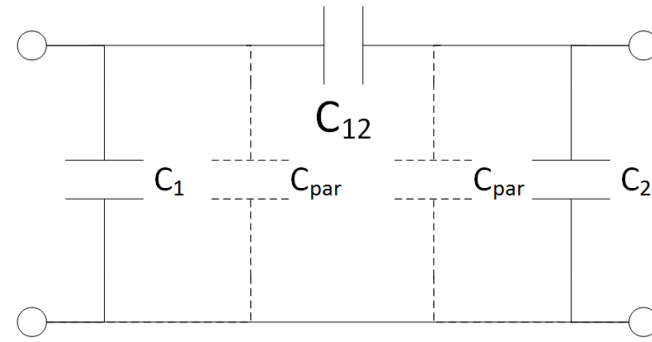
Experimentation : setup and results

Deembedding procedure : CO*

CO* deembedding 1/3



*Residual parasitic of the
3D-TRL method*



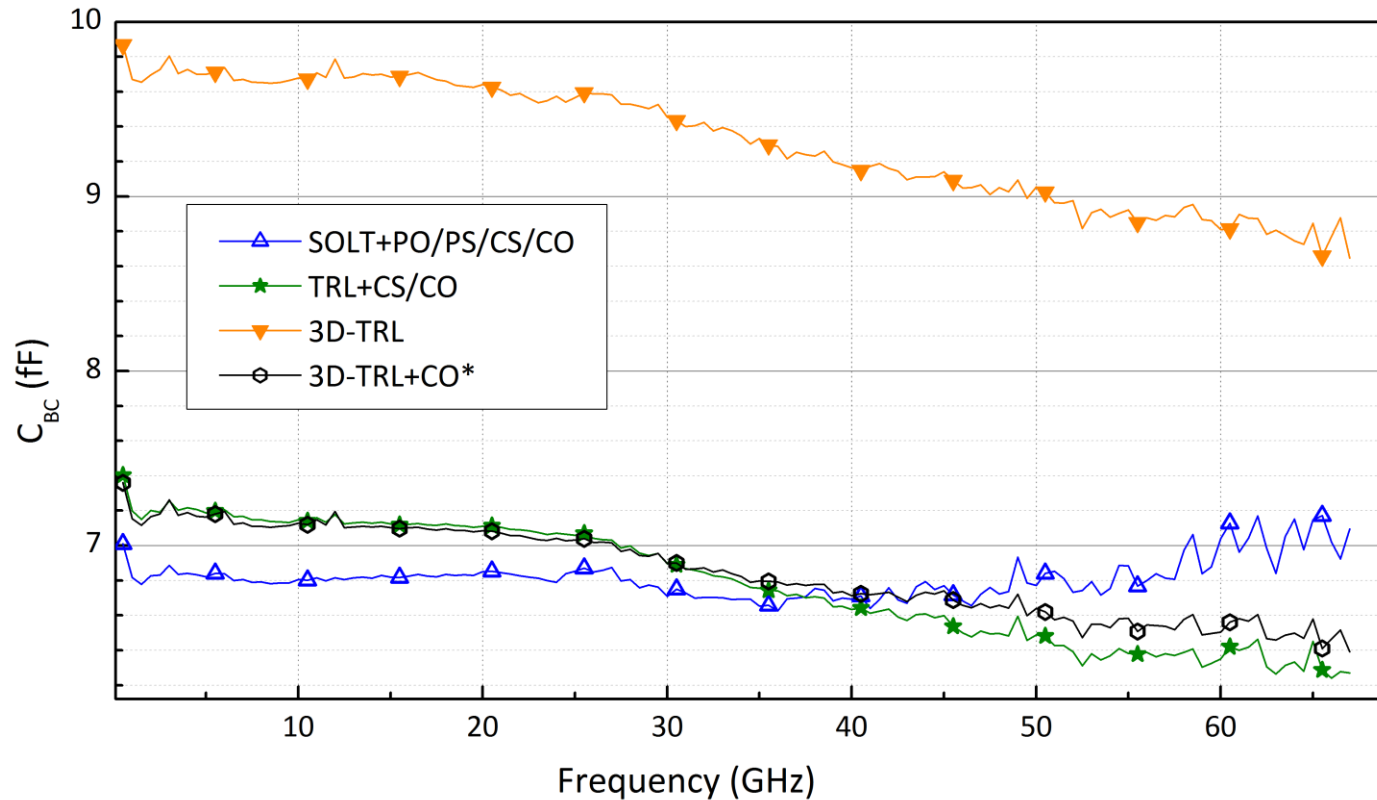
Parasitic of the complete open

- Emitter capacitance is correctly evaluated
 - The port admittance parasitics are removed
- Collector Capacitance is not correctly evaluated
 - Residual capacitance between the port
- Using CO, C_{12} is removed from the DUT

Experimentation : setup and results

Results : C_{BC}

CO* deembedding 2/3

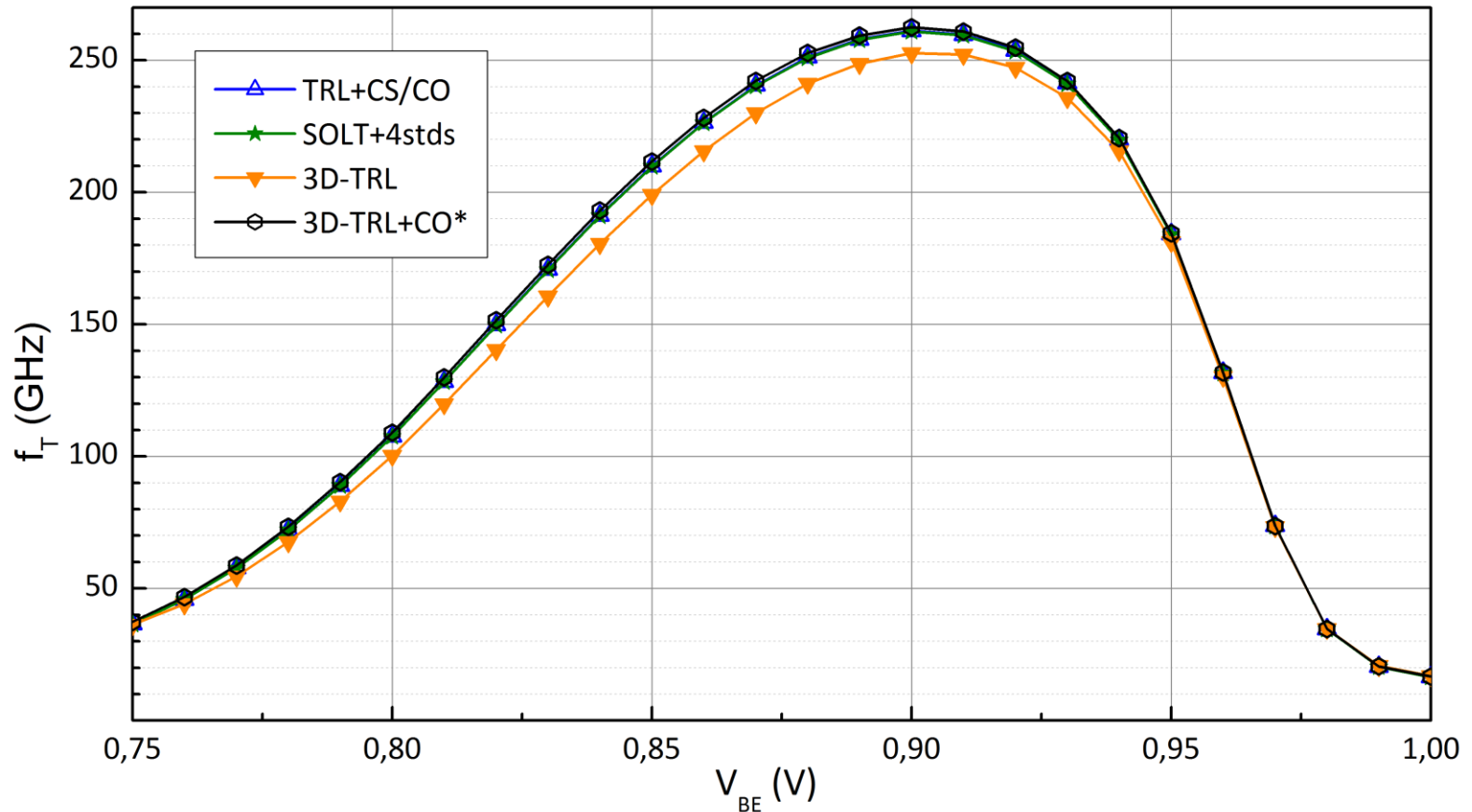


▶ With C_{12} removed, the three methods give similar results

Experimentation : setup and results

Results : f_T

CO* deembedding 3/3



➤ Same results for the f_T

Contribution à la caractérisation de composants sub-terahertz

Outline

I. Context

II. State of the Art of calibration and deembedding

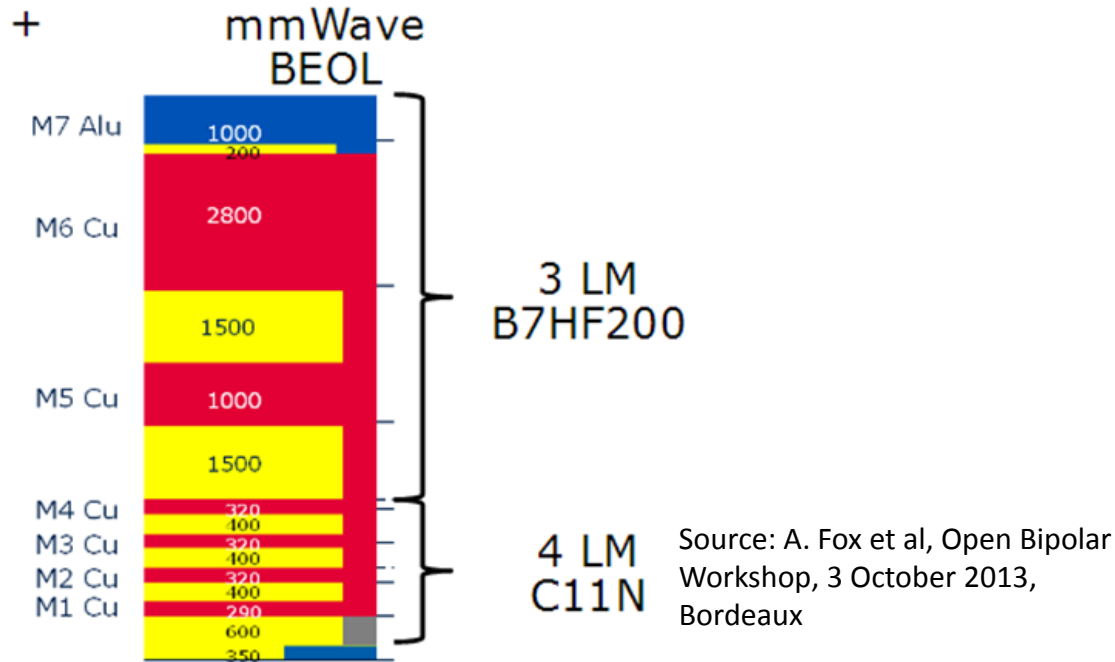
III. On-wafer calibration improvements

IV. Beyond 100GHz

V. Conclusion

And what about beyond 100GHz ?

Test-structures Back-End-Of-Line



Schematic view of the BEOL of INFINEON's B7HF200 process

Beyond 100GHz: Bench-marking of EM-simulation

Double check TRL calibration: method -> EM simulation

Beyond 100GHz: Bench-marking of EM-simulation

Double check TRL calibration: results

Beyond 100GHz: EM-simulation vs measurement

Characterization of Passive elements and comparison to EM simulation

Beyond 100GHz: Characterization of devices up to 500 GHz

Transistor measurements: f_T and f_{max}

Beyond 100GHz: Characterization of devices up to 500 GHz

Transistor measurements: S-Parameter

Beyond 100GHz: Measurements uncertainties

What about contacts?

Beyond 100GHz: Measurements uncertainties

What about Probe tip positioning?

Beyond 100GHz: Measurements uncertainties

What about Probe tip positioning?

Beyond 100GHz: Measurements uncertainties

What about Probe coupling with underlying surface ?

Beyond 100GHz: Measurements uncertainties

What about SOLT Calibration on ISS compared to on wafer TRL calibration?

Contribution à la caractérisation de composants sub-terahertz

Outline

- I. Context
- II. State of the Art of calibration and deembedding
- III. On-wafer calibration improvements
- IV. Beyond 100GHz
- V. Conclusion

Conclusion

- **State of the Art of calibration and deembedding techniques**
 - Presentation of both off-wafer and on-wafer techniques
 - Highlights of advantages and drawbacks of both of them
- **Presentation of new meander lines structures**
 - News structures give results close to the SoA
 - No manipulation required during calibration → easier calibration, automative probe station
- **Presentation of new 3D-TRL structures**
 - New structures → less noisy results, less test structures are needed
 - More straightforward
- **Measurement beyond 100GHz**
 - Reliable measurements: to be benchmarked through EM-simulation
 - On-wafer TRL calibration: method of choice beyond 100GHz
 - Investigation of probe positioning and probe coupling

Contribution à la caractérisation de composants sub-terahertz

Outline



VI. Thanks

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- **Journal publications**

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- M. Potereau, C. Raya, M. De Matos, S. Fregonese, A. Curutchet, M. Zhang, B. Ardouin, T. Zimmer “Limitations of on-wafer calibration and de-embedding methods in the sub-THz range”, – *Journal of Computer and Communications (JCC)*, pp 25-29, 2013
- Arnaud Curutchet, Anthony Ghiotto, Manuel Potéreau, Magali De Matos, Sébastien Fregonese, Eric Kerhervé, and Thomas Zimmer, “On the Development of a Novel High VSWR Programmable Impedance Tuner”, spécial issue du journal d’EUMA, *International Journal of Microwave and Wireless Technologies*, Volume 8, Issue 4-5, June 2016, pp. 723-730

- **Conferences (invited)**

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- Sebastien Fregonese, Rosario D’Esposito, Cristell Maneux, Thomas Zimmer, « Substrate coupling effect in BiCMOS technology for millimeter wave application », *Special Session NEWCAS 2015 "On-chip measurements for characterization, testing, and calibration of analog front-ends and mmW devices "*, June 7-10, 2015, Grenoble, France

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- A. Curutchet, A. Ghiotto, M. Potéreau, M. De Matos, S. Fregonese, E. Kerhervé, T. Zimmer, « Early Demonstration of a High VSWR Microwave Coaxial Programmable Impedance Tuner with Coaxial Slugs », European Microwave Integrated Circuits Conference (EuMIC), September 7-8, 2015, Paris, France
- Manuel Potéreau, Arnaud Curutchet, Rosario D’Esposito, Sebastien Fregonese, Thomas Zimmer, A Test Structure Set for on-wafer 3D-TRL calibration, International Conference on Microelectronic Test Structures (ICMTS), 28th-31st March 2016, Yokohama, Japan
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