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SiC tools for reliability study

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Abstract— Understanding the failure mechanisms is essential to ensure reliability for a new technology of semiconductors. Amongst various existing tools dedicated to silicon-based devices, there is no consensual method for silicon carbide (SiC) devices. This semiconductor offers very interesting properties for power electronics in comparison with Si, but these failures are different and need to be studied. This paper will compare different methods applied to failures, focusing on lock-in thermography and micro-Raman analysis. Three devices have been evaluated, a vertical diode, a lateral diode and a MESFET.

Keywords—SiC; failure mechanism; Focus ion Beam; raman spectroscopy; Lock-in thermography

1. Introduction

Nowadays, reliability is fundamental to establish a new market tendency with SiC technology. This technology can greatly improve our electrical energy management and failure mechanism study is required to propose devices with higher performances and better robustness [1]. In this study, we will discuss about several characterization methods for failures on SiC devices: Scanning Electron Microcopy (SEM), Focus Ion Beam (FIB), active infrared thermography, micro-Raman spectroscopy, etc. Each has some pro and cons and permits to observe different phenomena. The proposed study approach is valid for all devices without packaging but we will focus in this article on a vertical diode, a lateral diode and a MESFET.

2. Diodes and MESFET SiC structures

Vertical diodes were made by Dr. Lazar at the Ampere Laboratory as part of the ISMART project. The aim was to create a thermal and fast neutron sensor [2].

Compared to a vertical PiN power diode, a doped layer of Boron (^{10}B) used for radiation measurement in the Anode metallization, was added at the interface between the Nickel-Titan-Aluminum layer and SiC P^+ (Fig.1). A leakage current of 10 pA for a voltage of -5V was measured. In forward bias, the threshold voltage was around 2.8V and the internal resistance approximately equaled to $R_{\text{on}}=20\text{m}\Omega$.

MESFETs and lateral Schottky diodes (Fig.2) are contained on the same wafer, originated from the CNM Laboratory and were designed for an easy adaptation to drive power transistor. MESFETs characteristics were ranging from 0 to 15V with respectively 0 to 20 mA. They can also operate in static mode until 150V [3]. During electrostatic discharges (ESD) with Human Body Model (HBM) test, failure was observed at voltages from about 50V. The lateral diodes supported up to 200V in static mode when submitted to HBM-ESD failure at -140V. They have a threshold voltage of 0.6V, an internal resistance $R_{\text{on}}=33\text{m}\Omega$ and a high leakage current with milliamps.

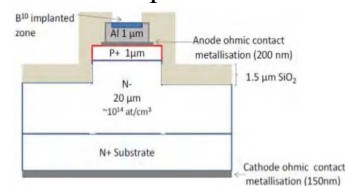


Fig. 1: Transversal section of vertical SiC diode

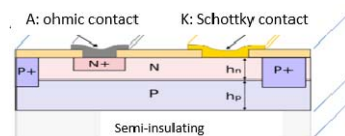


Fig. 2 : Transversal section of lateral Schottky diode

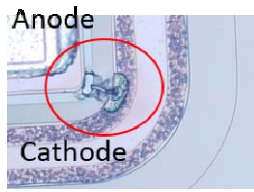


Fig. 3: Failure visualization after ESD stress on lateral diode

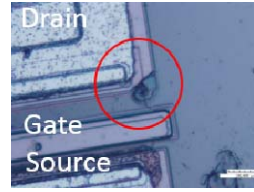


Fig. 4: ESD Failure at the MESFET corner

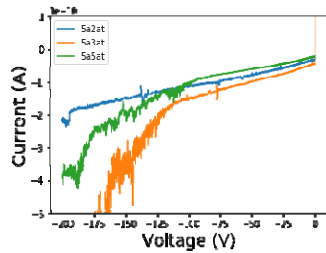


Fig. 5: I-V for three vertical diodes

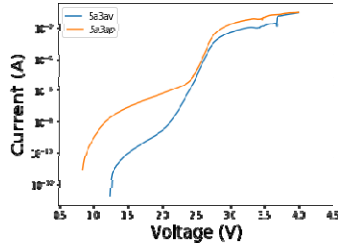


Fig. 6 : I-V in semilogy for SiC vertical diode before failure (5av2) and after (5ap2)



Fig. 7: Optical microscopy after high voltage failure on the corner of the device

3. Definition of destructive events

Two destructive stresses were performed in this article. First, the MESFET and the lateral diode were evaluated against ESD. HBM corresponds to a 150 pF capacity discharge. In this test method, the amplitude of the stress was increased until failure observation (Fig.3 and Fig.4). An electric arc was thereafter visible at microscopic scale between cathode and anode electrodes, using an optical microscope (Fig.3). I-V measurement present an abnormal current increase. According to the failure visualization, this current discharges through the defect appeared as a dielectric breakdown.

The second stress performed in this study was related to static voltage rise on the vertical diode. Voltage rise was first applied in reverse mode on three diodes. Up to 200V, no failure were observed (Fig.5) although some devices presented significant current increase, with particularly higher leakage current. One hypothesis to explain this observation could be that impact ionization -due to strong field- may have increased the probability of electrons crossing the Space Charge Barrier. The electric field applied could thus have been insufficient to create a crack in the dielectric, while in a transistor -composed of a succession of doping- a destructive parasitic transistor is triggered.

In forward mode, after reaching 30V a failure was revealed: the current increases linearly as represented in blue in Fig.6. This phenomenon occurred before failure as it can be seen in yellow. To take advantage of covering a surface without metallization, the tip was placed on the edge of the device and creates a defect, as depicted in Fig.7. As the failure occurred, the diode no longer emitted photons and its current level decreased drastically. When the voltage was increased again, the current increases was slower, indicating that R_{on} was modified (Fig.5).

4. Lock-in thermography after ESD stress

After ESD, thanks to SEM observation (Fig.4), it was shown in [4] that a too strong electric field can break the SiO_2 layer [5]. However, other tools have to be used to complete the analysis.

Even if the defect is visible on the surface, Lock-in Thermography -carried out at the CNM laboratory- could help to better and deeper understand failure mechanisms. After appropriate treatment, this infra-red measurement provides useful amplitude and phase representations of the excited electrons during device polarization [6]. In this study, 1V sinusoidal signal at a frequency of 100Hz was applied between MESFET Drain and Source.

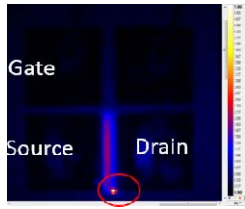


Fig. 8: Amplitude image with lock-in thermography after HBM-ESD stress on SiC MESFET

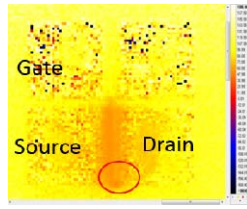


Fig. 9: Phases Image with lock-in thermography after HBM-ESD stress on SiC MESFET

Thereby failures have been located at the gate corner. Indeed failures were identified in x-axis and y-axis with the amplitude image (Fig.8) and in z-axis with the phase image, where the corner position depicted deeper failure characteristics (Fig.9). This representation is consistent with the SEM representation. Taking together, these results strongly suggest the creation of deep hot spots at the corner of the MESFET as failure origin. The resolution of this method is of about ten micrometers. It helps defining interesting hypotheses to understand failure mechanism, i) heating may have caused a hole in the semiconductor by sublimation, or ii) metal layer may have melt at the component surface, modifying the contact resistance, and slightly digging the SiC surface.

5. FIB-EDX results

Another method to study SiC-defects consists in using Focus ion Beam (FIB) [7]. In a previous study [3], short circuits were submitted to high temperatures until failure. Thanks to FIB analysis, the authors identified failure origin as gate metallization failure.

In one of our previous study, the FIB analysis on MESFET device also clearly revealed the presence of a hole (Fig.10). This defect undoubtedly appeared after the activation of a parasitic transistor, causing SiC sublimation, during ESD [3].

In this study, both FIB and Energy Dispersive X-ray (EDX) analyses were performed on vertical diode. Results suggested a melting of the metallization at the interface (Fig.11 and Fig.12). Comparing EDX response before and after stress, Aluminum Amplitude level decreased

significantly, whereas Silicon level increased and Nickel and Titan stayed stables (Fig.13 and Fig.14). This result can be explained by the lower melting temperature of Aluminum in comparison with Nickel and Titan. In addition, the FIB cut (Fig.13) showed that the defect remained on the surface and that SiC was not attacked (Fig. 14), explaining its relative proportion increase. As a result, internal resistance decrease -previously described in 3.- may only be due to the local modification of the metallization.

Thanks to FIB, failure mechanisms were highlighted for both vertical diode and MESFET devices. Whereas surface-level failure was identified on vertical diode, MESFET presented a completely different defect structure, occurring as a hole in the semiconductor.

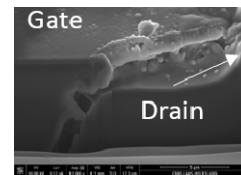


Fig. 10: SEM image after FIB on a failure in SiC MESFET after ESD [3]

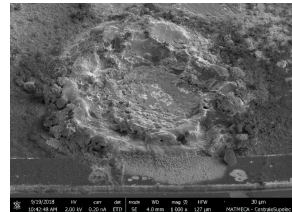


Fig. 11: SEM Image after FIB on a failure after high voltage applied on SiC vertical diode

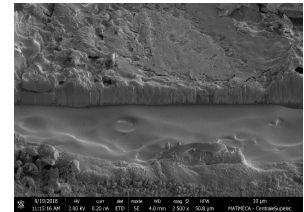


Fig. 12: Zoom on failure in SiC vertical diode

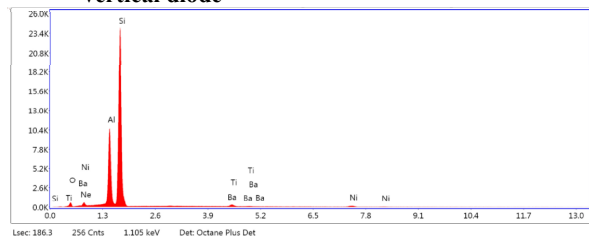


Fig. 13: EDX of SiC vertical diode before failure

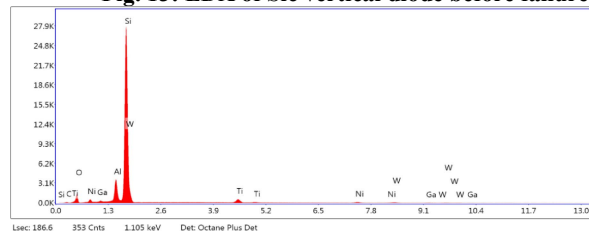


Fig. 14: EDX of SiC vertical diode after failure

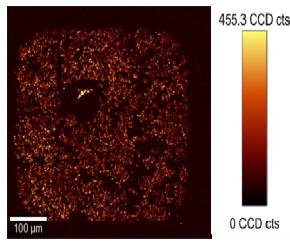


Fig. 15: Micro-Raman mapping of the Si integrated intensity

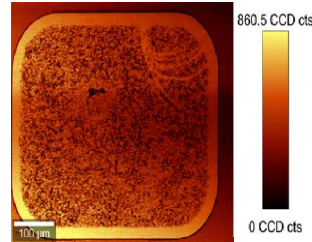


Fig. 16: Micro-Raman mapping of the SiC integrated intensity

6. Micro-Raman analysis

In this study, after identification of the vertical diode failure, we applied micro-Raman spectroscopy analysis -with a CLSM setup (Confocal Laser Scanning Microscope)- to identify SiC crystalline structure at the defect level [8]. This analysis indicated the presence of a metallic alloy residue on the diode surface. A migration of silicon atoms was also observed at the defect position (Fig.15 and Fig.16), suggesting atoms rupture and carbon atoms gathering in the observed metal alloy. In [9], SiC carbon atoms disappeared by combustion, leaving amorphous silicon and polysilicon on SiC surface device. Same results were obtained with Raman analysis performed in this study (Fig.15 and Fig.16). And the conclusions were the same for ESD failure and static failure. One strong explanation for this defect could be the presence of a strong electric field as well as a high temperature, both concentrated at the contact between the tip and SiC.

All together these methods help determining the mechanisms leading to failure for vertical and lateral SiC diodes as well as for MESFET component.

Conclusions

Failure mechanisms is crucial for new semiconductors, especially to entirely understand the limits and to overcome the industrialization obstacles. SiC is a semiconductor with different properties and behaviors than silicon, then, different tools for failure mechanism study are required. This work summarizes the mains different

tools usually used, with their pros and cons. A focus on lock-in thermography and on micro-Raman analysis is presented but the use of standard static measurements, assisted by TCAD Sentaurus simulation as well as SEM and FIB images, seems to be the most relevant approach to fully understand the three main phenomena that can occur in SiC devices: dielectric cracking, melting of the metallization and triggering of a parasitic transistor.

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References

- [1] J. Novacek, A. Viehl, O. Bringmann, W. Rosenstiel, "Reasoning-Supported Robustness Validation of Automotive E/E Components Process", in IEEE 11th ICSC, in 2017.
- [2] M. Lazar, "Technologie pour l'intégration de composants semiconducteurs à large bande interdite", HDR, Laboratoire Ampère, INSA Lyon, 2018.
- [3] T. Phulpin and al, "Contribution to Silicon-Carbide-MESFET ESD robustness analysis", in IEEE TDMR, pp214-223, in 2018.
- [4] M. Frischolz and al, "JTE concept evaluation and failure analysis: OBIC measurements on 4H-SiC p+-n diodes", in ISPSD & IC, Kyoto, 1998.
- [5] M. Wolborski, "Characterization of Dielectric Layers for passivation of 4H-SiC Devices", PhD. Thesis in Laboratory of Solid State Electronic (KTH) in Stockholm, 2006.
- [6] O. Breitenstein, W. Warta, M. Langerkamp, "Lock-in thermography: basics and use for evaluating electronic devices and material", 2nd ed. Berlin, Heidelberg: Springer-Verlag, 2010.
- [7] P. Diaz Reigosa, F. Iannuzzo, L. Ceccarelli, "Failure Analysis of a Degrade 2kV SiC MOSFET after Short Circuit at high Temperature", IEEE IFPA&IC, in 2018.
- [8] M. Ben Karoui and al, "Effect of defets on electrical properties of 4H-SiC Schottky diodes", Materials Science and Engineering C 28 (2008) 799-804, in 2008.
- [9] T.Kuhr, E. Sanchez, M. Skowronski, "Hexagonal voids and the formation of micropipes during SiC sublimation growth", in JAP 89, 4625, in 2001.