Low on-resistance and low trapping effects in 1200 V superlattice GaN-on-silicon heterostructures

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We report on the development of GaN-on-silicon heterostructures targeting 1200 V power applications. In particular, it is shown that the insertion of superlattices (SL) into the buffer layers allows pushing the vertical breakdown voltage above 1200 V without generating additional trapping effects as compared to a more standard optimized step-graded AlGaN-based epi-structure using a similar total buffer thickness. DC characterizations of fabricated transistors by means of back-gating measurements reflect both the enhancement of the breakdown voltage and the low trapping effects up to 1200 V. These results show that a proper buffer optimization along with the insertion of SL pave the way to GaN-on-silicon lateral power transistors operating at 1200 V with low on-resistance and low trapping effects.

1. Introduction

At the time of global warming, Gallium nitride on silicon (GaN-on-Si) technologies are highly promising to solve energy issues in the future [1-2]. Although the growth of GaN-on-Si represents a real challenge in managing large lattice and thermal mismatch [3-6], this technology remains the best candidate owing to its superior intrinsic properties such as high breakdown voltage (BV), large band-gap, high electron saturation velocity, low on-resistance, suitable for high volume commercialization of low cost substrates [7-22]. However, GaN-on-Silicon is currently limited to a voltage range around 1 kV on large wafer diameter with low

bow and low buffer trapping. That is why significant efforts are now deployed in order to find optimum GaN-on-silicon epitaxial structures enabling outstanding DC performances beyond 1 kV while delivering low trapping effects. This would allow extending the capabilities of these emerging types of devices. In this paper, we present GaN-on-Silicon material using superlattices into a carbon-doped buffer delivering a vertical breakdown well above 1.2 kV together with low buffer trapping for the first time.

2. Material description and device fabrication

Figure 1 shows a schematic cross section of the AlGaN/GaN-on-silicon heterostructures grown by metal organic chemical vapor deposition (MOCVD) capped with a thick in-situ SiN. Following the nucleation layer, the first structure referred as REF (shown in Figure 1.a) includes a 2.6 µm buffer (AlN nucleation layer and step-graded AlGaN layer), a 2.875 µm carbon-doped GaN layer (2×10^{19} cm^{-3}) resulting in a 5.5 µm total buffer thickness, a 0.3 µm unintentionally-doped GaN channel, a 20 nm $Al_{0.29}Ga_{0.71}N$ barrier layer and a 50 nm thick SiN MOCVD passivation. Using a Ti (12 nm)/Al (200 nm)/Ni (50 nm/Au (100 nm) stack with 875°C for 1 min rapid thermal annealing, ohmic contacts have been formed on the top of the barrier by fully etching the thick in-situ SiN cap layer using a Fluorine-based etching, yielding typical contact resistances of 0.4 Ω.mm. Then, the device isolation was achieved by using nitrogen ion triple implantation using the following energy doses: 20 keV, 50 keV, 100 keV resulting in an isolation depth of about 200 nm. A sheet resistivity of 300 Ω/sq has been measured by Hall Effect measurements revealing an electron mobility of 1800 cm^2/Vs and an electron concentration of 1.15×10^{13} cm^{-2}. The second structure (shown in Figure 1.b) consists in the same active layers but with a 1 µm carbon-doped GaN buffer and the insertion of 3.7 µm thick AlN/GaN superlattices (called SL) on top of the AlN nucleation layer. This structure shows with a mobility of 1600 cm^2/Vs and an electron concentration of 1.3×10^{13} cm^{-2}. Ni/Au gate metal was deposited within the in-situ SiN by partly dry etching the cap layer with a 20 nm

depth using an SF_6 plasma. The transistor gate length and source-gate distance were 2 μm and 1 μm, respectively with various gate-drain distances.

3. Results and discussion

Figure 2 shows the vertical breakdown measurements of both structures, which consist in applying a high voltage on an isolated ohmic contact (100×100 μm) while the substrate is grounded. The SL structure shows a vertical breakdown close to 1.3 kV defined at 1 mA/cm² while the REF structure delivers 1 kV under the same conditions despite the slightly thicker buffer layers. The achieved state-of-the-art vertical BV > 1.2 kV reflects the high crystal and growth quality. It can be noticed that from 1.1 kV up to 1.3 kV, the vertical breakdown shows a second plateau observed systematically with a leakage current below 1 mA/cm². Even though the related mechanism is still under investigation, it shows that the superior blocking voltage capabilities of the AlN/GaN superlattice results from a higher effective bandgap than the AlGaN back barriers and a better strain relaxation. Furthermore, the temperature dependence vertical breakdown measurements up to 1 kV (limited by the setup) have been performed as shown in **Figure 3**. A lower vertical leakage current is observed up to 150°C for the SL structure. The leakage current increase with the temperature is much lower than the REF structure, which further confirms the higher voltage insulation resistance nature of the SL structure. In addition, **Figure 4** depicts the lateral BV as a function of isolated contact distances while the substrate is floating. The measurements have been performed on-wafer and the samples have been immerged in a Fluorinert solution in order to avoid arcing in air. The lateral BV is well above 2000V and comparable for both structures when using large contact distances. The inset shows specifically the lateral BV characteristics with a 12 μm distance corresponding to the saturated regime. It turns out that the benefit of the superlattice configuration can only be observed when the substrate is grounded (e.g. when the vertical field is significant). On the other hand, from a practical point of view, power devices are generally used with grounded substrate. Electrical

characterizations have been realized on 2×50 µm transistors. The gate length was 2 µm with various gate-drain distances (GD) as shown in **Figure 5** (Ref) and **Figure 6** (SL). Transfer characteristics I_D-V_G reveal a low leakage current and an excellent pinch-off behavior reflecting the absence of parasitic punch-through effects or gate leakage current. The higher threshold voltage for the SL structure than the REF is most likely due to the gate etching depth, which may be higher than expected. High current densities are observed in both cases. The lower current density for the REF structure is in agreement with the lower electron concentration as compared to the SL structure. This is due to the AlGaN back barrier inducing a polarization rather close to the channel that slightly depletes the channel. It can be noticed that low static on-state resistance (R_{ON_STATIC}) of about 5 mΩ/cm² with a gate-drain distance of 5 µm has been obtained. For larger GD, R_{ON_STATIC} increases as expected but remains still below 15 mΩ/cm² for a GD = 40 µm for instance. **Figure 7** (Ref) and **Figure 8** (SL) show the 3-terminal off-state breakdown for several gate-drain distances with grounded and floating substrate. With grounded substrate, in agreement with the buffer breakdown measurements the 3-terminal BV at V_{GS} = -20V is about 1 kV and 1.3 kV for the REF and the SL buffer, respectively. Also, with floating substrate both structures shows a 3-terminal BV above 2 kV for large gate-drain distances.

When investigating higher voltage GaN power switch devices, it is critical to assess the related trapping effects. Buffer traps have been studied by means of substrate bias ramp measurements using various sweep rates at room temperature (RT) as described in [23][24]. Indeed, by monitoring the current between two ohmic contacts while ramping down the substrate bias, any charge storage is visible highlighting the presence of trapping effects within the buffer layers. The REF structure optimized for 650 V applications shows low trapping effects up to 800V with fast sweep rates (22 V/s). However, a strong trapping activation can be observed at 800 V when using slow sweep rates (4 V/s). The hysteresis increases significantly at 900 V as expected. On the other hand, the optimized SL structure uniformly delivers state-of-the-art low trapping

effects all the way to 1300 V regardless of the sweep rates as shown in **Figure 9**. Substrate bias ramp measurements have been also performed at high temperature in order to confirm these data. At 150°C, the REF structure shows trapping activation at 800V, which is in agreement with the measurements at RT using various sweep rates. The SL structure remains unaffected by trapping effects at high temperature (**Figure 10**). It has been shown that carbon-doping is directly linked to the trapping effects [24][25]. Thus the reduced trapping can be attributed to the lower incorporation of carbon in the case of SL buffer due to the slower growth process as compared to the REF structure. Trapping has been also studied through back-gating measurements on transistors with high vertical drain-to-substrate potential. In this case, tuning the transistor / substrate bias conditions allows in turn to distinguish the surface and bulk traps. **Figure 11** reveals the back-gating transistor measurements performed on the REF structure at a drain bias of 10V. We observe a perfect correlation with the substrate ramp measurements illustrated by low trapping effects up to 800V using a slow sweep rate and a strong activation at 800V and above using a fast sweep rate. For the SL structure (**Figure 12**), back-gating measurements have been applied and confirms the low buffer trapping up to 1200 V despite residual surface traps due to the processing that still needs to be optimized for operation beyond 1 kV.

4. Conclusion

This work showed an outstanding vertical breakdown above 1.3 kV using a 5 µm thick SL based carbon-doped buffer compared to 1 kV with a more standard AlGaN step-graded thicker buffer. Furthermore, significantly reduced buffer traps up to 1.3 kV have been observed by substrate ramp measurements up to 150°C. Back-gating measurements performed on transistors confirmed the state-of-the-art low trapping up to 1 kV limited by process-induced surface trapping at higher voltage. Finally, a 3-terminal BV above 2 kV associated to a $R_{on} < 15$ mΩ.cm²

for GD = 30 µm have been reached. These results pave the way to GaN-on-silicon lateral power transistors operating at 1200 V with low on-resistance and low trapping effects.

Acknowledgements

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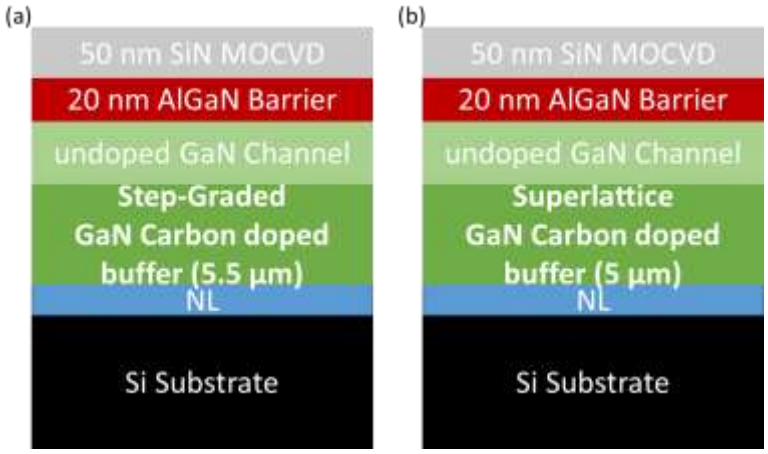

Figure 1. Schematic cross section of the structures with a step-graded buffer (REF) (a) and a superlattice buffer (SL) (b).

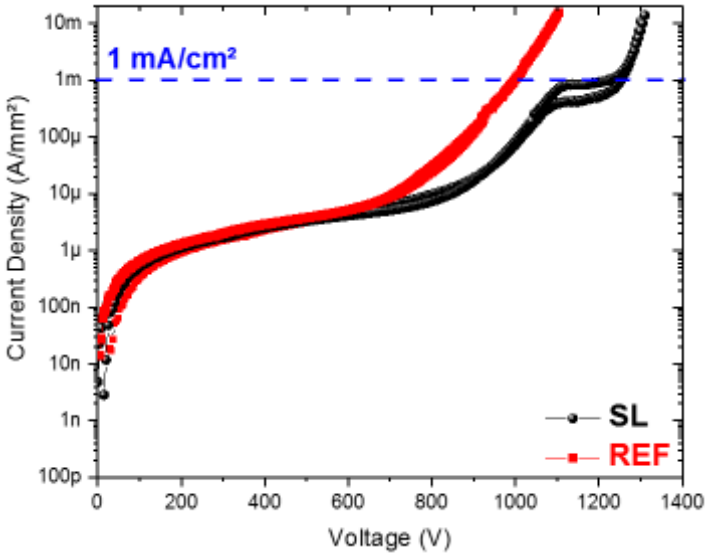

Figure 2. Vertical breakdown for the REF structure (red) and the SL structure (black) at room temperature.

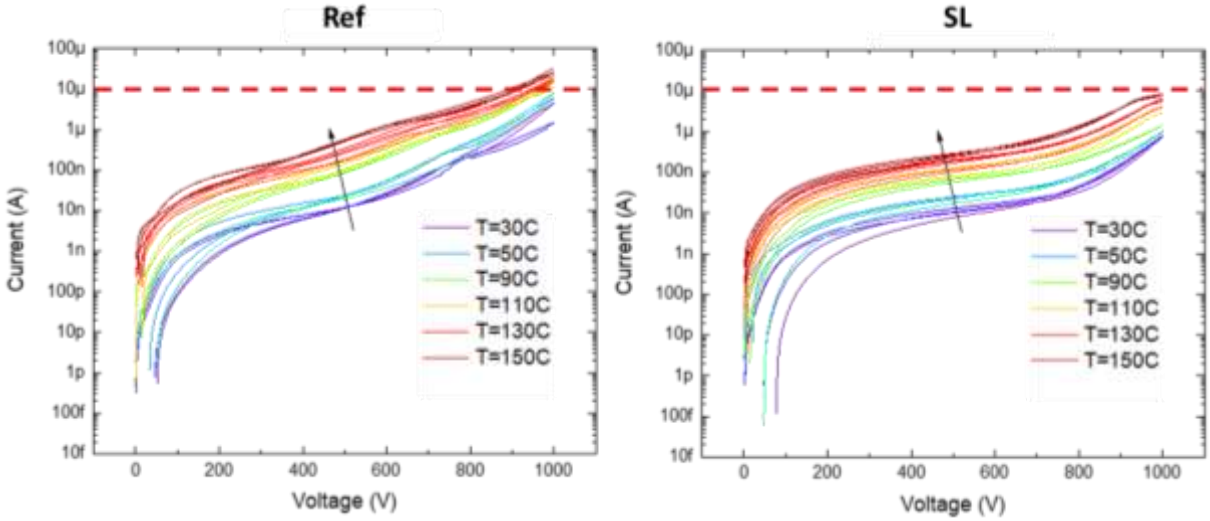

Figure 3. Vertical breakdown for the REF structure (left) and the SL structure (right) for various temperatures.

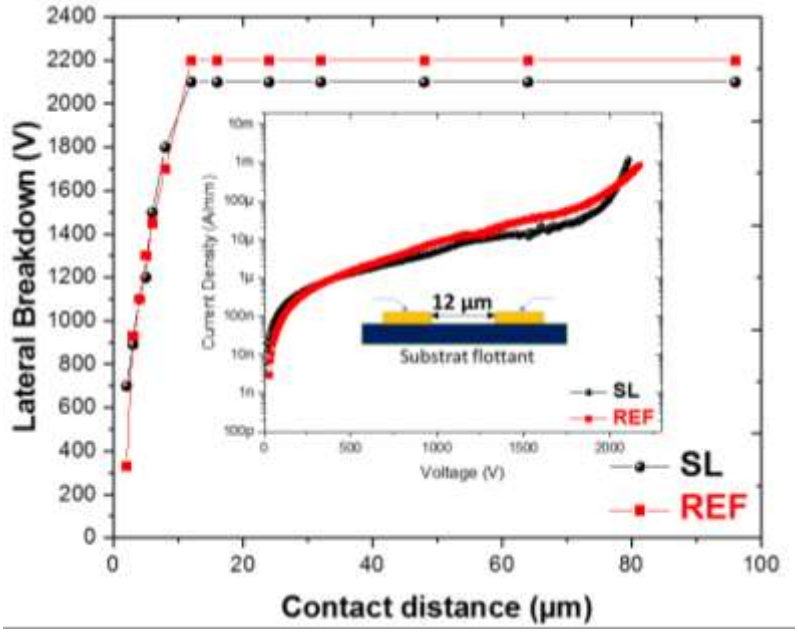

Figure 4. Lateral breakdown voltage as a function of the contact distances for the REF structure (red) and the SL structure (black) at room temperature.

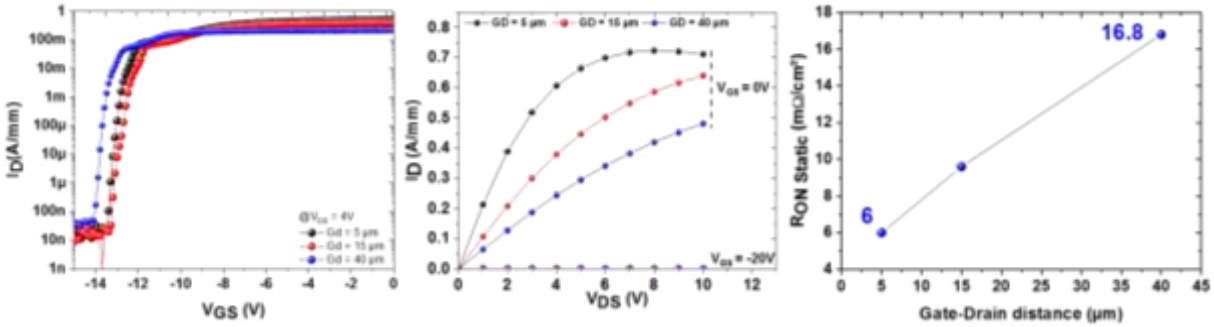

Figure 5. Transfer, open channel output characteristics at V_{GS} = 0V and R_{ON} for the REF structure.

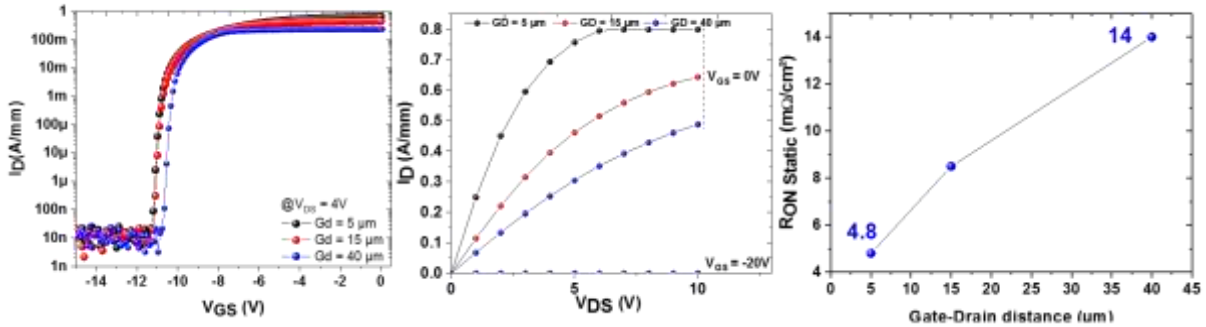

Figure 6. Transfer, open channel output characteristics at V_{GS} = 0V and R_{ON} for the SL structure.

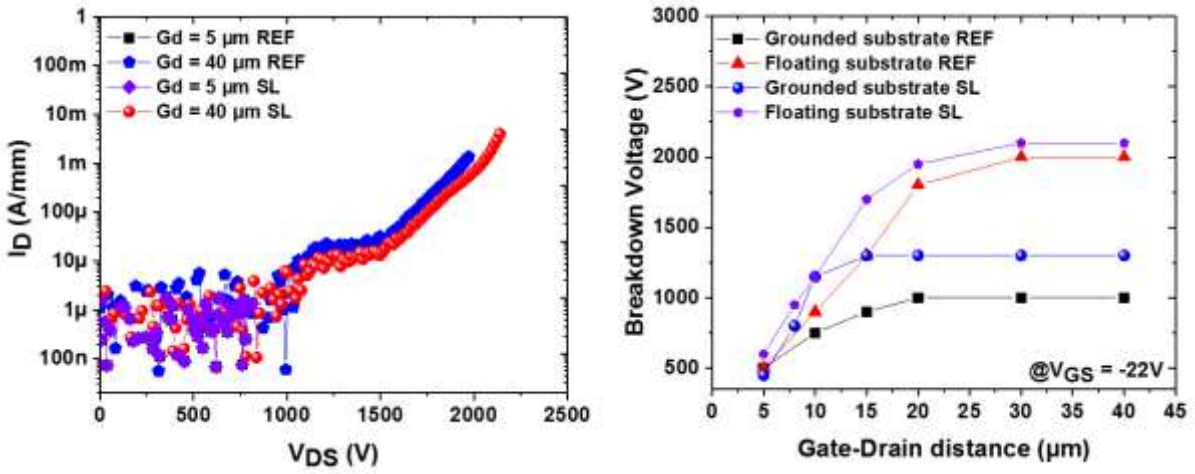

Figure 7. 3-terminal breakdown voltage for the REF and SL structures at V_{GS} = -22 V

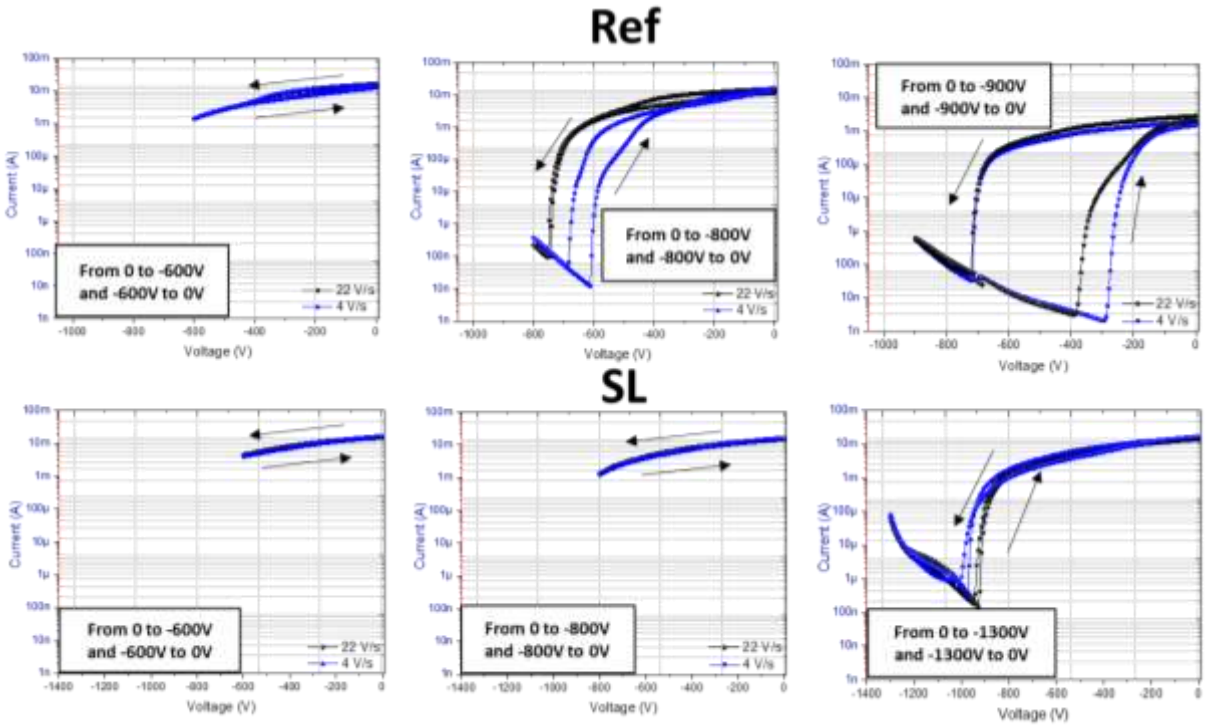

Figure 8. Substrate bias ramp measurements for the REF structure (top) and the SL structure (bottom) at room temperature.

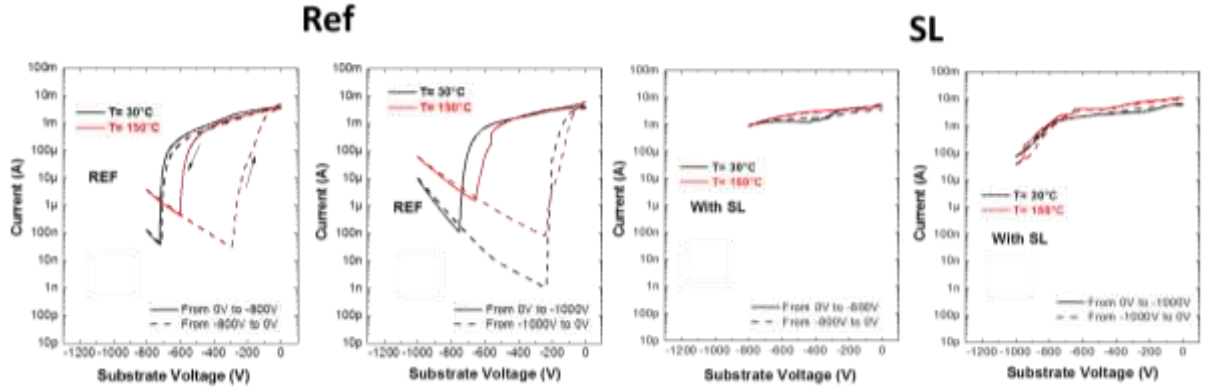

Figure 9. Substrate bias ramp measurements for the REF structure (left) and the SL structure (right) up to 150°C.

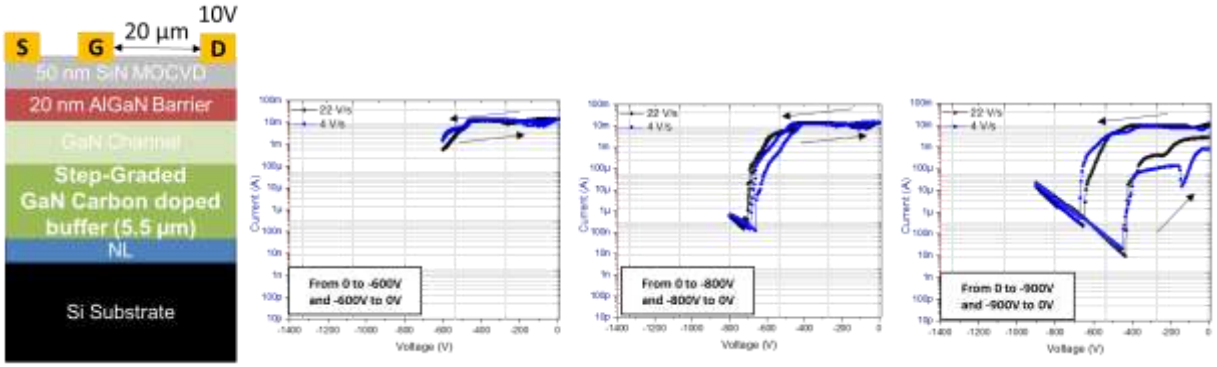

Figure 10. Back-gating measurements up to 900 V for the REF structure with V_{DS} = 10V

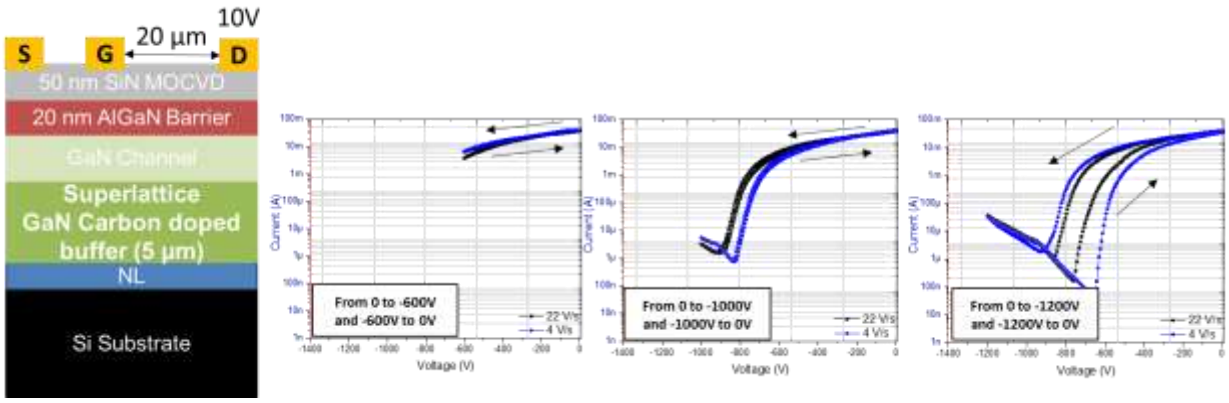

Figure 11. Back-gating measurements up to 1200 V for the SL structure with V_{DS} = 10V