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Power switch failures tolerance and remedial strategies of a 4-leg floating interleaved DC/DC boost converter for photovoltaic/fuel cell applications

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In recent years, many researchers have proposed new DC/DC converters in order to meet the fuel cell requirements. The reliability of these DC/DC converters is crucial in order to guarantee the availability of fuel cell systems. In these converters, power switches ranked the most fragile components. In order to enhance the reliability of DC/DC converters, fuel cell systems have to include fault-tolerant topologies. Usually, dynamic redundancy is employed to make a fault-tolerant converter. Despite this kind of converter allows ensuring a continuity of service in case of faults, the use of dynamic redundancy gets back to increase the complexity of the converter. In order to cope with reliability expectations in DC/DC converters, floating interleaved boost converters seem to be the best solution. Indeed, they have much to offer for fuel cells and DC renewable energy sources (i.e. photovoltaic system), including reduced input current ripple and reliability in case of faults. Despite the offered benefits of this topology, operating degraded modes lead up to undesirable effects such as electrical overstress on components and input current ripple increasing. The aim of this paper is to carry out a thorough analysis of these undesirable effects and to propose remedial strategies to minimize them.

1. Introduction

In order to cope with air pollution, global warming and oil depletion, electric transportation including Battery Electric Vehicles (BEVs), Hybrid Electric Vehicles (HEVs), Fuel Cell Electric Vehicles (FCEV) seems to be the most effective alternative to replace conventional vehicles in the future [1–4]. In the case of electric vehicles using Hydrogen as fuel, Fuel Cells (FCs) have much to offer. A FC uses the chemical energy of Hydrogen to cleanly and efficiently produce electricity. The latter can be used in a wide range of applications, including material handling, portable, stationary, emergency backup power, and transportation applications [5,6]. FCs present several advantages over conventional Internal Combustion Engines (ICEs) currently used in vehicles. They can operate

at higher efficiencies than ICEs, and can convert the chemical energy in Hydrogen to electricity with efficiencies up to 60%. Besides, FCs have lower emissions than ICEs. Indeed, they emit only water if Hydrogen is used as fuel, so there no carbon dioxide emissions and no air pollutants [5]. It is important to point out that Hydrogen can be produced from diverse, domestic resources. At the present time, most Hydrogen is produced from fossil fuels [5]. The use of fossil fuels gets back to increase carbon dioxide emissions and air pollutants. Among the existing processes to produce Hydrogen, electrolysis is a promising option for Hydrogen production from renewable resources (e.g. wind, solar) [5,7,8]. Hydrogen produced via electrolysis can result in zero greenhouse gas emissions, depending strongly on the source of the electricity used [8].

In recent years, Proton Exchange Membrane Fuel Cells (PEMFCs) have taken advantage of a growing interest from researchers and industrials due to their fast startup time, favorable power-to-weight ratio and solid electrolyte reducing corrosion and electrolyte management problems [5,9,10]. For this reason, PEMFCs are particularly suitable for automotive applications. In general, FCs generate a very low voltage of the order of 0.672 V at nominal

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Nomenclature

Acronyms

BEV	battery electric vehicle
DC	direct current
ECU	electronic control unit
FC	fuel cell
FCEV	fuel cell electric vehicle
FIBC	floating interleaved boost converter
FICBC	floating interleaved cascade boost converter
FPGA	field programmable gate array
FTC	fault-tolerant control
GaN	gallium nitride
HEV	hybrid electric vehicle
IBC	interleaved boost converter
ICE	internal combustion engine
IGBT	insulated-gate bipolar transistor
OCF	open circuit fault
PEMFC	proton exchange membrane fuel cell
SCF	short circuit fault
SiC	silicon carbide
SOC	state-of-charge
VHDL	VHSIC hardware description language

power [5]. As a result, individual cells are typically combined in series into a FC stack. However, the number of cells combined in series must be limited because stacking more cells in series decreases the reliability of the system [11,12]. When a PEMFC is used for transportation applications, such as electric vehicles, the DC bus voltage of the powertrain is usually a high-voltage of few hundred volts. As a consequence, a DC/DC converter is required to interface the FC stack with the DC bus of the powertrain. Such DC/DC converter is required not only for the voltage boost but also for the voltage conditioning as the FC stack voltage varies strongly with the load. In addition, these DC/DC converters must respond to several requirements for automotive applications, which are [13]:

1. Low weight and small volume.
2. High energy efficiency.
3. High power density.
4. Low cost.
5. Low electromagnetic interference.
6. Low input current ripple for both healthy and degraded operating modes to extend the PEMFC lifetime.

While the requirements (1)–(5) are linked with the expectations of transportation applications, the last requirement is related to the PEMFC. Over the last years, many researchers have investigated the effects of high-frequency current ripple coming from DC/DC converters on PEMFC performances [14–16]. Despite the impact on PEMFC durability is so far not well understood, many observations have ever been reported in the literature. In a previous work [13], a thorough review is presented regarding the effects of high-frequency current ripple on PEMFC performances. In summary, the FC stack voltage is subjected to long-term degradations due to the high-frequency current ripple. So far, the effects of high-frequency current ripple have been investigated up to a frequency equal of 10 kHz by using an electronic load combined with a signal generator [13]. Over the last years, the research has intensified to propose topologies of DC/DC converter operating at high-

Roman symbols

B_m	magnetic field of the inductor (T)
B_{max}	maximum magnetic field of the inductor (T)
C	capacitor (F)
D	duty cycle
f_s	switching frequency of the converter (Hz)
H	magnetic H-field (A/m)
i_{fc}	fuel cell stack current (A)
L	inductor (H)
N	number of turns of the inductor
N	number of legs
R	load resistance (Ω)
R_{diff}	differential resistance of the polarization curve (Ω)
S	power switch
S_F	area of the magnetic core of the inductor (m^2)
T_s	switching period of the DC/DC converter (s)
V_{dc}	DC bus voltage (V)
V_{fc}	fuel cell stack voltage (V)

Greek symbols

Δ	Ripple
μ_0	permeability constant (i.e. $4\pi 10e-7$ H/m)
μ_r	permeability of the inductor material (H/m).
Φ	magnetic flux of the inductor (Wb)

frequency, in order to increase the compactness and the energy efficiency of the converter. These topologies include soft-switching circuits [17–20], or more recently Silicon Carbide (SiC) [21,22], and Gallium Nitride (GaN) semiconductors [23]. Starting from the review presented in Refs. [13], it would be interesting to extend the investigations to high-frequencies (higher than 10 kHz). The use of a real DC/DC converter is the only way to broaden the scope of investigation to high frequencies. In summary, this would allow having a better understanding of the real impact of high-frequency current ripples on PEMFC lifetime; which one of the key challenges to FC commercialization [5] and [9].

Beyond the requirements given above, reliability and availability of FCEV powertrains remain major concerns so that the FCEVs can access to the mass automotive market [13] and [24]. Indeed, the presence of failures in powertrains can lead up to malfunctions in vehicles and consequently reduce their performances compared to conventional vehicles. Assuming that electrical faults occurred, powertrains of FCEV should include fault-tolerant DC/DC converter topologies and/or Fault-Tolerant Controls (FTCs). A FTC can be defined as the capability to compensate the faults in such a way that they do not lead up to additional faults within the converter and to performances reduction of the FCEV [25]. According to a recent survey focusing on reliability in power converters [26], power switches ranked the most fragile components in these converters. As it was highlighted in a previous work [27], power switch fault detection in DC/DC converters is an emerging research topic. Generally, a DC/DC boost converter topology is used not only in FC applications but also in photovoltaic systems due its simplicity and low cost. However, the latter presents several drawbacks for FC and photovoltaic applications which are [13] and [28]:

1. Low energy efficiency for high voltage ratio.
2. Low voltage ratio.
3. Weight and volume of the inductor (low compactness) by minimizing the input current ripple.

4. High input current ripple by optimizing the compactness of the converter.
5. The sensitivity of power switch faults (no redundancy).

In order to meet the FC requirements, some authors have proposed improvements for DC/DC boost converter topologies. In Ref. [17], the author has proposed a fully soft-switched pulse-width-modulated DC/DC boost converter for FC applications. This topology allows improving the energy efficiency and compactness of the converter to the detriment of the reliability of the converter. Besides, this topology suffers from having a low voltage ratio. In order to satisfy the high voltage ratio requirements, improvements have been carried out on boost topologies. For instance, cascaded boost converter [29], boost converter with switched capacitors [30], three-level boost converter [31], floating output DC–DC multilevel boost converter [32], and integrated double boost SEPIC [33,34], can be used for this purpose. In spite of the voltage ratio improvement, these topologies suffer from having high input current ripple in keeping small inductor value and volume. In Refs. [33] and [34], the input current ripple is reduced by coupling two inductors between each other. Besides, these topologies are not fault-tolerant in case of power switch faults. With the goal of improving reliability in DC/DC boost converters, dynamic redundancy can be employed [25]. The dynamic redundancy consists in adding components in order to make a fault-tolerant DC/DC boost converter [25]. In Ref. [35], Ribeiro et al. present a fault-tolerant three-level DC/DC boost converter for photovoltaic applications, depicted in Fig. 1. Fault-tolerance is made possible by means of a triac component located between the midpoint of the input capacitor bank and the midpoint of the Insulated-Gate Bipolar Transistor (IGBT). This triac is only triggered in the case of power switch fault occurrence. In addition, the latter allows reconfiguring the three-level boost converter into a two-level boost converter. However, the partial reconfiguration into a two-level boost converter after fault occurrence presents several drawbacks: power reduction (around 30%), input current ripple increasing (harmful for FC and photovoltaic applications), additional voltage stress to the power switch terminals (around 30%). Due to its drawbacks, this topology is not fit for FCEV applications. In Refs. [36–39], Jamshidpour et al. propose a fault-tolerant DC/DC boost converter based on dynamic redundancy. An example of fault-tolerant DC/DC boost converter topology is given in Fig. 2. Here, a photovoltaic source and supercapacitors are connected respectively to the DC bus through a boost converter and buck-boost converter. After power switch fault detection, a redundant leg (S_{R1} and S_{R2}) allows ensuring a continuity of service by switching on the fit triac switch (T_1 or T_2). It is important to emphasize that the use of dynamic redundancy gets back to increase the cost and the complexity of the converter [25]. For this reason, dynamic redundancy is not fit for automotive applications. According to a thorough review on papers focused on

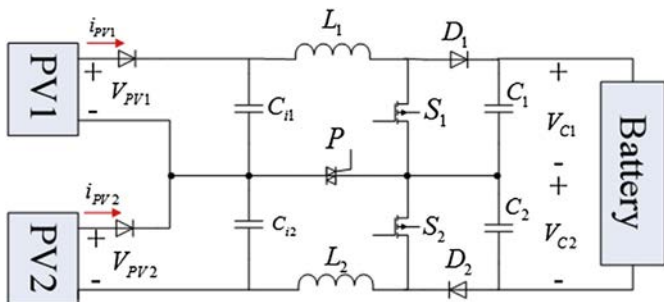


Fig. 1. Fault-tolerant three-level boost converter for photovoltaic applications [35].

power switch fault detection [27], only 34% of the papers present a power switch fault detection algorithm combined with a power switch fault management. Different approaches have been introduced in the literature regarding power switch fault management, such as dynamic redundancy with a control reconfiguration, control reconfiguration without dynamic redundancy and modularity. The major part of the papers is focused on the use of dynamic redundancy (around 69%); whereas 23% and 8% of the papers are focused respectively on control reconfiguration without dynamic redundancy and modularity [27].

In order to avoid the use of dynamic redundancy in FCEV applications, interleaved DC/DC boost converter topology is an effective solution. Many papers reported in the literature [13,28,40–42] have emphasized the benefits of this topology compared to other DC/DC converter topologies for FC applications. Indeed, interleaved boost converter topologies present several advantages in terms of compactness, reduced input current ripple, energy efficiency, and reliability in case of power switch faults. However, this topology suffers from having a limited voltage ratio similar to a boost converter. Improvements can be brought to the interleaved boost converter as reported in the literature in order to obtain a high voltage ratio [20,43,44]. However, these improvements increase the complexity of the converter by adding many components. The reliability and continuity of service of a 3-leg interleaved boost converter have been demonstrated through previous research works [13] and [27]. After power switch fault occurrence, the healthy legs allow compensating the faulty leg in order to avoid any power delivery interruption to the load. However, the loss of one leg leads up to additional electrical stresses (i.e. healthy leg currents increase of 50% compared to a healthy mode). Moreover, drastic increasing of input current ripple has been observed. Among existing interleaved boost converter topologies [28], Floating Interleaved Boost Converter (FIBC) [45,46], has many advantages for FCs and DC renewable energy sources (e.g. photovoltaic source) such as reduced input current ripple, high energy efficiency, compactness and high voltage ratio. For this reason, this topology is particularly fit for FC and photovoltaic applications where a high voltage ratio and low input current ripple are required [28,47,48], since FCs and photovoltaic sources produce an unregulated low-level DC voltage. In spite of the presence of natural redundancy, fault-tolerance has not been investigated yet [45–47,49]. Hence, the purpose of this paper is to carry out a thorough analysis of fault-tolerance of this topology in order to emphasize the undesirable effects of degraded operating modes. Besides, remedial strategies are presented in order to minimize these undesirable effects.

This paper is divided into 5 sections. After the introduction presenting a comprehensive review on this topic, section 2 presents the studied FCEV powertrain within the framework of this research work. Then, section 3 introduces the FIBC topologies and their main drawbacks in terms of fault-tolerance. Afterwards, in section 4, the experimental test bench carried out for this work is presented and obtained experimental results are given to investigate the undesirable effects of degraded operating modes. Finally, in section 5, a remedial strategy is introduced and experimental results are given to show the efficiency of the remedial strategy. Besides, a discussion focused on remaining challenges of this topology in case of power switch faults is provided.

2. Description of the studied FCEV powertrain

This research work comes within the scope of an European project MobyPost (<http://moby-post-project.eu/>), which aims at developing two fleets of five FCEV for postal delivery applications. The powertrain of this FCEV is shown in Fig. 3. FCEV powertrain is

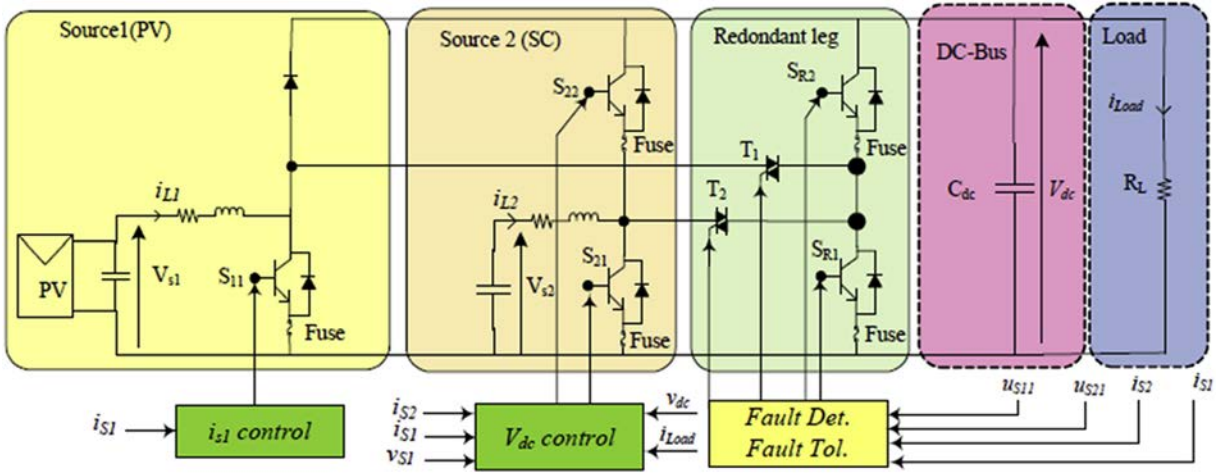


Fig. 2. Fault-tolerant DC/DC converter topology [36].

composed of a PEMFC, power converters (DC/DC and DC/AC converters), batteries and AC electric motors [13,27]. The choice of this powertrain results from a compromise in terms of price, compactness, and complexity of control [50]. In fact, in order to increase the global efficiency of the powertrain and to respond to sudden changes in the load, a storage device like a battery or a supercapacitor have to be added to recover the kinetic energy during regenerative braking phases and to provide energy during acceleration of the vehicle [51,52]. As it has been mentioned in Refs. [53], due to issues related to cost, manufacturing, robustness of the technology, hydrogen production, and the hydrogen infrastructure, the FCs could be used in a few years, as range extenders instead of the internal combustion engine-driven generators in series HEVs. These vehicles composed of a smaller FC and a larger battery (battery dominant) may be the future direction for automobiles [54–56].

In the case under study, the batteries are used as primary power source to assist the propulsion of the vehicle during transient phases and to absorb kinetic energy during regenerative braking phases; whereas the PEMFC is used as auxiliary power source to extend the autonomy of the vehicle [55,56]. In this case, the PEMFC operates like a range extender to maintain the State-of-Charge (SOC) of the batteries at a moderate value in order to limit its

aging. Then, the hybridization between these two sources allows extending their lifetime.

Figs. 4 and 5 respectively show an example of driving cycle and the supplied power by the PEMFC and batteries according to the driving cycle. It can be seen in Fig. 5 that batteries allow satisfying

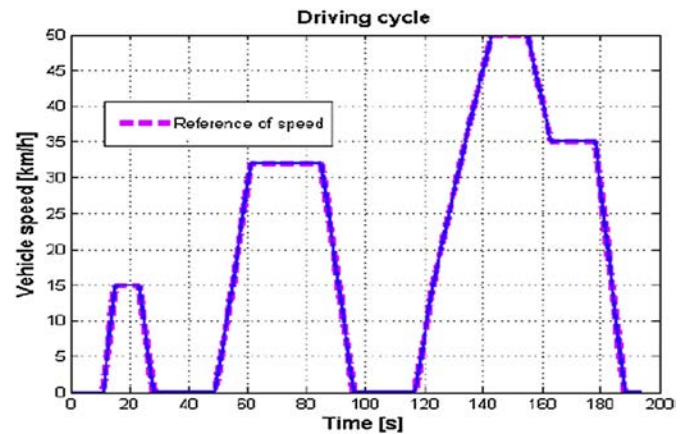


Fig. 4. Example of driving cycle.

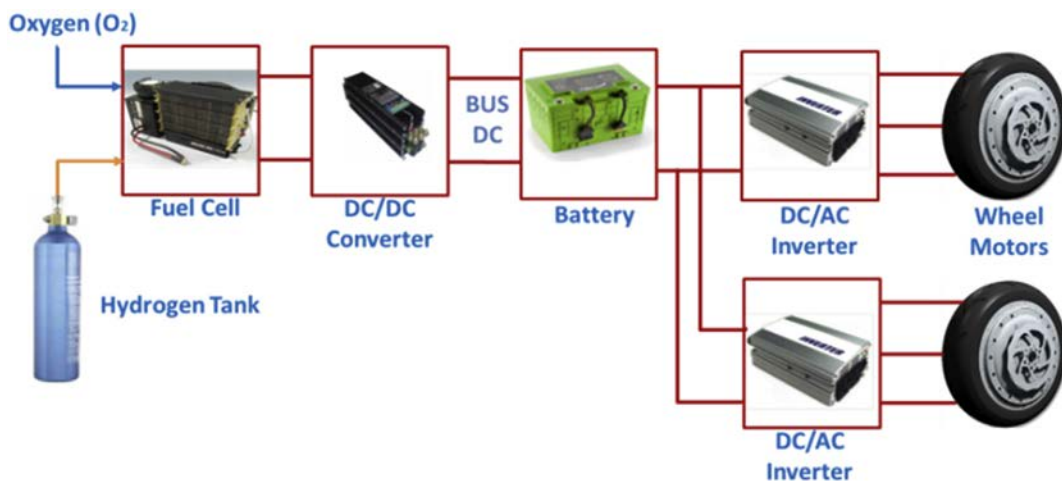


Fig. 3. Global block diagram of FCEV powertrain [13].

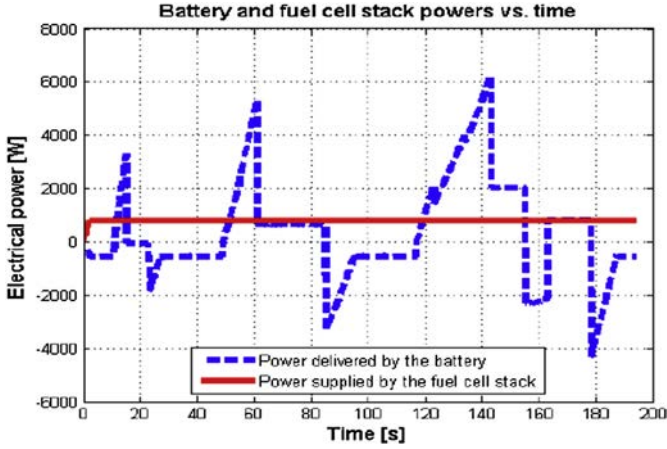


Fig. 5. Supplied power by the batteries and PEMFC according to the driving cycle.

power demand during acceleration phases (positive power) and absorbing kinetic energy during regenerative braking phases (negative power). The PEMFC is not requested during transient phases and supplies a constant power to the batteries by means of a DC/DC converter.

Due to the time constant of AC electric motors compared to the switching period of the FIBC topology (i.e. in our case, the switching period is equal to $50 \mu\text{s}$), the load can be considered as constant. Hence, the AC electric motors have no influences on the developed power switch fault detection algorithm and FTC. For this reason, in order to make easier the study, the rest of FCEV powertrain (batteries, inverter and AC electric motors) is considered like a resistive load. However, if the long-term effects as a result of an open-circuit fault wanted to be assessed on the fuel cell electric vehicle behavior, it would be crucial to reconsider the load modeling by developing an accurate model. This would allow having a better understanding of real impacts on fuel cell electric vehicle operation in case of power switch failures in DC/DC converter.

3. Presentation of FIBC topologies and their main drawbacks in terms of fault-tolerance

Several topologies based on classic boost converter have been proposed in the literature with the aim to improve the compactness, voltage ratio, energy efficiency and reliability [45] and [49]. Basic modifications brought to the classic boost converter topology are given in Ref. [45]. These new topologies allow building fault-tolerant interleaved converter topologies with high voltage ratio and reduced input current ripple. For this reason, these topologies are particularly suitable for FC and photovoltaic applications. A 2-leg FIBC is depicted in Fig. 6. The latter is built from the non-floating version of the boost converter (i.e. upper part) and the floating version of the boost converter (i.e. lower part). The interleaving concept is guaranteed by the parallel connection between of the non-floating and floating versions of the boost converter and the respective shift between the two power switches (S_1 and S_2). This interleaving allows reducing the input current ripple. Moreover, this topology allows minimizing the electrical stresses (voltage and current) on the power devices. The voltage ratio is given by the following expression [45] and [49]:

$$M(D) = \frac{v_{dc}}{v_{fc}} = \frac{1+D}{1-D} \quad (1)$$

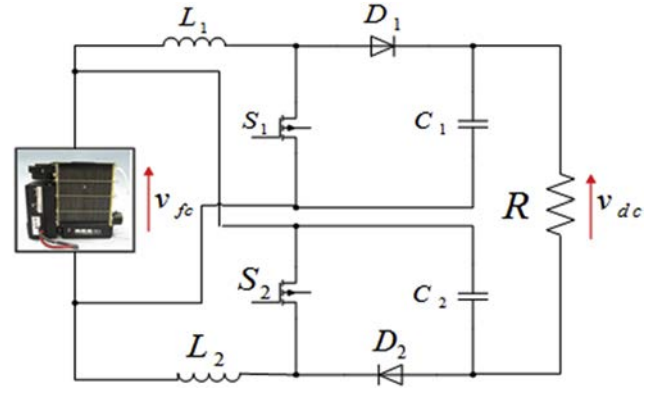


Fig. 6. 2-leg FIBC.

where v_{dc} is the DC bus voltage in [V], v_{fc} is the FC stack voltage in [V], and D is the duty cycle value.

Starting from this topology, others topologies can be built [45] and [49]. Two new topologies are given respectively in Fig. 7 and Fig. 8. The first is a 4-leg FIBC; whereas the second is a Floating Interleaved Cascade Boost Converter (FICBC). It is important to emphasize that the number of legs of FIBC topologies must be necessarily pair in order to keep a balance between the non-floating and floating parts. If the 2-leg and 4-leg FIBC are compared from the power switch fault-tolerance point of view, the 4-leg FIBC is more reliable. Indeed, by losing one leg of the 2-leg FIBC, this leads up to an unsteadiness between the non-floating and floating bus. In brief, this topology will lose all these benefits previously given. On the other hand, the loss of one leg of one of the parts (i.e. non-floating or floating) for a 4-leg FIBC, could be compensated by the other leg on the faulty part since the non-floating and floating part are independent between each other. However, keeping the balance between the two parts, this leads up to the leg overload; causing consequently additional electrical stress, particularly on inductive components. These effects are shown in section 4. An analysis carried out by Kabalo et al. [46] between a 2-leg, 4-leg and 6-leg FIBC based on several criteria (i.e. volume of inductors, FC current ripple, efficiency) has allowed demonstrating that the 4-legs FIBC is the best choice among the proposed converters. Regarding the FICBC, the cascade connection allows obtaining a high voltage ratio and a reduced output voltage ripple. The FICBC voltage ratio is given by the following expression:

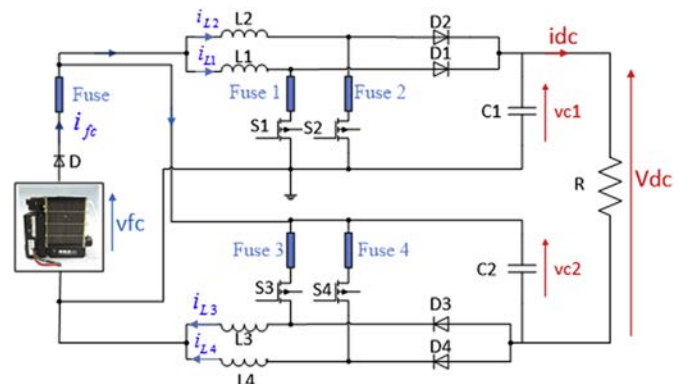


Fig. 7. 4-leg FIBC.

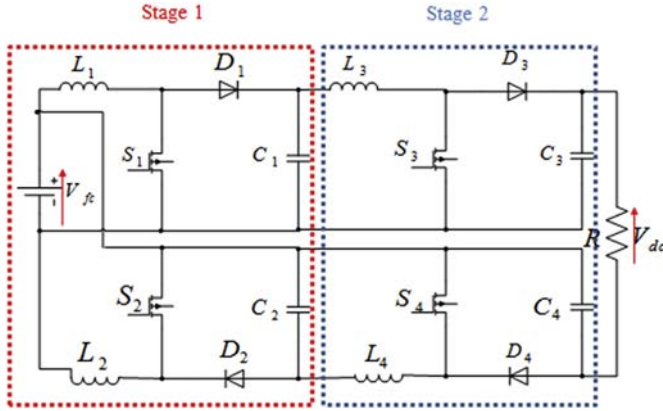


Fig. 8. Floating Interleaved Cascade Boost Converter (FICBC).

$$M(D) = \frac{v_{dc}}{v_{fc}} = \frac{2}{(1-D_1)(1-D_2)} - 1 \quad (2)$$

where D_1 and D_2 are respectively the duty cycles of the first and second stage respectively.

In order to minimize the input current ripple of the FICBC, a large inductor value is required and consequently increasing the overall volume of the converter. Besides, the reliability of the converter decreases by using the cascade connection. The reliability of the FICBC can be enhanced by using the interleaving concept, but this will get back to increase the complexity of the converter. Starting from this analysis, the 4-leg FIBC has been chosen in order to carry out a thorough investigation in terms of fault-tolerance. This investigation will allow to work out remedial strategies in order to minimize the undesirable effects in case of degraded operating modes.

In order to satisfy the fault tolerance requirements, fuses (Fuse 1, Fuse 2, Fuse 3, and Fuse 4) have been added in series with each power switch, as illustrated in Fig. 7. The fuses allow isolating faulty leg in case of SCFs. Furthermore, the PEMFC has to be electrically protected (e.g. addition of a fuse series connected with the FIBC) against possible SCF [13]. The diode D is used to protect the PEMFC from negative current. This diode conducts for all the duration of operation of the system. As a consequence, in order to reduce its conduction losses, it is realized from the parallel connexion of two diodes.

4. Description of the experimental test bench and experimental results in case of degraded operating modes

4.1. Experimental test bench description

In order to carry out a thorough investigation on the power switch failures tolerance, experimental tests have been carried out between a PEMFC and a 4-leg FIBC. The experimental test bench and the 4-leg FIBC are depicted in Fig. 9. The specifications of the implemented 4-leg FIBC are detailed in Table 1. The PEMFC is supplied using hydrogen from a tank under pressure, and with clean and dry air from a compressor. In order to supply the Electronic Control Unit (ECU) of the PEMFC with the necessary power to start the FC system, it has to be connected with an external power supply. The IBC topology has a TAMURA L03S050D15 current sensor per leg and a MTX 1032-B voltage sensor at the output for feedback control. The developed Matlab-Simulink control system has been transferred through the real-time board dSPACE DS 1104. Additionally, the control of the FIBC has been designed so that the

PEMFC works in the ohmic region in order to avoid the high and low voltage region for prolonging the PEMFC lifetime [13]. The polarization curve of the used PEMFC for this study is given in Fig. 10. The voltage range of the ohmic region has been determined by using the differential resistance [57]. Indeed, the differential resistance allows studying more easily the polarization curve variations and consequently to deduce the three operating regions [57,58]. The differential resistance is given by the following expression [57]:

$$R_{diff} = \frac{\partial v_{fc}}{\partial i_{fc}} \quad (3)$$

The differential resistance of the polarization curve is depicted in Fig. 11. Its evolution has been determined using the PEMFC model developed in a previous work [13]. As it can be seen in Fig. 11, the initial steep decrease in differential resistance is due to the charge transfer resistance in the low current region (i.e. activation region: area 1). It is followed by a constant value in the intermediate region (i.e. ohmic region: area 2) and a semi-exponential increase in the concentration region (i.e. area 3) [57]. The evolution of the differential resistance shows that the ohmic region is included between a PEMFC stack voltage of 25 V and 32 V. In order to guarantee the best performances of the FIBC topology, the parameters of the controllers are adaptative according to the operating point of the PEMFC [13].

The four PWM gate control signals are generated by a PWM signal generator block provided by the dSPACE library in Matlab-Simulink environment. However, these PWM signals are not shifted from each other. In order to guarantee the interleaving concept and to minimize the input current ripple, the four PWM gate control signals of the four switches (i.e. S1, S2, S3, S4) must be shifted from each other. In the case under study, each PWM gate control signal is shifted from each other with a time delay of $T_s/4$, where T_s is the switching period of the FIBC topology. These four PWM gate control signals are transferred to an Altera Cyclone FPGA board in order to shift them correctly from each other [13]. Additional details are given in a previous work [13] regarding the leg shift of the PWM gate control signals. The system specifications are summarized in Table 2.

The most common power switch failures in DC/DC converters are Open-Circuit Faults (OCFs), gating faults and Short-Circuit Faults [36]. Furthermore, OCFs can be a consequence of SCFs if and only if the fuse melts before the short-circuit damages the system [39,59]. These faults may occur due to external or internal events such as incorrect gate voltage, driver failure, lifting of bonding wires due to thermal cycling, electrical over stress (i.e. voltage or current) [36]. In this research work, only OCFs are investigated. The OCFs in each leg are simulated by using the four available push-button switches on the FPGA board. Each push-button switch is assigned to a specific pin number of the FPGA. The Cyclone device pin will see logic '1' when the push-button is not pressed; whereas it will see logic '0' when the push-button switch is pressed. Each push-button switch is combined with a specific PWM gate control signal. When the push-button switch is not pressed, the original PWM gate control signal is sent to the driver board in order to control the fit power switch of the FIBC. In contrast, if the push-button switch is pressed, the PWM gate control signal is forced to '0' in order to generate an OCF. If an SCF was generated, the PWM gate control signal would be forced to '1'. This strategy is carried out by means of a VHDL programming code implemented in the FPGA board. The flow diagram of this strategy is given in Ref. [27].

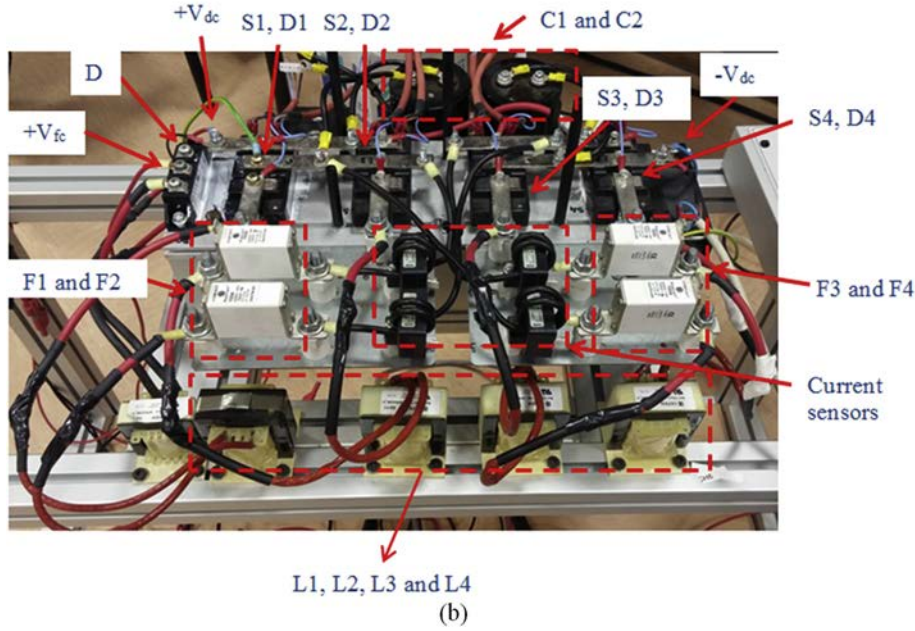
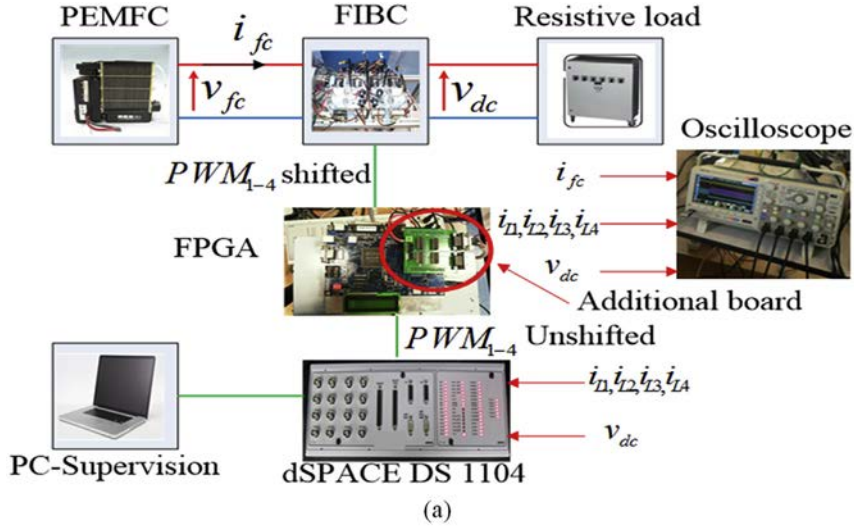


Fig. 9. (a) Experimental test bench carried out for this study, (b) 4-leg FIBC prototype.

Table 1
4-leg FIBC specifications.

Device	Specification
Power IGBT: S1 to S4	4× CM100DUS-12F
Diodes: D1 to D4	Anti-parallel diodes of 4× CM100DUS-12F
Diode: D	MEK 75-12 DA
Inductors: L1 to L4	4×(120 μH Cefem)
Capacitors: C1, C2	2 × 1000 μF electrolytic

4.2. Experimental investigation in case of degraded operating mode

During the operation of the PEMFC, two OCFs have been simulated in the two different parts (i.e. non-floating and floating) of the FIBC topology. These faults have been created separately. The obtained results from the experimental test bench are given in Figs. 12–14. As it can be seen in Figs. 12 and 13, only the healthy leg located in the faulty part is impacted by the loss of one leg. Indeed, as a result of an OCF on S1 (i.e. non floating-part), the healthy leg

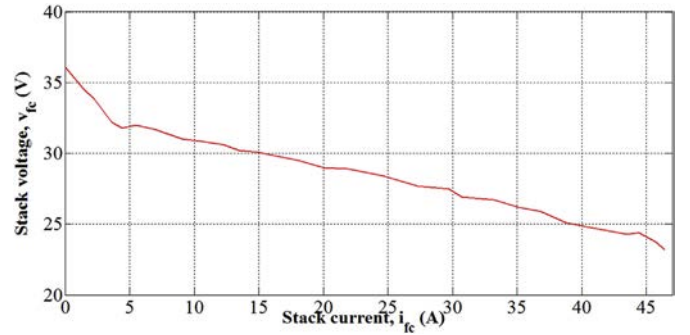


Fig. 10. Polarization curve of the used PEMFC for this study.

current (i.e. S2) increases of 100% compared to a healthy mode in order to compensate the failure. The same observation can be noticed in Fig. 13 with the healthy leg current (i.e. S4) increasing as a result of an OCF in S3. In Fig. 14, it can be observed the

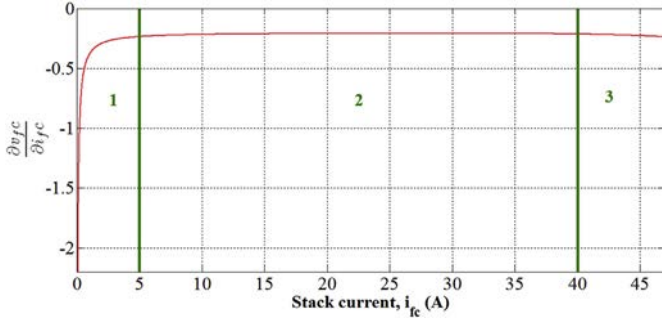


Fig. 11. Differential resistance of the polarization curve.

Table 2
System specifications.

Parameters	Values
PEMFC rated power, P_{fc}	1 kW
PEMFC rated current, I_{fc}	42 A
PEMFC current ripple, ΔI_{fc}	2 A
PEMFC voltage range, v_{fc}	25–32 V
Inductor value, L	120 μ H
DC bus voltage, V_{dc}	100 V
Switching frequency, f_s	20 kHz
Duty cycle range, D	0.5–0.56

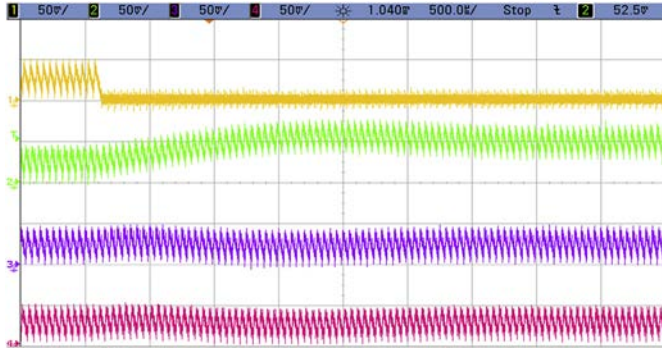


Fig. 12. Effects on the leg currents after an OCF on leg 1, obtained for $D = 0.53$: channel 1: leg 1 current (faulty) [5 A/div], channel 2: leg 2 current [5 A/div], channel 3: leg 3 current [5 A/div], channel 4: leg 4 current [5 A/div].

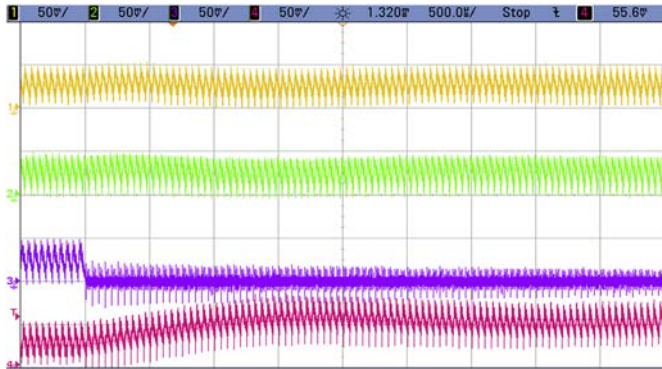


Fig. 13. Effects on the leg currents after an OCF on leg 3, obtained for $D = 0.53$: channel 1: leg 1 current [5 A/div], channel 2: leg 2 current [5 A/div], channel 3: leg 3 current (faulty) [5 A/div], channel 4: leg 4 current [5 A/div].

unsteadiness of the impacted leg current (i.e. S2) compared to the

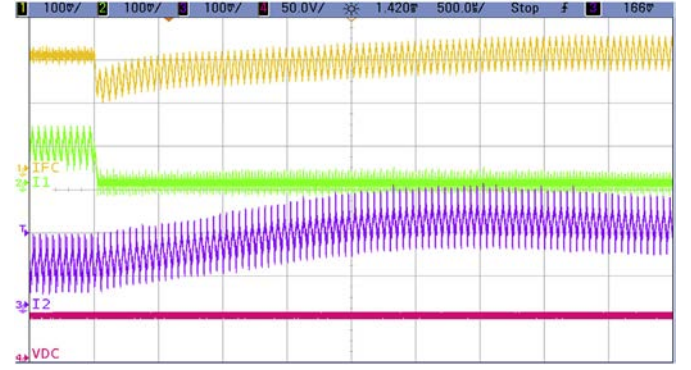


Fig. 14. Effects on the input current ripple and DC bus voltage after an OCF on leg 1, obtained for $D = 0.53$: channel 1: input current, I_{fc} [10 A/div], channel 2: leg 1 current (faulty) [10 A/div], channel 3: leg 2 current [10 A/div], channel 4: DC bus voltage [100 V/div].

other leg currents (i.e. S3 and S4). This unsteadiness between the three leg currents allows ensuring a continuity of service without impact on the DC bus voltage as shown in Fig. 14. The overload on the healthy leg of the faulty part allows keeping a balance between the non-floating and floating part of the FIBC topology. However, this overload leads up to additional electrical stresses particularly on inductive components and power devices. These additional electrical stresses may lead to saturation of the magnetic components and power switch failures.

In order to guarantee the reliability of the converter, power switches have been preliminarily sized in order to withstand the additional electrical stresses. By comparison, the inductors oversizing will lead up to the additional volume, weight and price which is not conceivable for FCEV applications [13]. For this reason, in order to avoid inductors oversizing, it is crucial to apply a FTC on the FIBC topology. The latter consists in decreasing the performances of the FIBC through its control. However, it is important to know accurately up to which PEMFC operating point, the inductors can withstand the additional electrical stresses without causing their saturation and consequently the loss of the control of the converter. Fig. 15 shows the evolution of a leg current for a healthy mode and a degraded operating mode. This evolution is plotted versus the duty cycle operating range. Each inductor has been sized to withstand one-quarter of the PEMFC rated current (i.e. 10.5 A). From a duty cycle value of 0.525, the inductors are out from their operating range. In order to avoid the saturation of magnetic circuits of inductors, the following requirement must be respected [60]:

$$S_F = \frac{L i_{Lmax}}{n B_{max}} \geq \frac{L i_{Lmax}}{n B_M} \quad (4)$$

where S_F is the area of the magnetic core in [m^2], L is the inductor value in [H], n is the number of turns, B_{max} is the maximum magnetic field of the inductor in [T], i_{Lmax} is the current flowing through the inductor in [A] and finally, B_m is the magnetic field of the inductor in [T]. Generally, the magnetic curve of an inductor is idealized as depicted in Fig. 16. The hysteresis phenomena have to be taken into account only to calculate the core losses. The magnetic B-field and the magnetic H-field are linked by the following expression:

$$B = \mu_0 \mu_r H \quad (5)$$

where μ_0 is the permeability constant (i.e. $4\pi 10e-7$ H/m) and μ_r is the permeability of the inductor material in [$H m^{-1}$]. If the magnetic B-field of the inductor exceeds the maximum magnetic B-field

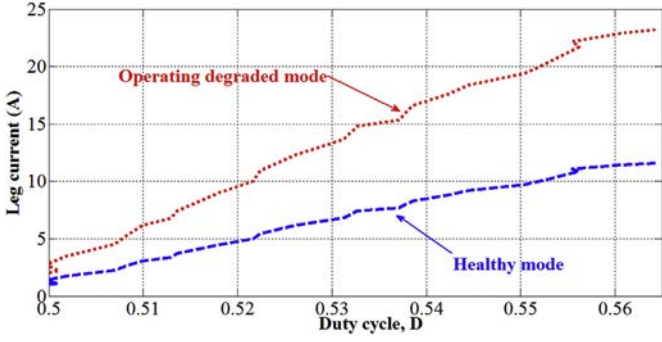


Fig. 15. Evolution of a leg current for a healthy mode and degraded operating mode.

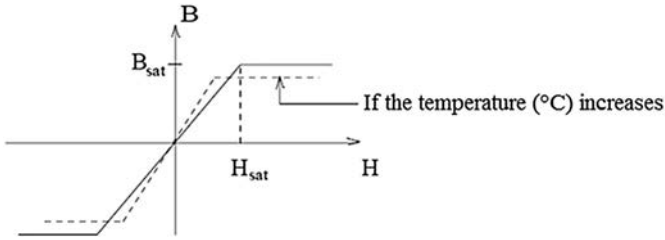


Fig. 16. Ideal magnetic curve of an inductor.

(described by the equation (4)), the inductor becomes saturated. In short, the inductor value decreases, causing consequently the loss of the control of the converter since the latter depends strongly on the system parameters [60]. In the case under study, the maximum magnetic field of the inductors is equal to 0.45 T. The rated current of each inductor is equal to 10.5 A and corresponds with a magnetic B-field of around 0.3 T. The magnetic flux of the inductor can be determined from the following expression:

$$\varphi = Li_L = nB_M S_f \quad (6)$$

As L , n and S_f are constant, it is possible to write that the magnetic B-field, B_M is proportional to the current i_L flowing through each inductor:

$$B_M = \frac{L}{ns_f} i_L \quad (7)$$

From the equation (7), the magnetic B-field can be determined versus the current flowing through each inductor (Fig. 17). Hence, it

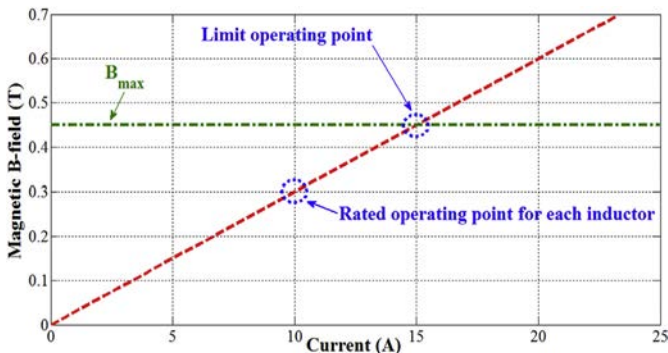


Fig. 17. Magnetic B-field versus the current flowing through each inductor.

is possible to anticipate the inductors saturation.

Starting from Fig. 17, it can be seen the inductors are saturated over a current equal to 15 A because the maximum magnetic B-field is reached. As a result, the PEMFC operating voltage range in the ohmic region must be limited up to 30 A in order to avoid damages on inductors. The previous and new PEMFC operating range taking into account the saturation of the inductors is given in Fig. 18 with the experimental polarization curve. Basing on Figs. 15 and 17, the new duty cycle range is included between 0.5 and 0.54. Figs. 15 and 17 are crucial to anticipate the saturation of the inductors. As the fuel stack current is restricted to 30 A, a power loss about 19% arises compared to a healthy mode. Besides, the power loss could be more substantial if the aging phenomenon (e.g. due to high-frequency current ripple) on the performances of the PEMFC (i.e. polarization curve) was taken into account.

The additional electrical stresses and saturation of the inductors are not the only issues in the case of degraded operating mode. Indeed, as it can be seen in Fig. 14, the loss of one leg leads up to the drastic increasing of input current ripple. This increasing is due to an unsuitable leg shift between the remaining legs. As it can be noticed in Fig. 19, the remaining legs continue to be shifted from each other with a leg shift equal to $T_s/4$. In order to illustrate the effects of degraded operating mode on the input current ripple, a study has been carried out to determine the expressions of input current ripple. The expressions can be determined by analyzing the operation of the FIBC and by using the dynamic expression of the input current ripple:

$$\frac{di_{fc}}{dt} = \frac{d_{iL1}}{dt} + \frac{d_{iL2}}{dt} + \frac{d_{iL3}}{dt} + \frac{d_{iL4}}{dt} \quad (8)$$

The input current ripples in healthy mode (i.e. without faults) are given by the following equations [46]:

$$\Delta i_{fc} = \begin{cases} \frac{v_{dc}(1-4D)D}{Lf_s} & \text{for } 0 < D < \frac{1}{4} \\ \frac{v_{dc}(4D-1)(2-4D)}{4Lf_s} & \text{for } \frac{1}{4} < D < \frac{1}{2} \\ \frac{v_{dc}(4D-3)(2-4D)}{4Lf_s} & \text{for } \frac{1}{2} < D < \frac{3}{4} \\ \frac{v_{dc}(4D-3)(1-D)}{Lf_s} & \text{for } \frac{3}{4} < D < 1 \end{cases} \quad (9)$$

where f_s is the switching frequency in [Hz] of the FIBC. In the same way, the same study can be carried out in order to determine the new equations of input current ripple in case of degraded operating mode. These new expressions are given below:

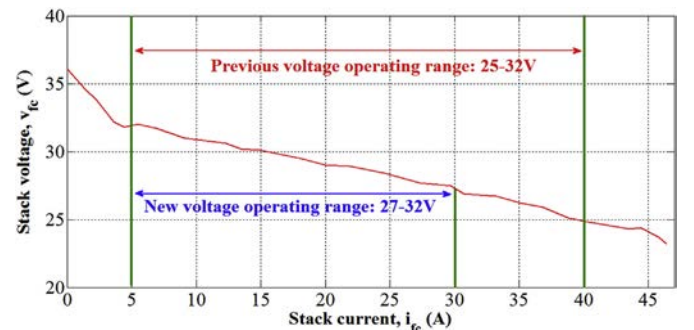


Fig. 18. PEMFC operating range taking into account the saturation of the inductors.

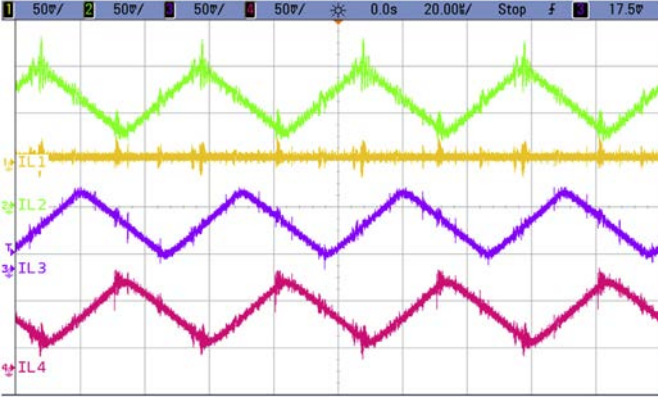


Fig. 19. Unsuitable leg shift between the healthy leg currents after an OCF on leg 1, obtained for $D = 0.53$: channel 1: leg 1 current (faulty) [5 A/div], channel 2: leg 2 current [5 A/div], channel 3: leg 3 current [5 A/div], channel 4: leg 4 current [5 A/div].

$$\Delta i_{fc} = \begin{cases} \frac{2v_{dc}\left(\frac{5}{4} - 3D\right)D}{Lf_s} & \text{for } 0 < D < \frac{1}{3} \\ \frac{2v_{dc}\left(3D - \frac{1}{2}\right)\left(\frac{5}{2} - 3D\right)}{9Lf_s} & \text{for } \frac{1}{3} < D < \frac{2}{3} \\ \frac{2v_{dc}\left(3D - \frac{7}{4}\right)(1 - D)}{Lf_s} & \text{for } \frac{2}{3} < D < 1 \end{cases} \quad (10)$$

These new expressions have been validated by performing experimental tests. In Fig. 14, input current ripple in degraded operating mode is equal roughly to 9 A. As the duty cycle varies between 0.5 and 0.54 (taking into account the operating limit of the inductors), the evolution of input current ripple has been plotted versus this duty cycle operating range (Fig. 20). As it can be observed in Fig. 20, the input current ripple increases drastically compared to a healthy mode. This increase is as large as that observed in a previous work [13] for a 3-leg IBC. Basing on a previous investigation on this topic as a result of a degraded operating mode [13], the PEMFC is not impacted by a degraded operating mode (Fig. 14). However, the input current ripple increase causes a slight increase of H₂ consumption. Despite the PEMFC is not affected as a result of a power switch fault in the FIBC, PEMFC operation over a long period of time could lead up to degradations

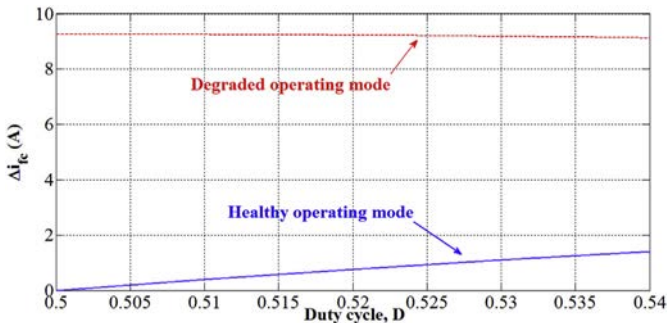


Fig. 20. Input current ripple evolution for a healthy mode and degraded mode versus the duty cycle operating range.

due to the high input current ripple as reported in the literature [13–16]. In Ref. [14–16], the authors have demonstrated by comparing an aging reference test and a dynamic test (i.e. application of a high-frequency current ripple) for 1000 h on a FC stack composed of 5 cells, that the FC stack voltage is subjected to degradations due to the high-frequency current ripple included between 1 and 5 kHz. Despite the effects of high-frequency input current ripple (>10 kHz) have not been investigated yet, the reported observations in the literature allow giving a general overview of likely degradations in the PEMFC. The most important degradations have been reported by Gerard et al. [15]. These authors have studied the effects of FC current ripple at a frequency equal to 5 kHz and a peak-to-peak amplitude of 20% of the FC average current (i.e. 110 A). The authors have observed a large disparity between the relative performances of different cells forming a stack (Fig. 21). As it can be seen in Fig. 21, cell 2 quickly diverges and shows the worst performance. Cells 1, 3 and 5 are the most efficient until the fourth characterization. At the end of the dynamic test, the potential drop of all cells except the cell 5 is faster than previously. By using the characterization by voltammetry, they have shown a significant increase of the current of the membrane permeation at the end of the dynamic test and a decrease of the active surface of platinum particularly important for the cells 1 and 2 (i.e. 29% drop in cell 1 and 23% for cell 2). These results, although not confirmed in the paper, could be an avenue that would explain the relationship of the rate of degradation of the active surface of platinum with the potential of the cell. Unfortunately, the dynamic test could not come to an end (i.e. duration of the dynamic test: 1000 h) due to the perforation of the cell membrane 4. The dynamic test has run for 590 h until a membrane failure occurs.

For this reason, it is crucial to propose a remedial strategy in order to reduce drastically the input current ripple and consequently the long-term degradations in the PEMFC. In a previous work [27], a state-of-the-art is provided regarding the reduction of high-frequency current ripple in DC/DC converters. The major part of the proposed solutions in the literature consists in using specific topologies of DC/DC converters or current ripple reduction techniques [27]. However, all these solutions have been developed when the DC/DC converter operates in a healthy mode without any power switch failure. Moreover, some proposed solutions increase the complexity and the volume of the converter by adding many components [27]. In the next section, a remedial strategy is proposed to minimize the input current ripple without adding components. The efficiency of the proposed remedial strategy is validated by carrying out experimental tests.

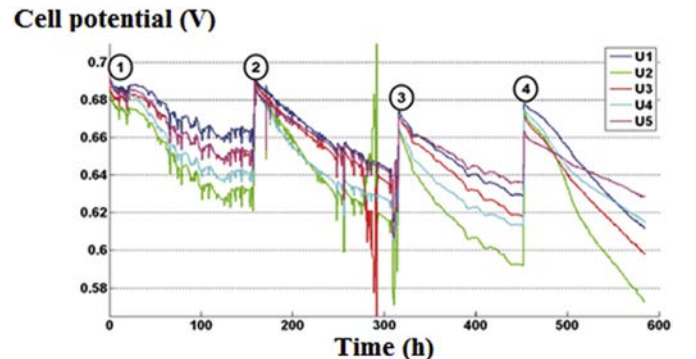


Fig. 21. Evolution of the cell potential during the dynamic test [15].

5. Proposed remedial strategy and experimental validation

5.1. Power switch fault-detection and remedial strategy

Before applying a FTC, it is important to detect accurately the faulty leg. Indeed, the information of faulty leg allows applying a suitable FTC to the FIBC topology in order to minimize the input current ripple. As mentioned in section 4, only the healthy leg located in the faulty part compensates the loss of one leg; whereas the others legs on the healthy part are not affected by the fault. To summarize, the faulty leg can be detected by analyzing the four leg currents. The power switch fault detection algorithm only needs the measurements from the four current sensors, used in the control of the FIBC. No additional sensors are required. Hence, the reliability of the measurements can be preserved [25]. The developed power switch fault-detection principle is explained below. This principle is given when the leg 1 is faulty (i.e. non-floating part) and can be fit to the others faulty legs.

For identifying accurately the faulty leg, four conditions are needed. For instance, for the faulty leg 1, the following conditions must be brought together:

1. The slope sign of leg 1 current must be negative (decreasing).
2. The slope sign of leg 2 current must be positive (increasing).
3. The waveform of leg 3 remains unchanged.
4. The waveform of leg 4 remains unchanged.

Each inductor current passes through a derivation block and then through a sign block which computes the slope sign of the current. For example, if the current increases, the slope sign is equal to '1'; whereas if the current decreases, the slope sign is equal to '-1'. The main drawback of this proposed power switch fault detection algorithm is that it can be applied only to interleaved DC/DC boost converter topologies because of their specific architectures. However, this power switch fault detection is efficient to detect accurately the faulty leg as demonstrated in the next part of section 5 regarding the obtained experimental results.

Once the faulty leg is identified and detected, a remedial strategy can be applied to the FIBC topology. Concerning this topology, FTC consists in changing the PWM gate control signal according to the faulty leg given by the proposed power switch fault detection algorithm. Indeed, the FTC depends strongly on the faulty leg. An unfit control reconfiguration could have undesirable effects on the system such as the FC current ripple increasing [13]. The flow diagram combining the power switch fault detection algorithm with the remedial strategy is given in Fig. 22. In order to gain the benefits of the used FPGA board [36–39], the power switch fault detection algorithm and the FTC have been implemented in the FPGA board

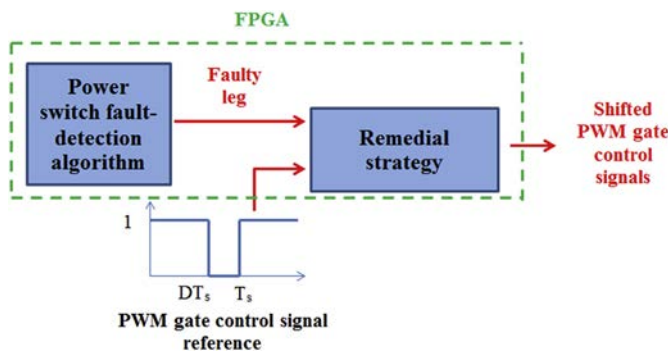


Fig. 22. Flow diagram combined the power switch fault detection algorithm with the remedial strategy.

by means of a VHDL programming code. The Quartus II software has been especially used to carry out the VHDL programming code. This VHDL programming code is then transferred to the FPGA board via an active serial connection. This interface performs communication between the FPGA (which implements the power switch fault detection algorithm and the FTC) and the PC (i.e. Quartus II software).

Table 3 gives the FTC to apply according to the faulty leg given by the power switch fault detection algorithm. On one hand, when the FIBC operates in a healthy mode, the power switch fault detection algorithm sends a logic '0' to the FTC. As a result, the normal leg shift is applied to the PWM gate controls signals. On the other hand, if one power switch is faulty, the algorithm sends a logic '1' to the FTC. Hence, the suitable PWM gate control signals are replaced by the new PWM gate control signals taking into account the suitable leg shift given in Table 3. The advantage of this FTC is that it can be fitted whatever the number of legs of interleaved DC/DC converter topologies. As it can be seen in Table 3, the leg shift of two PWM gate control signals has to be changed as a result of an OCF. By increasing the number of legs in interleaved DC/DC boost converter topologies; this leads up to increase the complexity of the FTC. The number of PWM gate control signals (i.e. N_{PWM}) to modify after fault occurrence can be determined by this following equation according to the number of legs (i.e. N) of interleaved DC/DC boost converter topologies:

$$N_{PWM} = N - 2 \quad (11)$$

5.2. Experimental results obtained

Starting from the power switch fault-detection algorithm and FTC, experimental tests have been performed in the laboratory when the PEMFC works at 80% of its rated power (i.e. $D = 0.535$) in order to take into account the saturation of the inductors. The purpose is to show and analyze the effects on the input current ripple applying the proposed FTC. Once the OCF has been detected on the faulty leg, the FTC is applied to the PWM gate control signals through the VHDL programming code implemented on the FPGA board. The results are depicted in Figs. 23 and 24. An OCF has been simulated through the FPGA board on the leg 2.

As it can be observed from Figs. 23 and 24, the loss of leg 2 is entirely compensated by the healthy leg located in the faulty part (i.e. non-floating part); whereas the legs 3 and 4 are not impacted by the loss of the leg 2. Therefore, the DC bus voltage remains

Table 3

Leg shift strategy to apply according to the faulty leg.

Faulty leg	Leg shift strategy to apply
Leg 1 (non-floating part)	1) Reconfigure the leg-shift of leg 3 ($T_s/2 \rightarrow 7T_s/12$) 2) Reconfigure the leg-shift of leg 4 ($3T_s/4 \rightarrow 5T_s/6$)
Leg 2 (non-floating part)	1) Reconfigure the leg-shift of leg 3 ($T_s/2 \rightarrow T_s/3$) 2) Reconfigure the leg-shift of leg 4 ($3T_s/4 \rightarrow 2T_s/3$)
Leg 3 (floating part)	1) Reconfigure the leg-shift of leg 2 ($T_s/4 \rightarrow T_s/3$) 2) Reconfigure the leg-shift of leg 4 ($3T_s/4 \rightarrow 2T_s/3$)
Leg 4 (floating part)	1) Reconfigure the leg-shift of leg 2 ($T_s/4 \rightarrow T_s/3$) 2) Reconfigure the leg-shift of leg 3 ($T_s/2 \rightarrow 2T_s/3$)

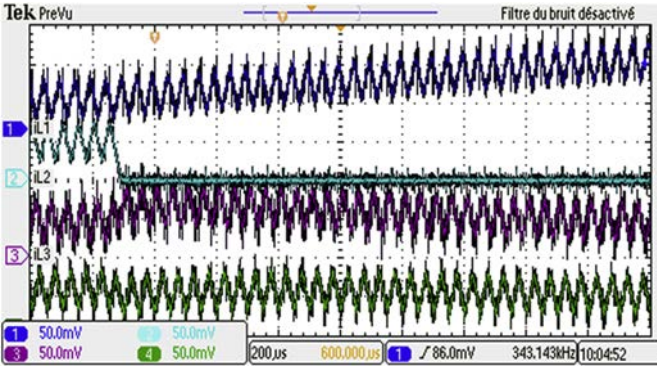


Fig. 23. Application of the FTC once the fault has been detected on leg 2: channel 1: leg 1 current [10 A/div], channel 2: leg 2 current (faulty) [10 A/div], channel 3: leg 3 current [10 A/div], channel 4: leg 4 current [10 A/div].

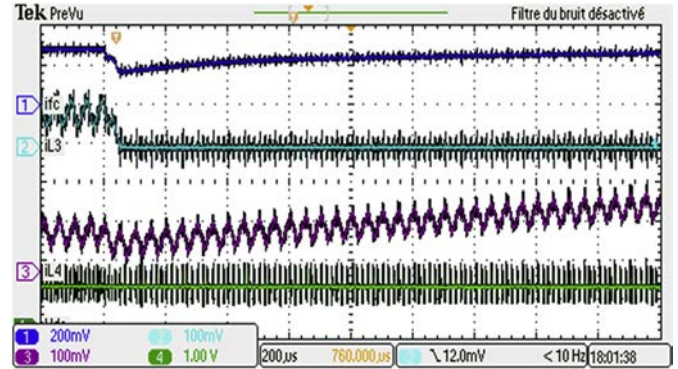


Fig. 26. Effect of the FTC on input current ripple: channel 1: fuel cell current [20 A/div], channel 2: leg 3 current (faulty) [10 A/div], channel 3: leg 4 current [10 A/div], channel 4: DC bus voltage [100 V/div].

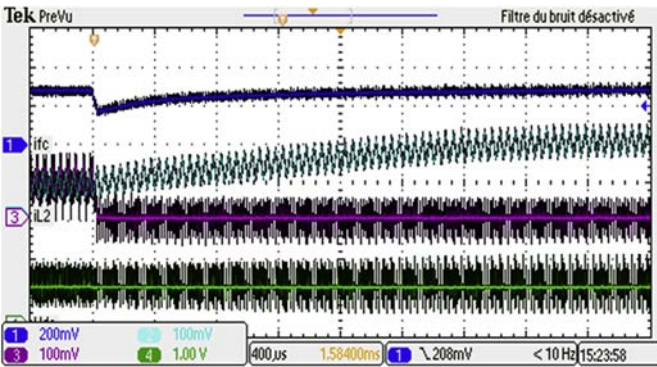


Fig. 24. Effect of the FTC on input current ripple: channel 1: fuel cell current [20 A/div], channel 2: leg 1 current [10 A/div], channel 3: leg 2 current (faulty) [10 A/div], channel 4: DC bus voltage [100 V/div].

constant despite the loss of one leg (Fig. 24). According to the faulty leg and Table 3, a fit FTC is applied to the control of the FIBC topology. This allows minimizing drastically the FC current ripple and consequently the reported long-term degradations in the literature (Fig. 24). In order to demonstrate the efficiency of the FTC whatever the faulty leg, an OCF has been simulated on the leg 3. The obtained experimental results are provided in Figs. 25 and 26. The OCF is compensated by the healthy leg located in the faulty part (i.e. floating part). The PWM gate control signals of the power switch S2 and S4 are modified to guarantee a minimum input current ripple. Besides, the DC bus voltage is not affected as a result of PWM gate

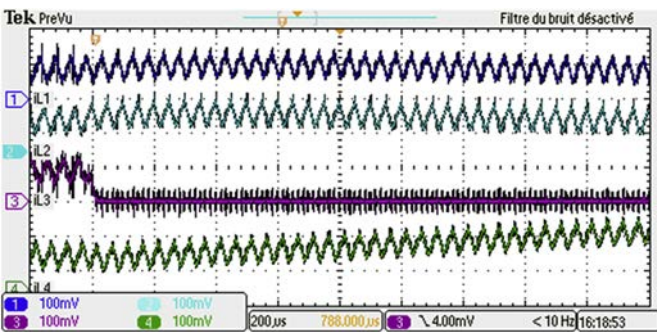


Fig. 25. Application of the FTC once the fault has been detected on leg 3: channel 1: leg 1 current [10 A/div], channel 2: leg 2 current [10 A/div], channel 3: leg 3 current (faulty) [10 A/div], channel 4: leg 4 current [10 A/div].

control signals change. As it can be seen in Figs. 24 and 26, the peak-to-peak value of input current ripple after fault occurrence is roughly the same compared to a healthy mode. In brief, the FIBC topology allows keeping its benefits from the input current ripple reduction point of view.

5.3. Discussion

Despite the benefits of 4-leg fIBC topology when it operates in healthy mode, an operating degraded mode leads up to the drastic increase of input current ripple and additional electrical stresses on the healthy leg of the faulty part (i.e. the current of the healthy leg increases of 100% compared to a healthy mode). The high current stresses flowing through the healthy switch of the faulty part are due the parallel connection of the non-floating and floating versions of the basic boost topology. If a 4-leg IBC was used to replace the FIBC, the electrical stresses on the healthy switches in case of degraded operating mode would be less important than a FIBC topology. Indeed, as demonstrated in a previous work [13] for a 3-leg IBC, the two healthy power switches compensate together the loss of one leg. Hence, the current stresses increase of 50% compared to a healthy mode. By comparison, for a 4-leg IBC, the current stresses of the three healthy legs increase of 33.33% compared to a healthy mode. These current stresses are three times smaller than a FIBC topology. Thus, the inductors operating range can be extended in degraded operating mode compared to a FIBC topology. Despite these benefits, the IBC topology suffers still from having a low voltage ratio, which limits its use for low power applications compared to a FIBC topology [13].

Another important issue is remaining, namely the reliability of the FIBC topology in the case of degraded operating mode. The power switches have to be correctly sized so that they can withstand the additional electrical stresses flowing through the healthy switches. Besides, it is crucial to work out a remedial strategy after fault-occurrence for critical operating case (as demonstrated in section 4) in order to protect the inductors against high current stresses.

6. Conclusion

The main objective of this paper was to investigate power switch failures tolerance of a 4-leg floating interleaved DC/DC boost converter. Nowadays, dynamic redundancy is widely used to make a fault-tolerant DC/DC converter. However, the use of dynamic redundancy in DC/DC converter gets back to increase its volume, price, and complexity, which are not suitable for automotive

applications. In order to avoid the use of dynamic redundancy, floating interleaved DC/DC boost converter is an effective solution. This topology is particularly suitable for automotive applications due to its many benefits such as: high voltage ratio, compactness, reduced input current ripple, high energy efficiency, and reliability in case of power switch faults. In this paper, open-circuit faults have been investigated. It was demonstrated that the loss of one leg in case of open-circuit fault leads up to additional electrical stresses on power devices and inductors. Indeed, as a result of an open-circuit fault, the current of the healthy switch located in the faulty part increases of 100% compared to a healthy mode. In order to guarantee the reliability of the converter as a result of a power switch faults, additional electrical stresses have to be taken into account for the power devices sizing. Thus, the power devices could withstand the additional current stresses after fault occurrence. On the other hand, if the inductors were oversized, this would lead up to additional volume and cost, which are not fit for automotive applications. For this reason, a thorough study has been carried out to identify accurately the limit of inductors operation, avoiding their saturation and the loss of the control of the converter. This study will allow working out a remedial strategy implemented in a FPGA board to protect inductors against possible saturations.

The additional electrical stresses and saturation of the inductors are not the only issues in the case of degraded operating mode. Indeed, it was shown that the input current ripple increased drastically as a result of a power switch fault. According to the existing literature, a high input current ripple could lead up to long-term degradations on the fuel cell. In order to minimize the undesirable effects on the fuel cell, a fault-tolerant control without using additional components is applied to the interleaved DC/DC converter topology when the fault has been detected by the developed power switch fault detection algorithm. The fault-tolerant control consists in modifying the leg shift of the PWM gate control signals according to the faulty leg. The results obtained by experimental tests have demonstrated that the FC current ripple decreases drastically compared with a degraded operating mode without applying a fault-tolerant control. The current ripple reduction allows improving the fuel cell performance while reducing hydrogen consumption and optimizing its lifetime.

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